

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7WB383FK

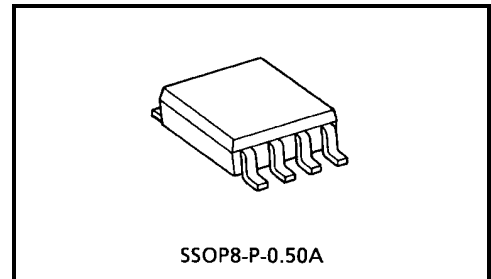
2-Bit Bus Exchange Switch

The TC7WB383FK is a low on-resistance, high-speed CMOS 2-bit bus exchange switch. This bus switch allows the connections or disconnections to be made with minimal propagation delay while maintaining Low power dissipation which is the feature of CMOS.

When output enable (\overline{OE}) is at high level, the switches are off. When at low level, the switches are on, and by the logic of EX terminal, It can choose whether 2 bits data are transferred to the corresponding terminal as it is, or the data are transferred to a terminal with exchanging data line. Therefore it may be used as 2 to 1 multiplexer switch.

Since the switch channels consist of N type MOSFET, the high level output voltage is provided about 1 V lower than VCC level.

All inputs are equipped with protection circuits to protect the device from static discharge.

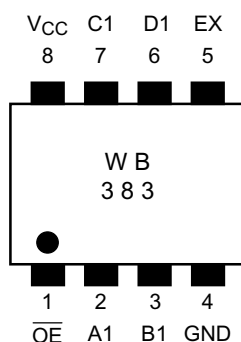


Weight: 0.01 g (typ.)

Features

- Operating voltage: VCC = 4.5~5.5 V
- High speed operation: $t_{pd} = 0.25$ ns (max)
- Ultra-low on resistance: $R_{ON} = 5 \Omega$ (typ.)
- Electro-static discharge (ESD) performance: ± 200 V or more (JEITA)
 ± 2000 V or more (MIL)
- TTL level input (control input)
- Package: US8

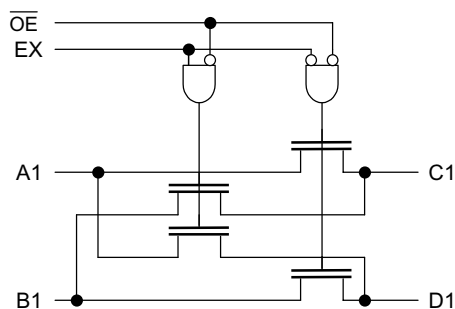
Pin Assignment (top view)



Truth Table

$\overline{\text{OE}}$	EX	A1	B1	C1	D1	Function
H	X	Hi-Z				Disconnect
L	L	A1 = C1, B1 = D1				Connect
L	H	A1 = D1, B1 = C1				Exchange

System Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.5~7.0	V
Control pin input voltage	V_{IN}	-0.5~7.0	V
Switch terminal I/O voltage	V_S	-0.5~7.0	V
Clump diode current	I_{IK}	-50	mA
Switch I/O current	I_S	128	mA
Power dissipation	P_D	200	mW
DC V_{CC} /GND current	I_{CC}/I_{GND}	± 100	mA
Storage temperature	T_{stg}	-65~150	°C

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	4.5~5.5	V
Control pin input voltage	V_{IN}	0~5.5	V
Switch I/O voltage	V_S	0~5.5	V
Operating temperature	T_{opr}	-40~85	°C
Control pin input rise/fall time	dt/dv	0~10	ns/V

Electrical Characteristics

DC Characteristics (Ta = -40~85°C)

Characteristics		Symbol	Test Condition		Min	Typ. (Note 1)	Max	Unit
				V _{CC} (V)				
Control pin input voltage	"H" level	V _{IH}	—	4.5~5.5	2.0	—	—	V
	"L" level	V _{IL}	—	4.5~5.5	—	—	0.8	
Input leakage current		I _{IN}	V _{IN} = 0~5.5 V	4.5~5.5	—	—	±1.0	μA
Power off leakage current		I _{OFF}	A, B, \overline{OE} = 0~5.5 V	0	—	—	±1.0	μA
Off-state leakage current (switch off)		I _{SZ}	A, B = 0~5.5 V, \overline{OE} = V _{CC}	4.5~5.5	—	—	±1.0	μA
ON resistance (Note 2)		R _{ON}	V _{IS} = 0 V	I _{IS} = 64 mA	4.5	—	5	Ω
				I _{IS} = 30 mA	4.5	—	5	
			V _{IS} = 2.4 V, I _{IS} = 15 mA		4.5	—	10	
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND I _{OUT} = 0	5.5	—	—	10	mA
		ΔI _{CC}	V _{IN} = 3.4 V (one input)	5.5	—	—	2.5	

Note 1: The typical values are at V_{CC} = 5 V, Ta = 25°C.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on two (A or B) pins.

AC Characteristics (Ta = -40~85°C)

Characteristics		Symbol	Test Condition		Min	Max	Unit
				V _{CC} (V)			
Propagation delay time (bus to bus)		t _{pLH}	Figure 1, Figure 2 (Note 3)	4.5	—	0.25	ns
		t _{pHL}					
Propagation delay time (EX to bus)		t _{pLH}	Figure 1, Figure 3	4.5	—	4.5	ns
		t _{pHL}					
Output enable time		t _{pZL}	Figure 1, Figure 4	4.5	—	4.5	ns
		t _{pZH}					
Output disable time		t _{pLZ}	Figure 1, Figure 4	4.5	—	5.5	ns
		t _{pHZ}					

Note 3: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitive Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition		Typ.	Unit
				V _{CC} (V)		
Control pin input capacitance		C _{IN}	(Note 4)	5.0	3	pF
Switch terminal capacitance		C _{I/O}	\overline{OE} = V _{CC} (Note 4)	5.0	17	pF

Note 4: This item is guaranteed by design.

AC Test Circuit

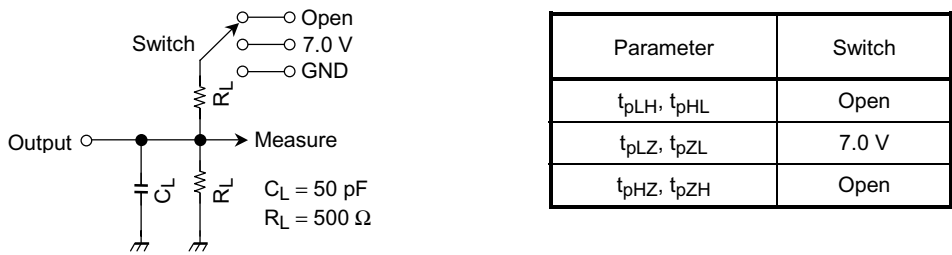


Figure 1

AC Waveform

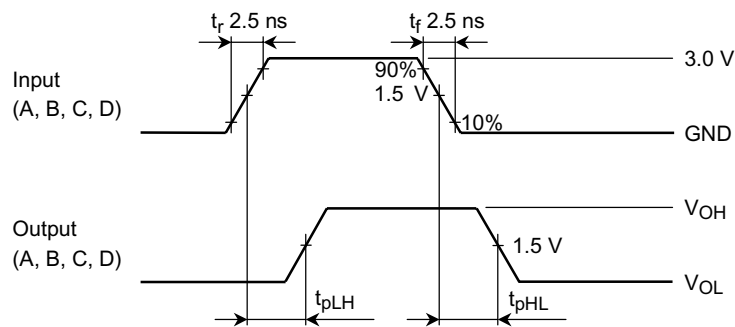


Figure 2 t_{pLH} , t_{pHL}

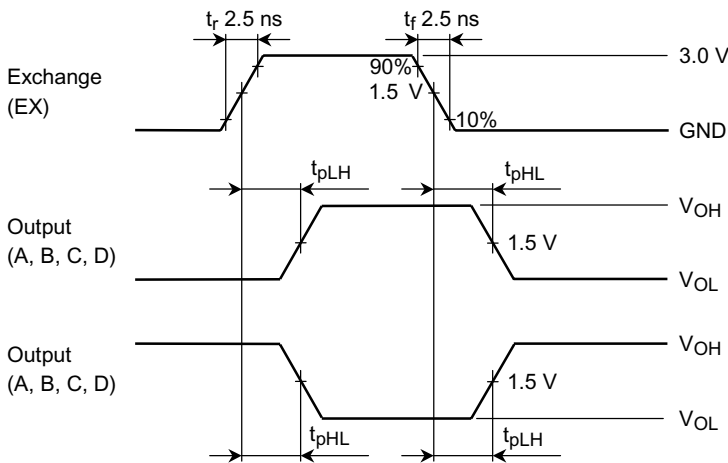


Figure 3 t_{pLH} , t_{pHL}

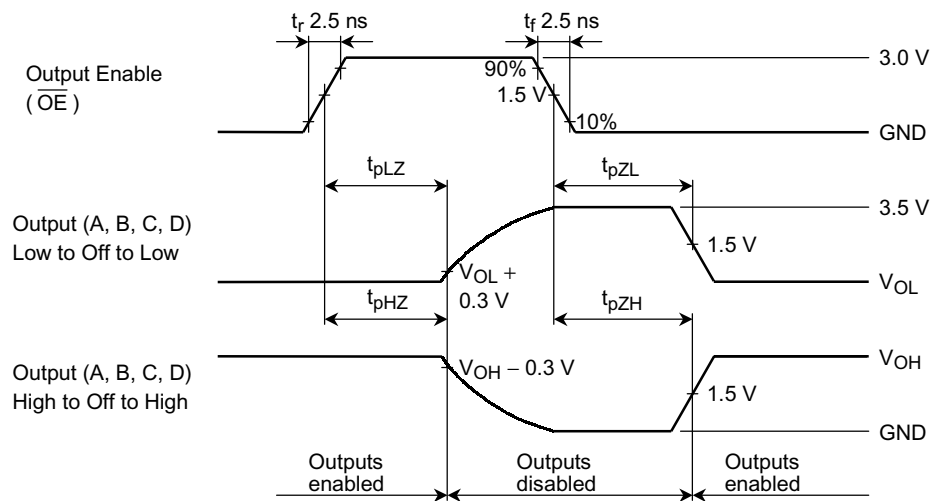
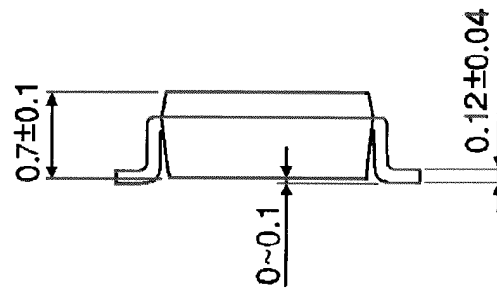


Figure 4 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

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