ATA663232/55

LIN System Basis Chip Including LIN Transceiver, Voltage Regulator and Wake-Input

Features

- Supply Voltage up to 40V
- Operating Voltage V_{VS} = 5V to 28V
- Supply Current
  - Sleep Mode: Typically 9 µA
  - Silent Mode: Typically 47 µA
  - Very Low Current Consumption at Low Supply Voltages (2V < V_{VS} < 5.5V): Typically 130 µA
- Linear Low Drop Voltage Regulator, 85 mA Current Capability:
  - MLC (Multi-Layer Ceramic) Capacitor with 0Ω ESR
  - Normal, Fail-Safe and Silent Mode
    ATA663255: V_{VCC} = 5.0V ± 2%
    ATA663232: V_{VCC} = 3.3V ± 2%
  - Sleep Mode: VCC Is Switched Off
- VCC Undervoltage Detection with Internal Reset (NRES_int)
- Voltage Regulator Is Short Circuit and Overtemperature Protected
- LIN Physical Layer According to LIN 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2
- Wake-Up Capability via LIN Bus (100 µs Dominant) and WKin Pin (100 µs Low Level)
- Wake-Up Source Recognition
- TXD Time-Out Timer
- Bus Pin Is Overtemperature and Short Circuit Protected versus GND and Battery
- Advanced EMC and ESD Performance
- Fulfills the “OEM Hardware Requirements for LIN in Automotive Applications”, Version.1.3
- Interference and Damage Protection According to ISO7637
- Qualified According to AEC-Q100
- Available in 8-Pin, 3 mm x 3 mm VDFN Package with Wettable Flanks (Moisture Sensitivity Level 1)

Applications

- LIN Networks in Automotive
- Industrial
- Medical
- Consumer Applications

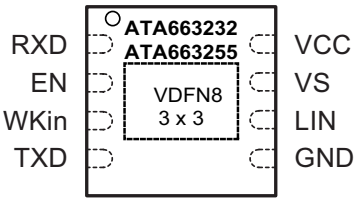
General Description

The ATA663232/55 system basis chip is a fully integrated LIN transceiver, designed according to the LIN specification 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2, with a low drop voltage regulator (3.3V/5V/85 mA) and a high voltage wake-input. The combination of voltage regulator and bus transceiver makes it possible to develop simple but powerful slave nodes in LIN bus systems. ATA663232/55 is designed to handle the low speed data communication in vehicles (for example, in convenience electronics). Improved slope control at the LIN driver ensures secure data communication up to 20 Kbaud. The bus output is designed to withstand high voltage. Sleep mode and Silent mode guarantee minimized current consumption even in the case of a floating or a short circuited LIN bus.

The voltage regulator is a fully integrated low drop voltage regulator, with 5V/3.3V output voltage and 85 mA current capability. It is especially designed for the automotive environment. A key feature is that the current consumption is always below 170 µA (without load), even if the supply voltage is below the regulator’s nominal output voltage.

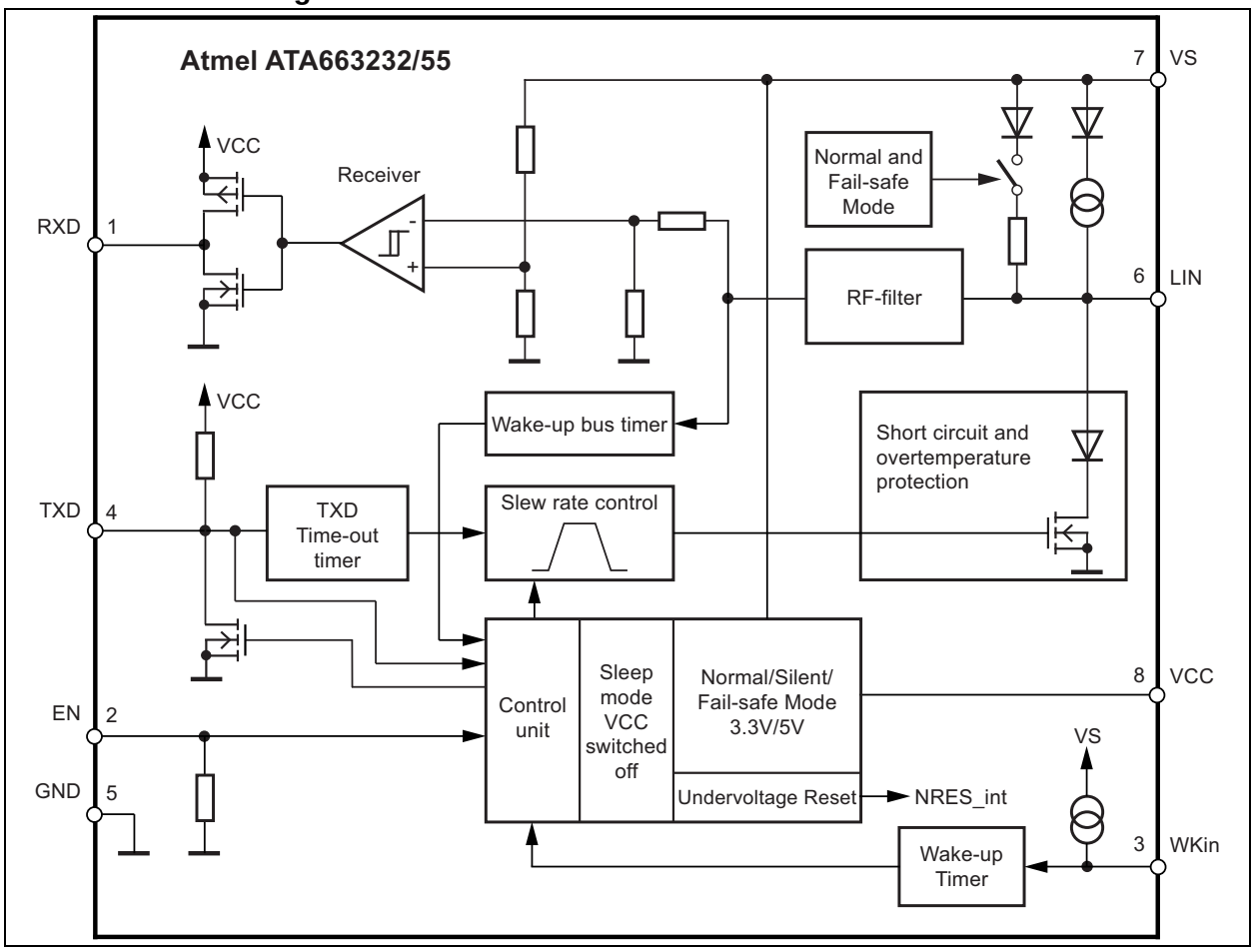
Package Type

ATA663232/55
3 mm x 3 mm 8-Lead VDFN*



* Includes Exposed Thermal Pad (EP); see Table 1-4.

Functional Block Diagram



1.0 FUNCTIONAL DESCRIPTION

1.1 Physical Layer Compatibility

Because the LIN physical layer is independent of higher LIN layers (for example LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes based on earlier versions (LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3) without any restrictions.

1.2 Operating Modes

FIGURE 1-1: OPERATING MODES

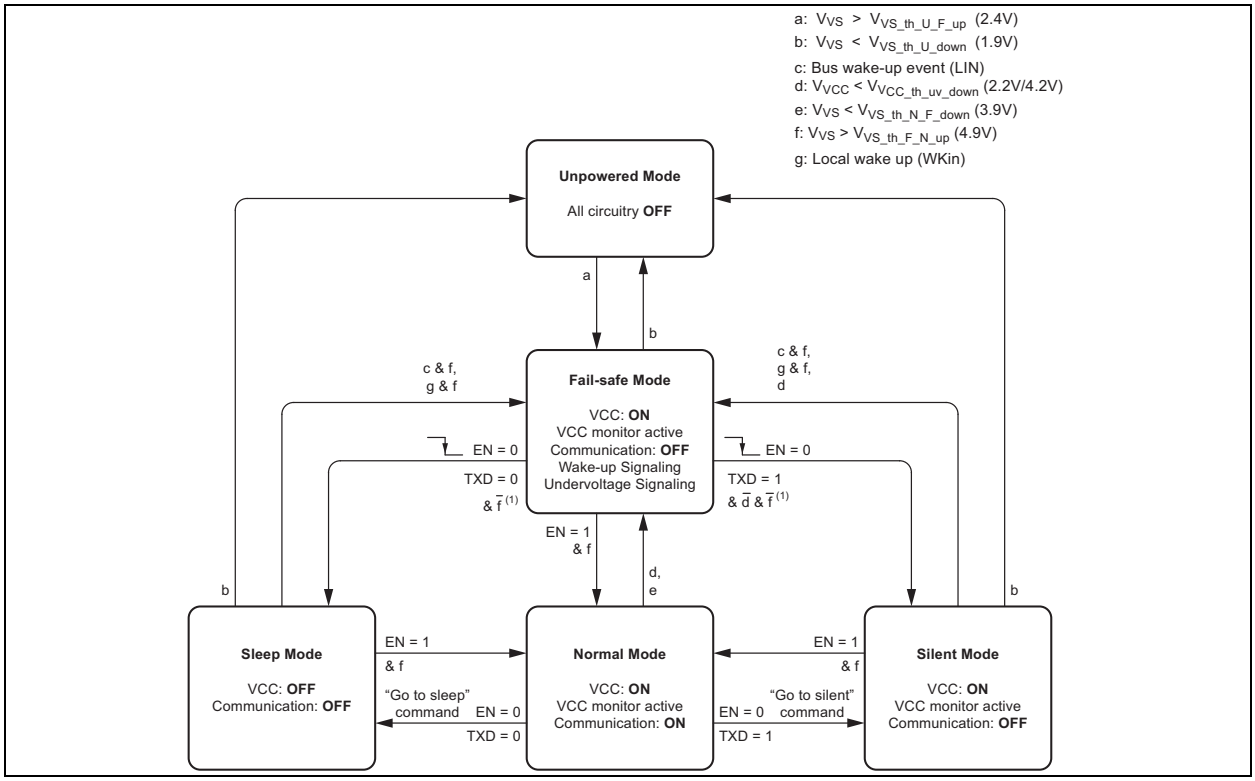


TABLE 1-1: OPERATING MODES

Operating Mode	Transceiver	VCC	LIN	TXD	RXD
Fail-Safe	OFF	3.3V/5V	Recessive	Signaling fail-safe sources (see Table 1-2)	
Normal	ON	3.3V/5V	TXD-dependent	Follows data transmission	
Silent	OFF	3.3V/5V	Recessive	High	High
Sleep/Unpowered	OFF	0V	Recessive	Low	Low

1.2.1 NORMAL MODE

This is the normal transmitting and receiving mode of the LIN Interface, in accordance with LIN specification 2.x.

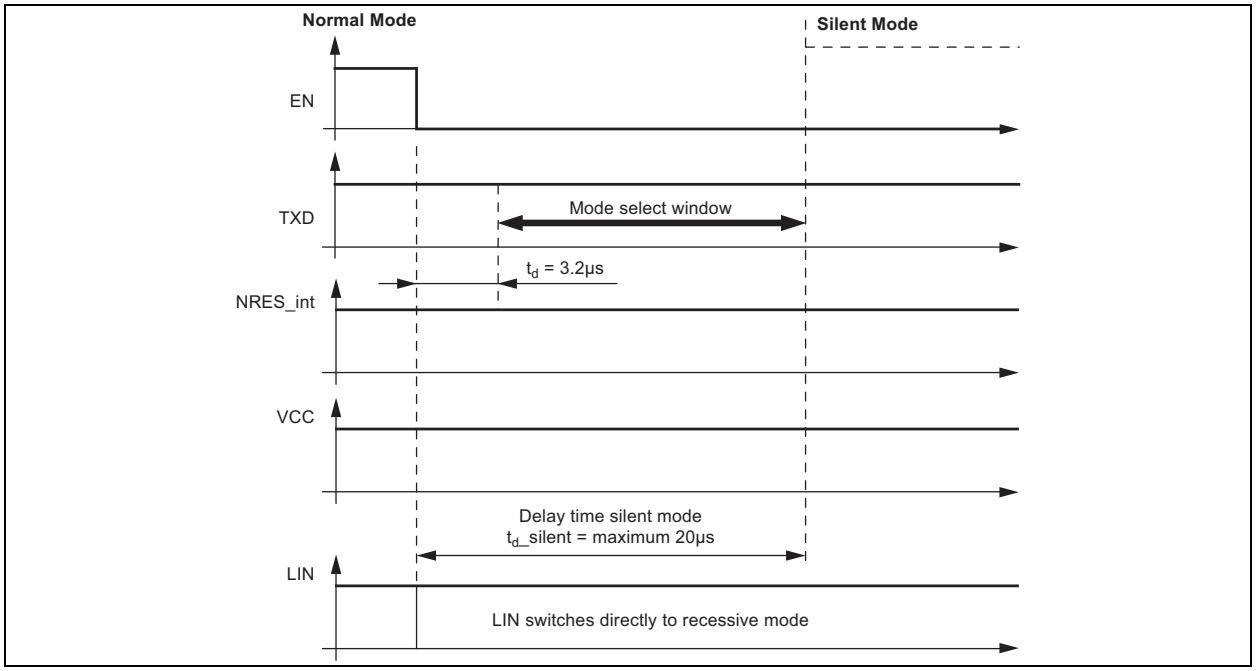
The VCC voltage regulator operates with 3.3V/5V output voltage, with a low tolerance of ±2% and a maximum output current of 85 mA. If an undervoltage condition occurs, the internal reset NRES_int switches to low and the IC changes its state to Fail-Safe mode.

1.2.2 SILENT MODE

A falling edge at EN while TXD is high switches the IC into Silent mode. The TXD signal has to be logic high during the mode select window (Figure 1-2).

The transmission path is disabled in Silent mode. The voltage regulator is active. The overall supply current from V_{Bat} is a combination of the $I_{VSsilent}$ = 47 µA plus the VCC regulator output current I_{VCC}.

FIGURE 1-2: SWITCHING TO SILENT MODE.



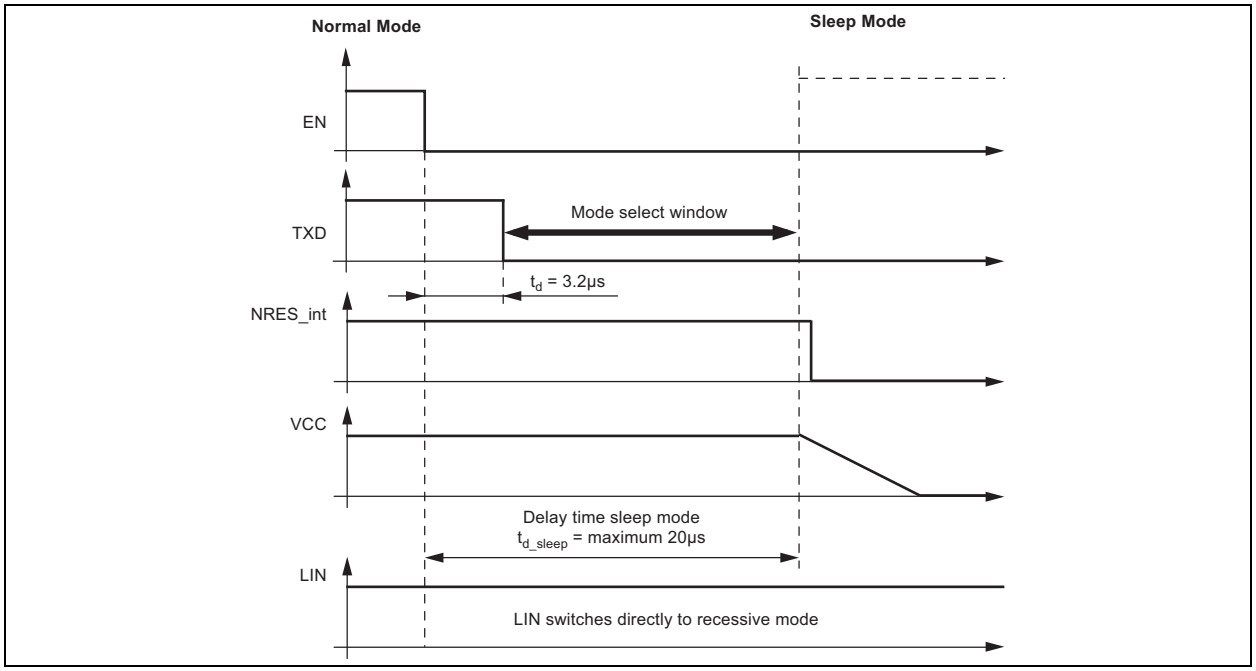
In Silent mode the internal slave termination between the LIN pin and VS pin is disabled to minimize the current consumption in case the pin LIN is short-circuited to GND. Only a weak pull-up current (typically 10 µA) between the LIN pin and VS pin is present. Silent mode can be activated independently from the current level on pin LIN.

If an undervoltage condition occurs, the internal reset NRES_int switches to low and the System Basis Chip (SBC) changes its state to Fail-Safe mode.

1.2.3 SLEEP MODE

A falling edge at EN while TXD is low switches the IC into Sleep mode. The TXD signal has to be logic low during the mode select window (Figure 1-3).

FIGURE 1-3: SWITCHING TO SLEEP MODE



In order to avoid any influence to the LIN pin when switching into Sleep mode it is possible to switch the EN pin up to 3.2 µs earlier to low than the TXD pin. The easiest and best way to do this is by having two falling edges at TXD and EN at the same time.

In Sleep mode, the transmission path is disabled. Supply current from V_{Bat} is typically $I_{VSsleep}$ = 9 µA. The VCC regulator is switched off, the internal reset NRES_int and pin RXD are low. The internal slave termination between the LIN pin and VS pin is disabled to minimize the current consumption in case the LIN pin is short-circuited to GND. Only a weak pull up current (typically 10 µA) between the LIN pin and the VS pin is present. The Sleep mode can be activated independently from the current level on the LIN pin. Voltage below the LIN pre-wake detection V_{LINL} at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer.

If the TXD pin is short circuited to GND, it is possible to switch to Sleep mode via EN after t > t_{dom}.

1.2.4 FAIL-SAFE MODE

The device automatically switches to Fail-Safe mode at system power-up. The voltage regulator is switched on. The internal reset NRES_int remains low for t_{res} = 4 ms and LIN communication is switched off. The IC stays in this mode until EN is switched to high. The IC then changes to Normal mode. A low level at the internal reset NRES_int switches the IC into Fail-Safe mode directly. During Fail-Safe mode the TXD pin is an output and together with the RXD output pin, signals the fail-safe source.

If the device enters Fail-Safe mode coming from the Normal mode (EN = 1) due to an VS undervoltage condition ($V_{VS} < V_{VS\_th\_N\_F\_down}$), it is possible to switch into Sleep or Silent mode by a falling edge at the EN input. With this feature the current consumption can be further reduced.

A wake-up event switches the IC to Fail-Safe mode.

A wake-up event from either Silent or Sleep mode is signaled to the microcontroller using the RXD pin and the TXD pin. A VS undervoltage condition is also signaled at these two pins. The coding is shown in Table 1-2.

TABLE 1-2: SIGNALING IN FAIL-SAFE MODE

Fail-Safe Sources	TXD	RXD
LIN wake-up (LIN pin)	Low	Low
Local wake-up (WKin pin)	Low	High
VS_{th} (battery) undervoltage detection (V_{VS} < 3.9V)	High	Low

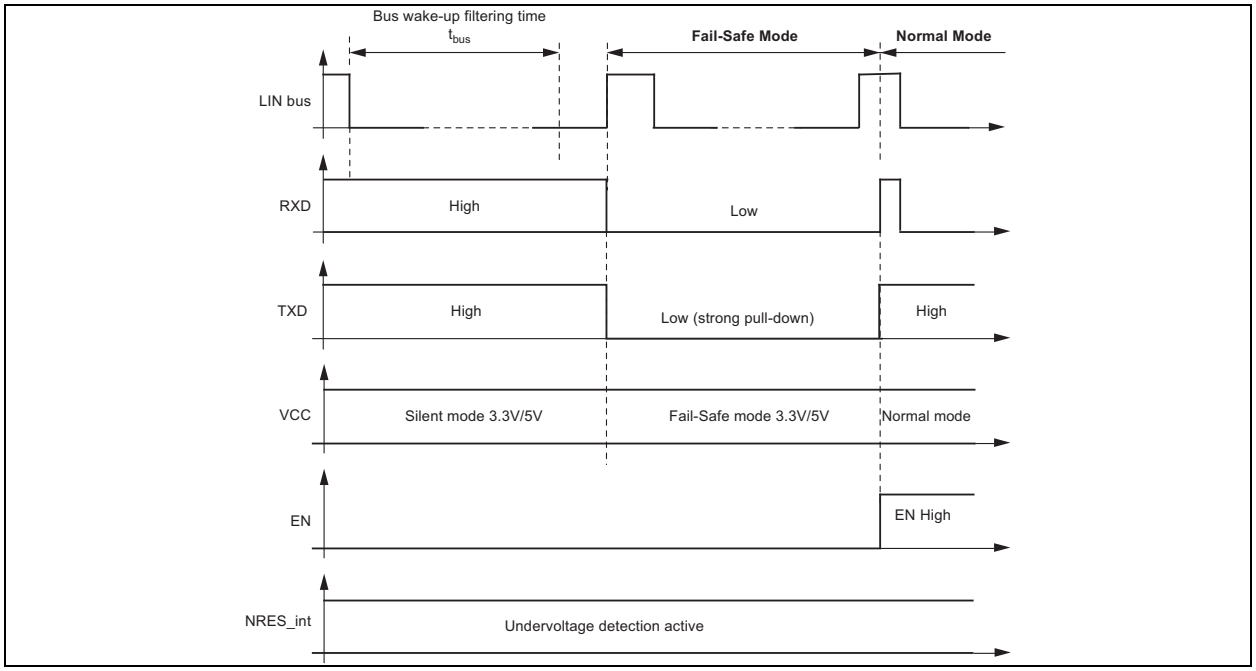
1.3 Wake-Up Scenarios from Silent Mode or Sleep Mode

1.3.1 REMOTE WAKE-UP VIA LIN BUS

1.3.1.1 Remote Wake-up from Silent Mode

A remote wake-up from Silent mode is only possible if TXD is high. A voltage less than the LIN pre-wake detection VLINL at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer. A falling edge at the LIN pin followed by a dominant bus level maintained for a certain period of time (> t_{bus}) and the following rising edge at pin LIN (see Figure 1-4) result in a remote wake-up request. The device switches from Silent mode to Fail-Safe mode, the VCC voltage regulator remains activated and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at the RXD pin and TXD pin (strong pull-down at TXD). EN high can be used to switch directly to Normal mode.

FIGURE 1-4: LIN WAKE-UP FROM SILENT MODE



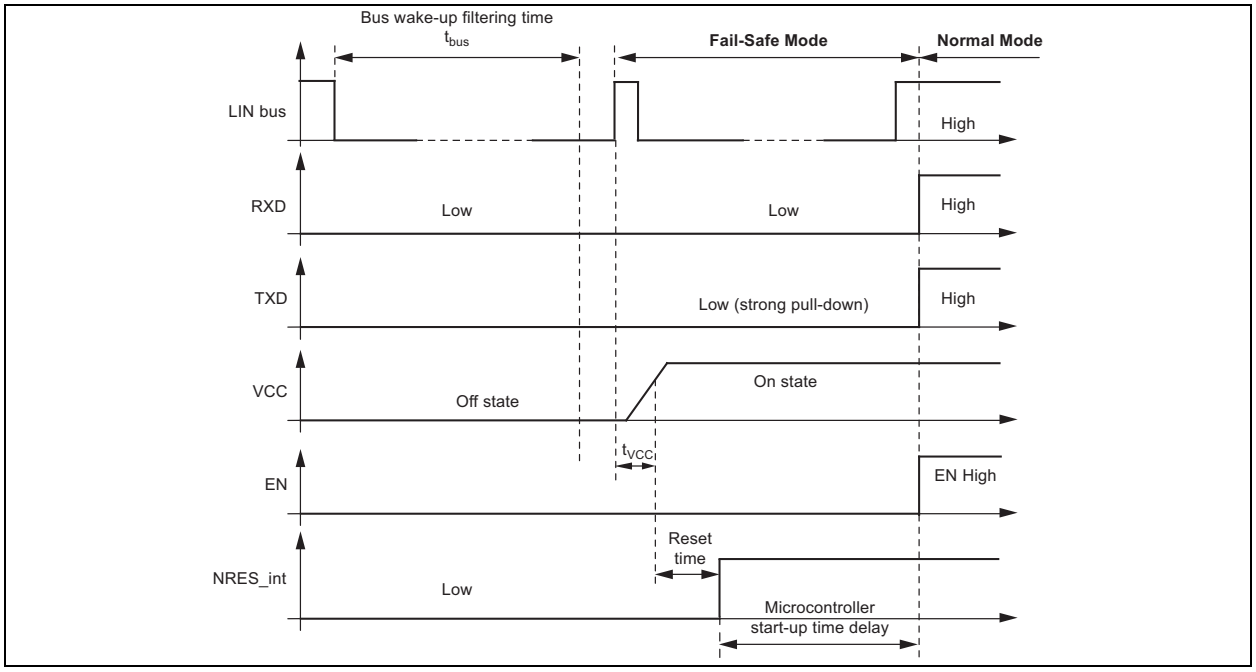
1.3.1.2 Remote Wake-Up from Sleep Mode

A falling edge at the LIN pin followed by a dominant bus level maintained for a certain period of time (> t_{bus}) and a following rising edge at the LIN pin result in a remote wake-up request, causing the device to switch from Sleep mode to Fail-Safe mode.

The VCC regulator is activated, and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at RXD and TXD (strong pull-down at TXD). See Figure 1-5.

EN high can be used to switch directly from Sleep/Silent mode to Normal mode. If EN is still high after VCC ramp-up and undervoltage reset time, the IC switches to Normal mode.

FIGURE 1-5: LIN WAKE-UP FROM SLEEP MODE



1.3.2 LOCAL WAKE-UP VIA WKin PIN

A falling edge at the WKin pin followed by a low level maintained for a given time period (> t_{WKin}) results in a local wake-up request. The device switches to Fail-Safe mode. The internal slave termination resistor is switched on. The local wake-up request is indicated by a low level at the TXD pin to generate an interrupt for the microcontroller. When the WKin pin is low, it is possible to switch to Silent mode or Sleep mode via the EN pin. In this case, the wake-up signal has to be switched to high > 10 µs before the negative edge at WKin starts a new local wake-up request.

FIGURE 1-6: LOCAL WAKE-UP VIA WKin PIN FROM SLEEP MODE

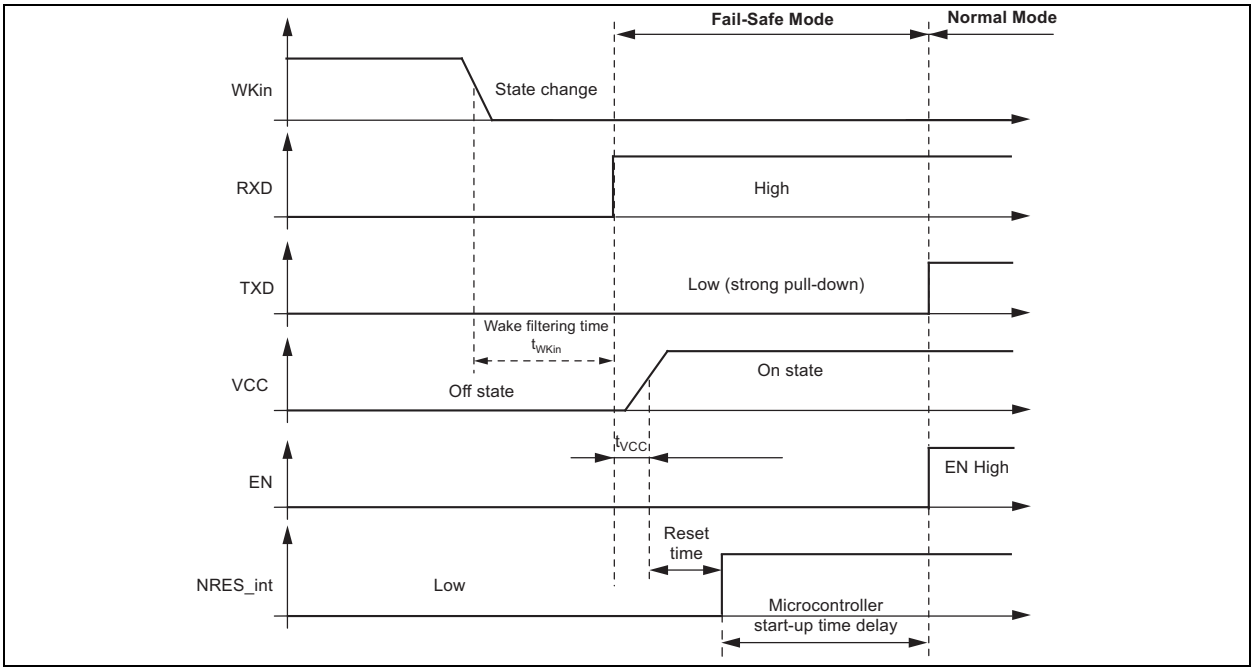
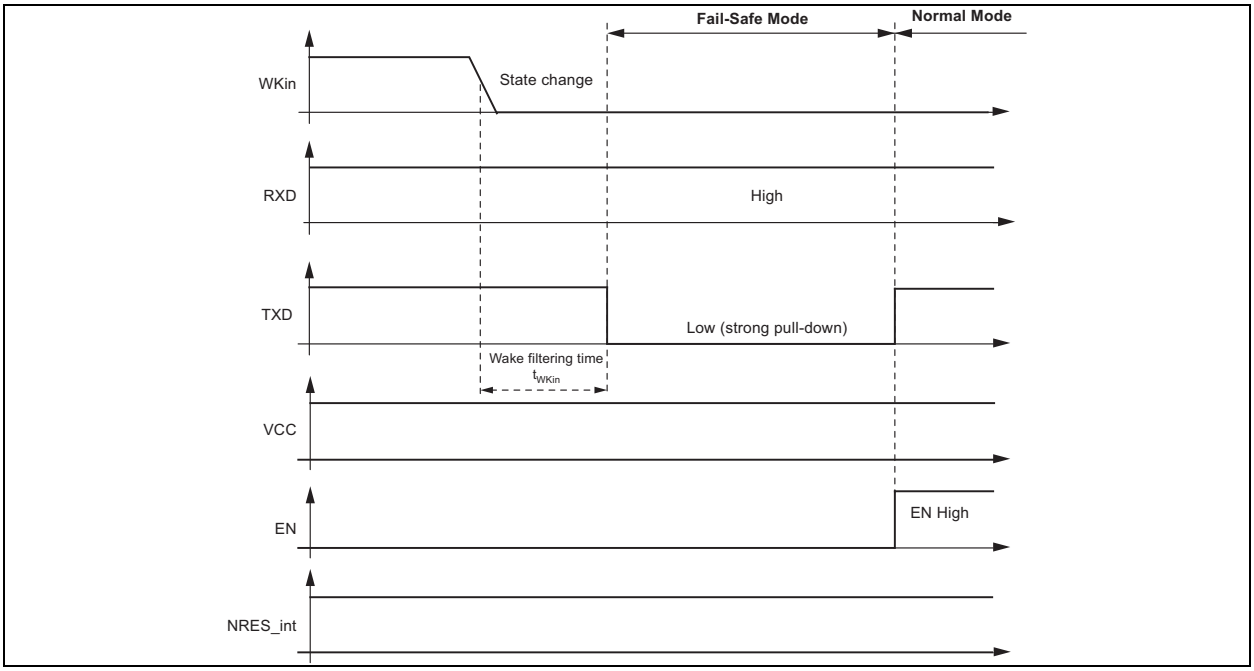


FIGURE 1-7: LOCAL WAKE-UP VIA WKin PIN FROM SILENT MODE



1.3.3 WAKE-UP SOURCE RECOGNITION

The device can distinguish between different wake-up sources. The wake-up source can be read on the TXD and RXD pin in Fail-Safe mode. These flags are immediately reset if the microcontroller sets the EN pin to high and the IC is in Normal mode.

TABLE 1-3: SIGNALING IN FAIL-SAFE MODE

Fail-Safe Sources	TXD	RXD
Bus wake-up (LIN pin)	Low	Low
Local wake-up (WKin pin)	Low	High
VS_{th} (battery) undervoltage detection (VS < 3.9V)	High	Low

1.4 Behavior under Low Supply Voltage Condition

After the battery voltage has been connected to the application circuit, the voltage at the VS pin increases according to the block capacitor used in the application (see Typical Application Circuit). If V_{VS} is higher than the minimum VS operation threshold $V_{VS\_th\_U\_F\_up}$, the IC mode changes from Unpowered mode to Fail-Safe mode. As soon as V_{VS} exceeds the undervoltage threshold $V_{VS\_th\_F\_N\_up}$, the LIN transceiver can be activated.

The VCC output voltage reaches its nominal value after t_{VCC}. This parameter depends on the externally applied VCC capacitor and the load. The internal reset NRES_int output is low for the reset time delay t_{reset}. No mode change is possible during this time t_{reset}.

The behavior of VCC, the internal reset NRES_int and VS is shown in Figure 1-8, Figure 1-9, Figure 1-10 and Figure 1-11.

FIGURE 1-8: VCC AND THE INTERNAL RESET NRES_INT VERSUS VS (RAMP-UP) FOR 3.3V.

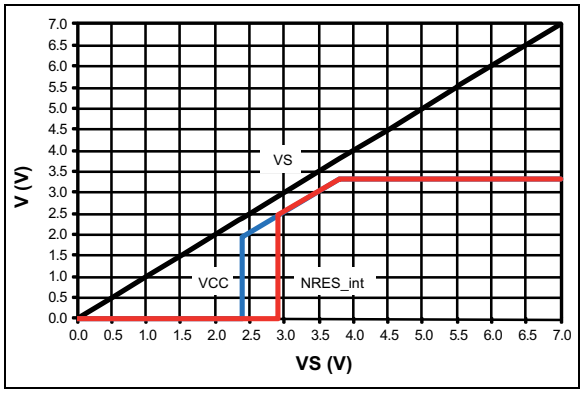


FIGURE 1-9: VCC AND THE INTERNAL RESET NRES_INT VERSUS VS (RAMP-DOWN) FOR 3.3V.

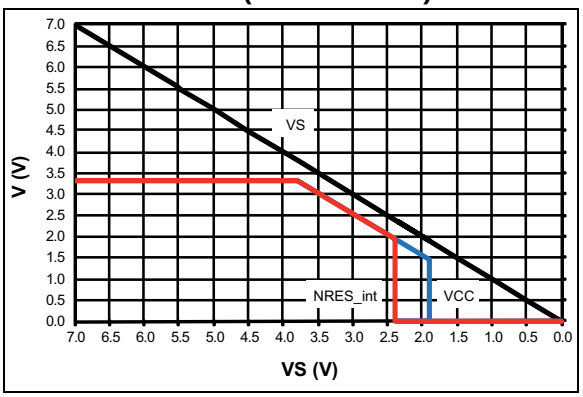


FIGURE 1-10: VCC AND THE INTERNAL RESET NRES_INT VERSUS VS (RAMP-UP) FOR 5V

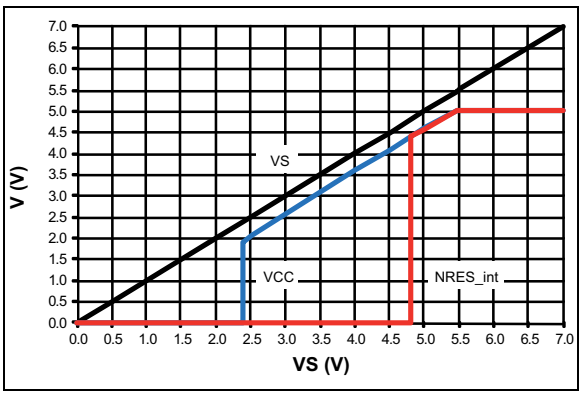
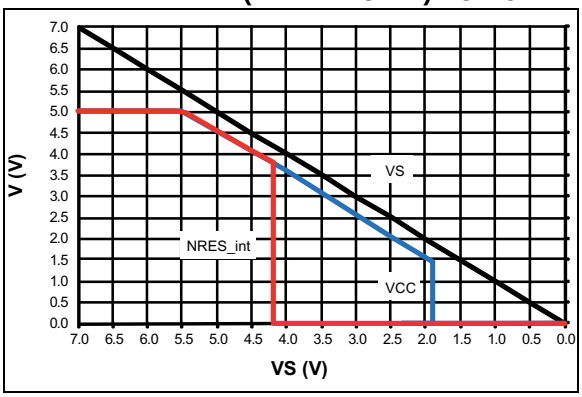


FIGURE 1-11: VCC AND THE INTERNAL RESET NRES_INT VERSUS VS (RAMP-DOWN) FOR 5V.



The graphs are only valid if the VS ramp-up and ramp-down times are much slower than the VCC ramp-up time t_{Vcc} and the internal reset NRES_int delay time t_{reset}.

If during **Sleep mode** the voltage level of V_{VS} drops below the undervoltage detection threshold $V_{VS\_th\_N\_F\_down}$ (typically 4.3V), the operation mode is not changed and no wake-up is possible. Only if the supply voltage on pin VS drops below the VS operation threshold $V_{VS\_th\_U\_down}$ (typically 2.05V), does the IC switch to Unpowered mode.

If during **Silent mode** the VCC voltage drops below the VCC undervoltage threshold $V_{VCC\_th\_uv\_down}$ the IC switches into Fail-Safe mode. If the supply voltage on pin VS drops below the VS operation threshold $V_{VS\_th\_U\_down}$ (typically 2.05V), does the IC switch to Unpowered mode.

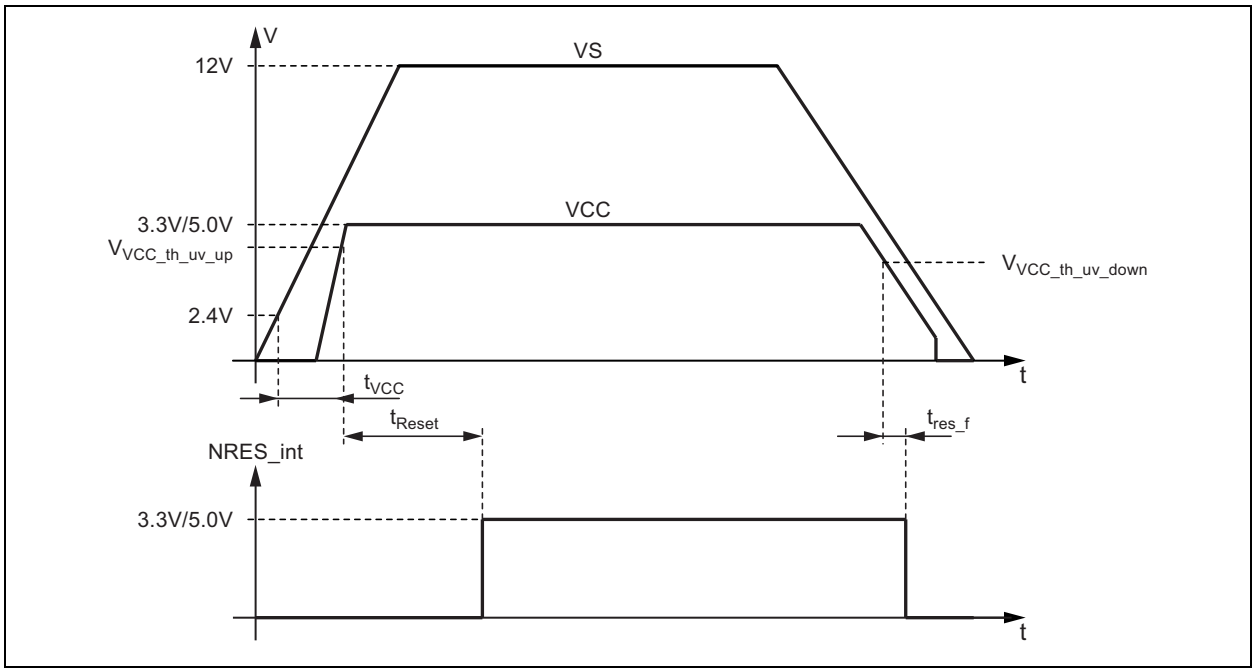
If during **Normal mode** the voltage level on the VS pin drops below the VS undervoltage detection threshold $V_{VS\_th\_N\_F\_down}$ (typically 4.3V), the IC switches to Fail-Safe mode. This means the LIN transceiver is disabled in order to avoid malfunctions or false bus messages. The voltage regulator remains active.

- **For 3.3V SBC**: In this undervoltage situation it is possible to switch the device into Sleep mode or Silent mode by a falling edge at the EN input. For this feature, switching into these two current saving modes is always guaranteed, allowing current consumption to be reduced even further. When the VCC voltage drops below the VCC undervoltage threshold $V_{VCC\_th\_uv\_down}$ (typically 2.6V) the IC switches into Fail-Safe mode.
- **For 5V SBC**: Because of the VCC undervoltage condition in this situation, the IC is in Fail-Safe mode and can be switched into Sleep mode only. Only when the supply voltage V_{VS} drops below the operation threshold $V_{VS\_th\_U\_down}$ (typically 2.05V) does the IC switch into Unpowered mode.

The current consumption of the SBC in Silent mode or in Fail-Safe mode is always below 170 µA, even when the supply voltage V_{VS} is lower than the regulator's nominal output voltage V_{VCC}.

1.5 Voltage Regulator

FIGURE 1-12: VOLTAGE REGULATOR: SUPPLY VOLTAGE RAMP-UP AND RAMP-DOWN



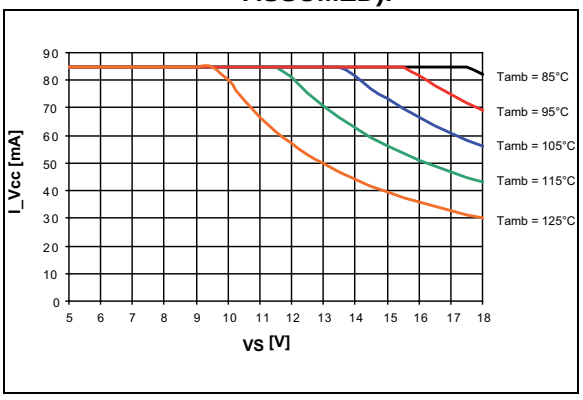
The voltage regulator needs an external capacitor for compensation and to smooth the disturbances from the microcontroller. It is recommended to use a MLC capacitor with a minimum capacitance of 3.5 µF together with a 100 nF ceramic capacitor. Depending on the application, the values of these capacitors can be modified by the customer.

During a short circuit at VCC, the output limits the output current to I_{VCClim}. Because of undervoltage, the internal reset NRES_int switches to low. If the chip temperature exceeds the value T_{VCCoff}, the VCC output switches off. The chip cools down and, after a hysteresis of T_{hys}, switches the output on again.

When the ATA663232/55 is being soldered onto the PCB it is mandatory to connect the exposed thermal pad with a wide GND plate on the printed board to get a good heat sink.

The main power dissipation of the IC is created from the VCC output current I_{VCC}, which is needed for the application. See Figure 1-13.

FIGURE 1-13: POWER DISSIPATION: SAFE OPERATING AREA: REGULATOR'S OUTPUT CURRENT I_{VCC} VERSUS SUPPLY VOLTAGE VS AT DIFFERENT AMBIENT TEMPERATURES (R_{thJA} = 50K/W ASSUMED).



1.6 Pin Descriptions

The descriptions of the pins are listed in Table 1-4.

TABLE 1-4: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1	RXD	Receive data output.
2	EN	Enables Normal mode if the input is high.
3	WKin	High voltage input for local wake-up request. If not needed, connect directly to VS.
4	TXD	Transmit data input.
5	GND	Ground, exposed thermal pad.
6	LIN	LIN bus line input/output.
7	VS	Supply voltage.
8	VCC	Output voltage regulator 3.3V/5V/85 mA.
EP	EP	Exposed Thermal Pad (GND).

1.6.1 OUTPUT PIN (RXD)

In Normal mode this pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is indicated by a high level at RXD; LIN low (dominant state) is indicated by a low level at RXD.

The output is a push-pull stage switching between VCC and GND. The AC characteristics are measured by an external load capacitor of 20 pF.

In silent mode the RXD output switches to high.

1.6.2 ENABLE INPUT PIN (EN)

The enable input pin controls the operating mode of the device. If EN is high, the circuit is in Normal mode, with transmission paths from TXD to LIN and from LIN to RXD both active. The VCC voltage regulator operates with 3.3V/5V/85 mA output capability.

If EN is switched to low while TXD is still high, the device is forced to Silent mode. No data transmission is then possible, and current consumption is reduced to $I_{VSsilent}$ typ. 47 µA. The VCC regulator retains its full functionality.

If EN is switched to low while TXD is low, the device is forced to Sleep mode. No data transmission is possible, and the voltage regulator is switched off.

The EN pin provides a pull down resistor to force the transceiver into recessive mode if EN is disconnected.

1.6.3 WAKE INPUT PIN (WKin)

The WKin pin is a high-voltage input used to wake-up the device from Sleep mode or Silent mode. It is usually connected to an external switch in the application to generate a local wake-up. A pull-up current source with typically 10 µA is implemented. The voltage threshold for a wake-up signal is typically 2V below the VS voltage. If a local wake-up is not needed in the application, the WKin pin can be connected directly to the VS pin.

1.6.4 INPUT/OUTPUT (TXD)

In Normal mode the TXD pin is the microcontroller interface for controlling the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high or unconnected (internal pull up resistor), the LIN output transistor is turned off and the bus is in the recessive state. If the TXD pin stays at GND level while switching into Normal mode, it must be pulled to high level longer than 10 µs before the LIN driver can be activated. This feature prevents the bus line from being accidentally driven to dominant state after Normal mode has been activated (also in case of a short circuit at TXD to GND). During Fail-Safe mode, this pin is used as output and signals the fail-safe source.

The TXD input has an internal pull up resistor.

An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{dom} > 20 ms, the LIN bus driver is switched to the recessive state. Nevertheless, when switching to Sleep mode, the actual level at the TXD pin is relevant.

To reactivate the LIN bus driver, switch TXD to high (> 10 µs).

1.6.5 GROUND PIN (GND)

The IC does not affect the LIN bus in the event of GND disconnection. It is able to handle a ground shift of up to 11.5% of V_{VS}.

1.6.6 BUS PIN (LIN)

A low side driver with internal current limitation and thermal shut down as well as an internal pull up resistor according to LIN specification 2.x is implemented. The voltage range is from –27V to +40V. This pin exhibits no reverse current from the LIN bus to VS, even in the

event of a GND shift or VBat disconnection. The LIN receiver thresholds comply with the LIN protocol specification.

The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope-controlled.

During a short circuit at LIN to V_{Bat}, the output limits the output current to I_{BUS_LIM}. Due to the power dissipation, the chip temperature exceeds T_{LINoff} and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. RXD stays on high because LIN is high. The VCC regulator works independently during LIN overtemperature switch-off.

During a short circuit from LIN to GND the IC can be switched into Sleep or Silent mode and even in this case the current consumption is lower than 100 µA in Sleep mode and lower than 120 µA in Silent mode. If the short circuit disappears, the IC starts with a remote wake-up.

The reverse current is < 2 µA at pin LIN during loss of V_{Bat}. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.

1.6.7 SUPPLY PIN (VS)

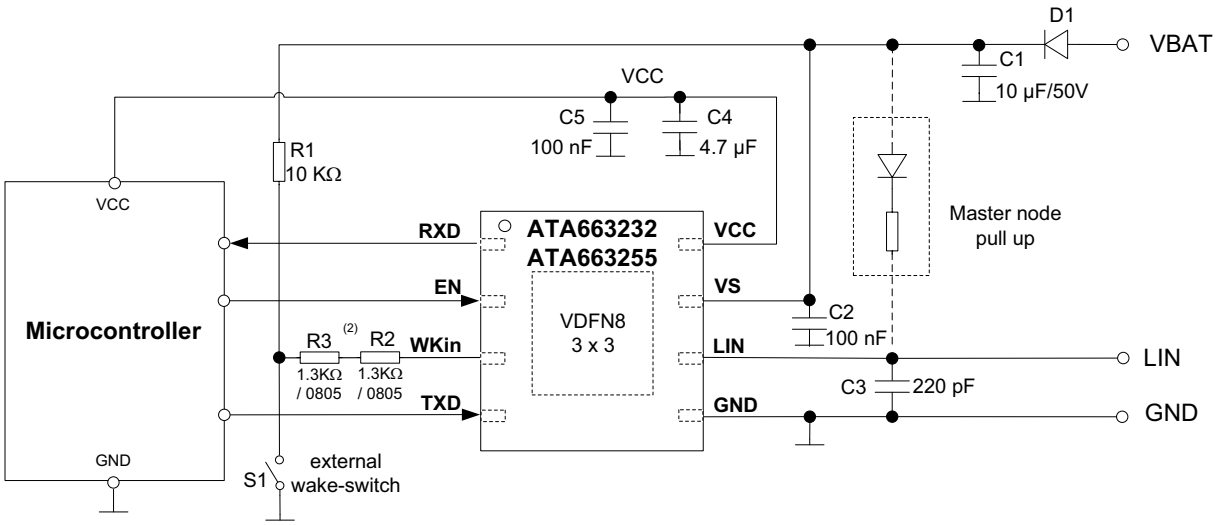
LIN operating voltage is V_{VS} = 5V to 28V. Undervoltage detection is implemented to disable transmission if V_{VS} falls below typ. 4.5V, thereby avoiding false bus messages. After switching on V_{VS}, the IC starts in Fail-Safe mode and the voltage regulator is switched on.

The supply current in Sleep mode is typically 9 µA and 47 µA in Silent mode.

1.6.8 VOLTAGE REGULATOR OUTPUT PIN (VCC)

The internal 3.3V/5V voltage regulator is capable of driving loads up to 85 mA, supplying the microcontroller and other ICs on the PCB and is protected against overload by means of current limitation and overtemperature shutdown. Furthermore, the output voltage is monitored and causes an internal reset signal NRES_int, if it drops below a defined threshold $V_{VCC\_th\_uv\_down}$.

Typical Application Circuit



Note 1: The Exposed Thermal Pad must always be connected to GND.

2: With these 2 resistors in series at the WKin- pin +/-6 kV ESD robustness according IEC61000-4-2 is achieved.

2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage V_{VS} ..... –0.3V to +40V
VS Pulse Time ≤ 500 ms, Tamb = +25°C, Output Current I_{VCC} ≤ 85 mA ..... +43.5V
VS Pulse Time ≤ 2 min, Tamb = +25°C, Output Current I_{VCC} ≤ 85 mA ..... +28V
Logic Pins:
Voltage Levels (RxD, TxD, EN), V_{Logic} ..... –0.3V to +5.5V
Output DC Currents, I_{Logic} ..... –5 mA to +5 mA
LIN:
DC Voltage, V_{LIN} ..... –27V to +40V
Pulse Time < 500 ms, V_{LIN} ..... –27V to +43.5V
WKin Voltage Levels:
DC Voltage, V_{WKin} ..... –0.3V to +40V
Transient Voltage(1), V_{WKin} ..... –150V to +100V
VCC:
DC Voltage, V_{VCC} ..... –0.3V to +5.5V
DC Input Current, I_{VCC} ..... +200 mA
ESD(2) Pin VS, LIN, WKin to GND (with external circuitry according to applications diagram) ..... ± 6 kV
ESD HBM following STM5.1 with 1.5 kΩ/100 pF:
Pin VS, LIN to GND ..... ± 6 kV
Pin WKin to GND ..... ± 5 kV
HBM ESD, ANSI/ESD-STM5.1, JESD22-A114, AEC-Q100 (002) ..... ± 3 kV
CDM ESD STM 5.3.1 ..... ± 750 V
Machine Model ESD AEC-Q100-RevF(003) ..... ± 200 V
Virtual Junction Temperature, T_{vJ} ..... –40°C to +150°C
Storage Temperature, T_{stg} ..... –55°C to +150°C

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not ensured to function outside its operating ratings.

Note 1: According to ISO7637 (coupling 1 nF), with 2 x 1.3 kΩ.

2: According to IBEE LIN EMC Test specification 1.0 following IEC 61000-4-2.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{vJ} < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
1	**VS Pin**						
1.1	Nominal DC Voltage Range	VS	5	13.5	28	V	
1.2	Supply Current in Sleep Mode	$I_{VSsleep}$	6	9	15	µA	Sleep mode V_{LIN} > V_{VS} – 0.5V V_{VS} < 14V, T = 27°C (**Note 1**)
		$I_{VSsleep}$	3	11	18	µA	Sleep mode V_{LIN} > V_{VS} – 0.5V V_{VS} < 14V
		$I_{VSsleep\_short}$	20	50	100	µA	Sleep mode V_{LIN} = 0V bus shorted to GND V_{VS} < 14V
1.3	Supply Current in Silent Mode	$I_{VSsilent}$	30	47	58	µA	Bus recessive 5.5V < V_{VS} < 14V without load at VCC T = 27°C (**Note 1**)
		$I_{VSsilent}$	30	50	64	µA	Bus recessive 5.5V < V_{VS} < 14V without load at VCC
		$I_{VSsilent}$	50	130	170	µA	Bus recessive 2V < V_{VS} < 5.5V without load at VCC
		$I_{VSsilent\_short}$	50	80	120	µA	Silent mode 5.5V < V_{VS} < 14V bus shorted to GND without load at VCC
1.4	Supply Current in Normal Mode	I_{VSrec}	150	230	290	µA	Bus recessive V_{VS} < 14V without load at VCC
1.5	Supply Current in Normal Mode	I_{VSdom}	200	700	950	µA	Bus dominant (internal LIN pull up resistor active) V_{VS} < 14V without load at VCC
1.6	Supply current in Fail-Safe Mode	I_{VSfail}	40	55	80	µA	Bus recessive 5.5V < V_{VS} < 14V without load at VCC
		I_{VSfail}	50	130	170	µA	Bus recessive 2.0V < V_{VS} < 5.5V without load at VCC
1.7	VS Undervoltage Threshold (Switching from Normal to Fail-Safe Mode)	$V_{VS\_th\_N\_F\_down}$	3.9	4.3	4.7	V	Decreasing supply voltage
		$V_{VS\_th\_F\_N\_up}$	4.1	4.6	4.9	V	Increasing supply voltage
1.8	VS Undervoltage Hysteresis	$V_{VS\_hys\_F\_N}$	0.1	0.25	0.4	V	
1.9	VS Operation Threshold (Switching to Unpowered Mode)	$V_{VS\_th\_U\_down}$	1.9	2.05	2.3	V	Switch to Unpowered mode
		$V_{VS\_th\_U\_up}$	2.0	2.25	2.4	V	Switch from Unpowered to Fail-Safe mode
1.10	VS Undervoltage Hysteresis	$V_{VS\_hys\_U}$	0.1	0.2	0.3	V	
2	**RXD Output Pin**						
2.1	Low Level Output Sink Capability	V_{RXDL}	—	0.2	0.4	V	Normal mode, V_{LIN} = 0V, I_{RXD} = 2 mA

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{VJ} < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
2.2	High-Level Output Source Capability	V_{RXDH}	V_{VCC} – 0.4V	V_{VCC}– 0.2V	—	V	Normal mode V_{LIN} = V_{VS}, I_{RXD} = – 2mA
3	**TXD Input/Output Pin**						
3.1	Low-Level Voltage Input	V_{TXDL}	–0.3	—	+0.8	V	
3.2	High-Level Voltage Input	V_{TXDH}	2	—	V_{VCC} + 0.3V	V	
3.3	Pull-Up Resistor	R_{TXD}	40	70	100	kΩ	V_{TXD} = 0V
3.4	High-Level Leakage Current	I_{TXD}	–3	—	+3	µA	V_{TXD} = V_{VCC}
3.7	Low-Level Output Sink Current at LIN Wake-Up Request	I_{TXD}	2	2.5	8	mA	Fail-Safe mode V_{LIN} = V_{VS} V_{TXD} = 0.4V
4	**EN Input Pin**						
4.1	Low-Level Voltage Input	V_{ENL}	–0.3	—	+0.8	V	
4.2	High-Level Voltage Input	V_{ENH}	2	—	V_{VCC} + 0.3V	V	
4.3	Pull-Down Resistor	R_{EN}	50	125	200	kΩ	V_{EN} = V_{VCC}
4.4	Low-Level Input Current	I_{EN}	–3	—	+3	µA	V_{EN} = 0V
5	**Internal Reset NRES_int**						
5.1	Undervoltage Reset Time	t_{Reset}	2	4	6	ms	V_{VS} ≥ 5.5V (**Note 1**)
5.2	Reset Debounce Time for Falling Edge	t_{res_f}	0.5	—	10	µs	V_{VS} ≥ 5.5V (**Note 3**)
6	**WKin Pin**						
6.1	High-Level Input Voltage	V_{WKinH}	V_{VS} – 1V	—	V_{VS} + 0.3V	V	
6.2	Low-Level Input Voltage	V_{WKinL}	–1	—	V_{VS} –3.3V	V	Initializes a wake-up signal
6.3	WKin Pull-Up Current	I_{WKin}	–30	–10	—	µA	V_{VS} < 28V, V_{WKin} = 0V
6.4	High-Level Leakage Current	I_{WKinL}	–5	—	+5	µA	V_{VS} = 28V, V_{WKin} = 28V
6.5	Debounce Time of Low Pulse for Wake-Up via WKin Pin	t_{WKL}	50	100	150	µs	V_{WKin} = 0V
8	**VCC Voltage Regulator (3.3V)**						
8.1	Output Voltage VCC	V_{VCCnor}	3.234	—	3.366	V	4V < V_{VS} < 18V (0 mA to 50 mA)
		V_{VCCnor}	3.234	—	3.366	V	4.5V < V_{VS} < 18V (0 mA to 85 mA) (**Note 2**)

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{vJ} < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
8.2	Output Voltage V_{VCC} at Low V_{VS}	V_{VCClow}	V_{VS} – V_D	—	3.366	V	3V < V_{VS} < 4V
8.3	Regulator Drop Voltage	V_{D1}	—	100	150	mV	V_{VS} > 3V, I_{VCC} = –15 mA
8.4	Regulator Drop Voltage	V_{D2}	—	300	500	mV	V_{VS} > 3V, I_{VCC} = –50 mA
8.5	Line Regulation Maximum	VCC_{line}	—	0.1	0.2	%	4V < V_{VS} < 18V
8.6	Load Regulation Maximum	VCC_{load}	—	0.1	0.5	%	5 mA < I_{VCC} < 50 mA
8.7	Output Current Limitation	I_{VCClim}	—	–180	–120	mA	V_{VS} > 4V
8.8	Load Capacity	C_{load}	3.5	4.7	—	µF	MLC capacitor (**Note 3**)
8.9	VCC Undervoltage Threshold (NRES_int low)	$V_{VCC\_th\_uv\_down}$	2.2	2.5	2.8	V	Referred to VCC V_{VS} > 4V
	VCC Undervoltage Threshold (NRES_int high)	$V_{VCC\_th\_uv\_up}$	2.4	2.6	2.9	V	Referred to VCC V_{VS} > 4V
8.10	Hysteresis of VCC Undervoltage Threshold	$V_{VCC\_hys\_uv}$	100	200	300	mV	Referred to VCC V_{VS} > 4V
8.11	Ramp-Up Time V_{VS} > 4V to V_{VCC} = 3.3V	t_{VCC}	—	1	1.5	ms	C_{VCC} = 4.7 µF I_{load} = –5 mA at VCC
9	**VCC Voltage Regulator (5V)**						
9.1	Output voltage VCC	V_{VCCnor}	4.9	—	5.1	V	5.5V < V_{VS} < 18V (0 mA to 50 mA)
		V_{VCCnor}	4.9	—	5.1	V	6V < V_{VS} < 18V (0 mA to 85 mA) (**Note 2**)
9.2	Output Voltage V_{VCC} at Low V_{VS}	V_{VCClow}	V_{VS} – V_D	—	5.1	V	4V < V_{VS} < 5.5V
9.3	Regulator Drop Voltage	V_{D1}	—	100	200	mV	V_{VS} > 4V, I_{VCC} = –20 mA
9.4	Regulator Drop Voltage	V_{D2}	—	300	500	mV	V_{VS} > 4V, I_{VCC} = –50 mA
9.5	Regulator Drop Voltage	V_{D3}	—	—	150	mV	V_{VS} > 3.3V, I_{VCC} = –15 mA
9.6	Line Regulation Maximum	VCC_{line}	—	0.1	0.2	%	5.5V < V_{VS} < 18V
9.7	Load Regulation Maximum	VCC_{load}	—	0.1	0.5	%	5 mA < I_{VCC} < 50 mA
9.8	Output Current Limitation	I_{VCClim}	—	–180	–120	mA	V_{VS} > 5.5V
9.9	Load Capacity	C_{load}	3.5	4.7	—	µF	MLC capacitor (**Note 3**)

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{VJ} < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
9.10	VCC Undervoltage Threshold (NRES_int low)	$V_{VCC\_th\_uv\_down}$	4.2	4.4	4.6	V	Referred to VCC V_{VS} > 4V
	VCC Undervoltage Threshold (NRES_int high)	$V_{VCC\_hys\_uv}$	4.3	4.6	4.8	V	Referred to VCC V_{VS} > 4V
9.11	Hysteresis of Undervoltage Threshold	$V_{VCC\_hys\_uv}$	100	200	300	mV	Referred to VCC V_{VS} > 5.5V
9.12	Ramp-Up Time V_{VS} > 5.5V to V_{VCC} = 5V	t_{VCC}	—	1	1.5	ms	C_{VCC} = 4.7 µF I_{load} = –5 mA at VCC
10	**LIN Bus Driver: Bus Load Conditions: Load 1 (small): 1 nF, 1 kΩ; Load 2 (large): 10 nF, 500Ω;; C_{RXD} = 20 pF, Load 3 (medium): 6.8 nF, 660Ω characterized on samples 12.7 and 12.8 specifies the timing parameters for proper operation at 20 kb/s and 12.9 and 12.10 at 10.4 kb/s**						
10.1	Driver Recessive Output Voltage	V_{BUSrec}	0.9 * V_{VS}	—	V_{VS}	V	Load1/Load2
10.2	Driver Dominant Voltage	$V_{\_LoSUP}$	—	—	1.2	V	V_{VS} = 7V R_{load} = 500Ω
10.3	Driver Dominant Voltage	$V_{\_HiSUP}$	—	—	2	V	V_{VS} = 18V R_{load} = 500Ω
10.4	Driver Dominant Voltage	$V_{\_LoSUP\_1k}$	0.6	—	—	V	V_{VS} = 7V R_{load} = 1000Ω
10.5	Driver Dominant Voltage	$V_{\_HiSUP\_1k}$	0.8	—	—	V	V_{VS} = 18V R_{load} = 1000Ω
10.6	Pull-Up Resistor to V_{VS}	R_{LIN}	20	30	47	kΩ	The serial diode is mandatory
10.7	Voltage Drop at the Serial Diodes	$V_{SerDiode}$	0.4	—	1.0	V	In pull-up path with R_{slave} $I_{SerDiode}$ = 10 mA (**Note 3**)
10.8	LIN Current Limitation V_{BUS} = V_{Bat_max}	I_{BUS_LIM}	40	120	200	mA	
10.9	Input Leakage Current at the Receiver Including Pull-Up Resistor as Specified	$I_{BUS\_PAS\_dom}$	–1	–0.35	—	mA	Input leakage current driver off V_{BUS} = 0V V_{Bat} = 12V
10.10	Leakage Current LIN Recessive	$I_{BUS\_PAS\_rec}$	—	10	20	µA	Driver off 8V < V_{Bat} < 18V 8V < V_{BUS} < 18V V_{BUS} ≥ V_{Bat}

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{vJ} < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
10.11	Leakage Current when Control Unit Disconnected from Ground. Loss of local ground must not affect communication in the residual network.	$I_{BUS\_NO\_gnd}$	–10	+0.5	+10	µA	GND_{Device} = V_{VS} V_{Bat} = 12V 0V < V_{BUS} < 18V
10.12	Leakage Current at Disconnected Battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	$I_{BUS\_NO\_bat}$	—	0.1	2	µA	V_{Bat} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V
10.13	Capacitance on pin LIN to GND	C_{LIN}	—	—	20	pF	Note 3
11	**LIN Bus Receiver**						
11.1	Center of Receiver Threshold	V_{BUS_CNT}	0.475 * V_{VS}	0.5 * V_{VS}	0.525 * V_{VS}	V	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2
11.2	Receiver Dominant State	V_{BUSdom}	–27	—	0.4 * V_{VS}	V	V_{EN} = 5V/3.3V
11.3	Receiver Recessive State	V_{BUSrec}	0.6 * V_{VS}	—	40	V	V_{EN} = 5V/3.3V
11.4	Receiver Input Hysteresis	V_{BUShys}	0.028 * V_{VS}	0.1 * V_{VS}	0.175 * V_{VS}	V	V_{hys} = V_{th_rec} – V_{th_dom}
11.5	Pre-Wake Detection LIN High-Level Input Voltage	V_{LINH}	V_{VS} – 2V	—	V_{VS} + 0.3V	V	
11.6	Pre-Wake Detection LIN Low-Level Input Voltage	V_{LINL}	–27	—	V_{VS} – 0.3V	V	Activates the LIN receiver
12	**Internal Timers**						
12.1	Dominant Time for Wake-Up via LIN Bus	t_{bus}	50	100	150	µs	V_{LIN} = 0V
12.2	Time Delay for Mode Change from Fail-Safe into Normal Mode via EN Pin	t_{norm}	5	15	20	µs	V_{EN} = 5V/3.3V
12.3	Time Delay for Mode Change from Normal Mode to Sleep Mode via EN Pin	t_{sleep}	5	15	20	µs	V_{EN} = 0V
12.5	TXD Dominant Time-Out Time	t_{dom}	20	40	60	ms	V_{TXD} = 0V

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: 5V < V_{VS} < 28V, –40°C < T_{vJ} < 150°C; unless otherwise specified all values refer to GND pins.

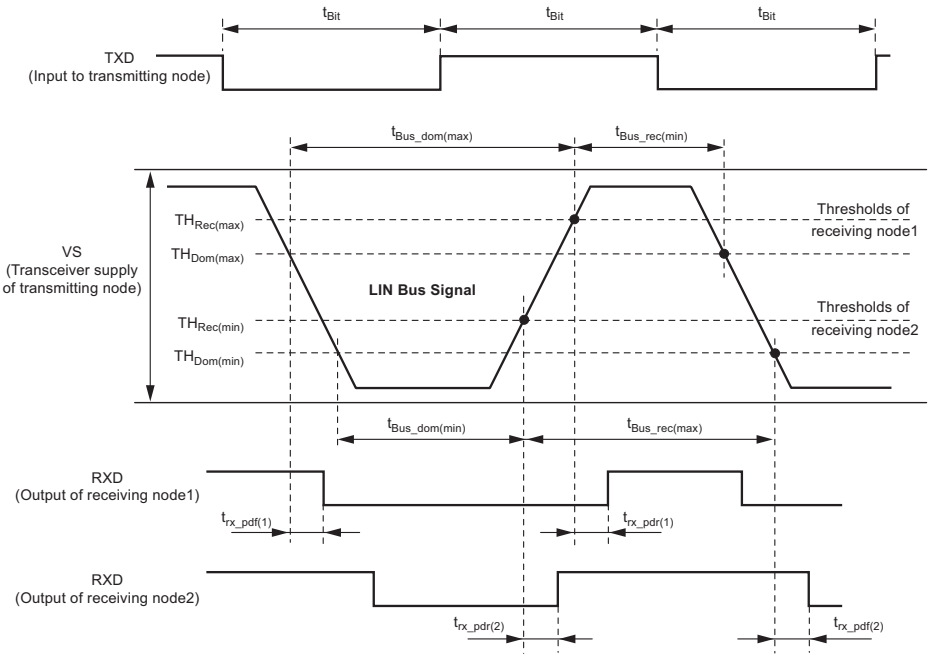
No.	Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
12.6	Time Delay for Mode Change from Silent Mode into Normal Mode via EN Pin	t_{s_n}	5	15	40	µs	V_{EN} = 5V/3.3V
12.7	Duty Cycle 1	D1	0.396	—	—	—	$TH_{Rec(max)}$ = 0.744 * V_{VS} $TH_{Dom(max)}$ = 0.581 * V_{VS} V_{VS} = 7.0V to 18V t_{Bit} = 50 µs D1 = $t_{bus\_rec(min)}$/(2 * t_{Bit})
12.8	Duty Cycle 2	D2	—	—	0.581	—	$TH_{Rec(min)}$ = 0.422 * V_{VS} $TH_{Dom(min)}$ = 0.284 * V_{VS} V_{VS} = 7.6V to 18V t_{Bit} = 50 µs D2 = $t_{bus\_rec(max)}$/(2 * t_{Bit})
12.9	Duty Cycle 3	D3	0.417	—	—	—	$TH_{Rec(max)}$ = 0.778 * V_{VS} $TH_{Dom(max)}$ = 0.616 * V_{VS} V_{VS} = 7.0V to 18V t_{Bit} = 96 µs D3 = $t_{bus\_rec(min)}$/(2 * t_{Bit})
12.10	Duty Cycle 4	D4	—	—	0.590	—	$T_{HRec(min)}$ = 0.389 * V_{VS} $T_{HDom(min)}$ = 0.251 * V_{VS} V_{VS} = 7.6V to 18V t_{Bit} = 96 µs D4 = $t_{bus\_rec(max)}$/(2 * t_{Bit})
12.11	Slope Time Falling and Rising Edge at LIN	t_{SLOPE_fall} t_{SLOPE_rise}	3.5	—	22.5	µs	V_{VS} = 7.0V to 18V
13	**Receiver Electrical AC Parameters of the LIN Physical Layer LIN Receiver, RXD Load Conditions: C_{RXD} = 20 pF**						
13.1	Propagation Delay of Receiver	t_{rx_pd}	—	—	6	µs	V_{VS} = 7.0V to 18V t_{rx_pd} = max$_{(trx_pdr, t_{rx_pdf})}$
13.2	Symmetry of Receiver Propagation Delay Rising Edge Minus Falling Edge	t_{rx_sym}	–2	—	+2	µs	V_{VS} = 7.0V to 18V t_{rx_sym} = t_{rx_pdr} – t_{rx_pdf}

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

FIGURE 2-1: DEFINITION OF BUS TIMING CHARACTERISTICS



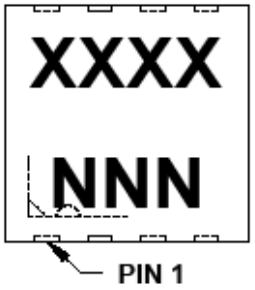
TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Thermal Resistance Virtual Junction to Exposed Thermal Pad	R_{thvJC}	—	+10	—	K/W	
Thermal Resistance Virtual Junction to Ambient, where Exposed Thermal Pad is Soldered to PCB According to JEDEC	R_{thvJA}	—	+50	—	K/W	
Thermal Shutdown of VCC Regulator	T_{VCCoff}	+150	+165	+180	°C	
Thermal Shutdown of LIN Output	T_{LINoff}	+150	+165	+180	°C	
Thermal Shutdown Hysteresis	T_{hys}	—	+10	—	°C	

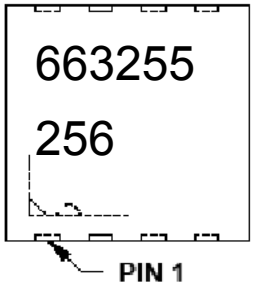
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

8-Lead 3 x 3 mm VDFN



Example

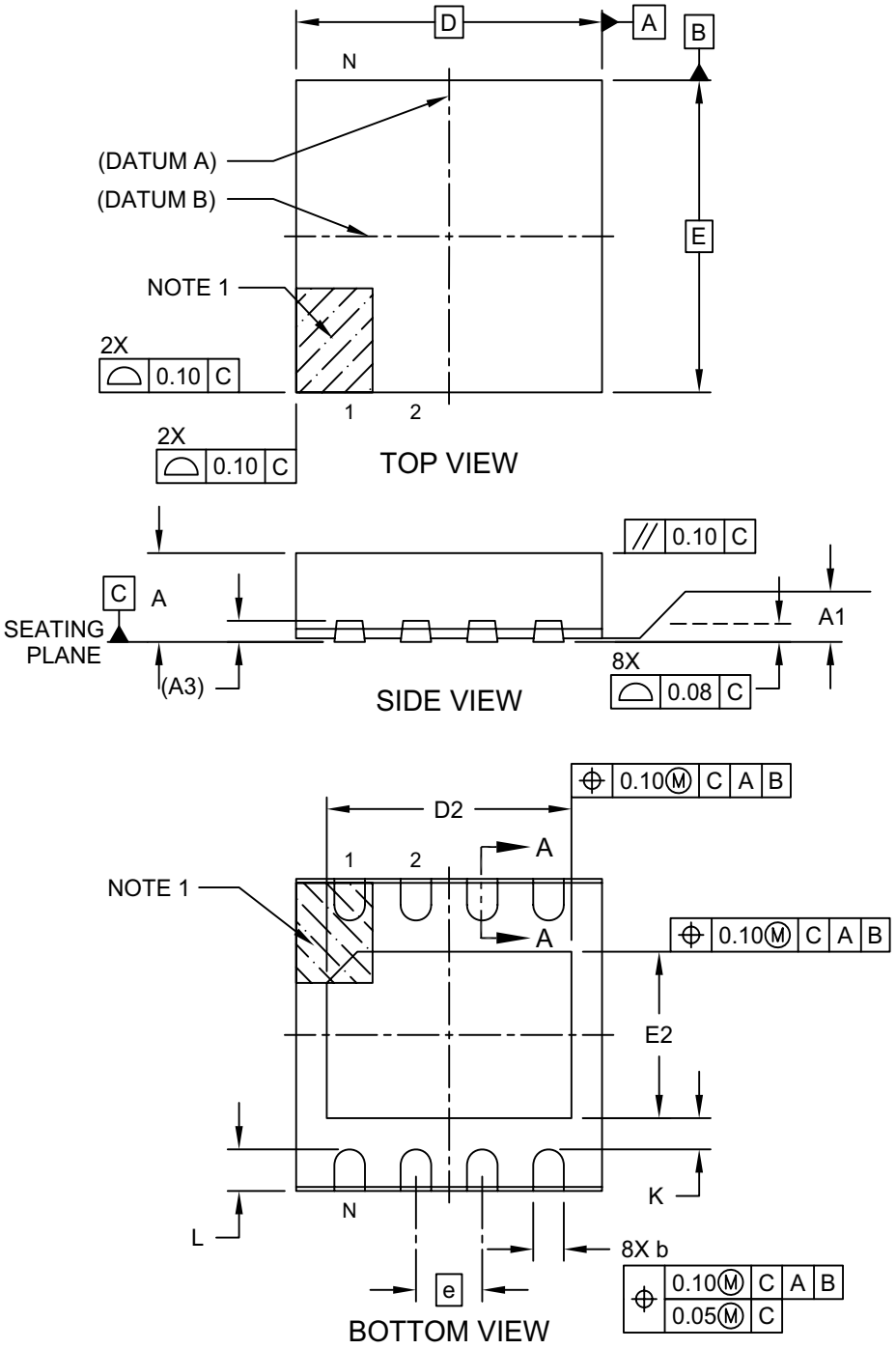


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN]
With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

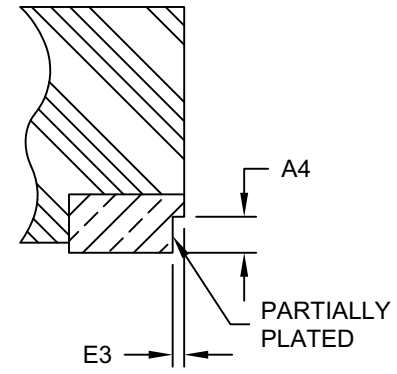
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



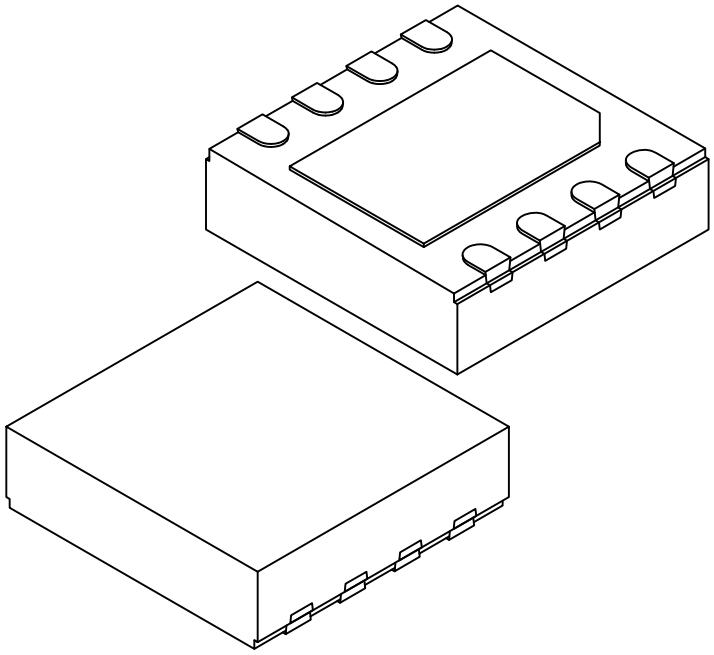
Microchip Technology Drawing C04-21358 Rev B Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A–A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.03	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.30	2.40	2.50
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Depth	A4	0.10	0.13	0.15
Wettable Flank Step Cut Width	E3	-	-	0.04

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

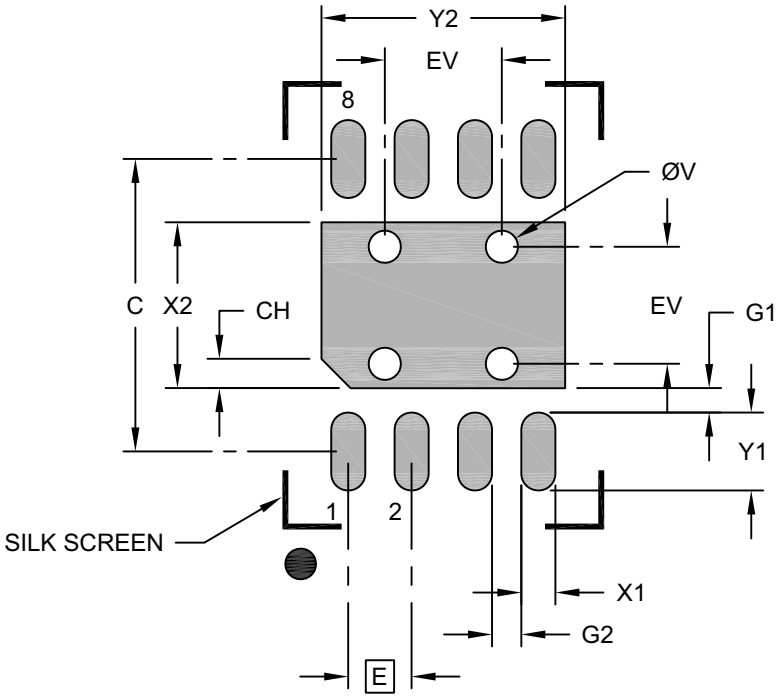
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21358 Rev B Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			1.70
Optional Center Pad Length	Y2			2.50
Contact Pad Spacing	C		3.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Contact Pad to Contact Pad (X6)	G2	0.20		
Pin 1 Index Chamfer	CH	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23358 Rev B

APPENDIX A: REVISION HISTORY

Revision A (October 2017)

- Original Release of this Document.
- Updated the Typical Application Circuit.
- Minor text changes throughout.
- This document replaces Atmel - 9231A-AUTO-08/15.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	[X](1)	X
Device	Package	Tape and Reel Option	Package Directives Classification

Device:	ATA663232:		LIN System Basis Chip Including LIN Transceiver, 3.3V Voltage Regulator and Wake-Input
	ATA663255:		LIN System Basis Chip Including LIN Transceiver, 5V Voltage Regulator and Wake-Input
Package:	GB	=	8-Lead VDFN
Tape and Reel Option:	Q	=	330 mm diameter Tape and Reel
Package Directives Classification:	W	=	Package according to RoHS(2)

Examples:

a) ATA663232-GBQW: ATA663232, 8-Lead VDFN, Tape and Reel, Package according to RoHS

b) ATA663255-GBQW: ATA663255, 8-Lead VDFN, Tape and Reel, Package according to RoHS

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: RoHS compliant, Maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (Cl) and less than 0.15% (1500 ppm) total Bromine (Br) and Chlorine (Cl) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material.

NOTES:

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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