

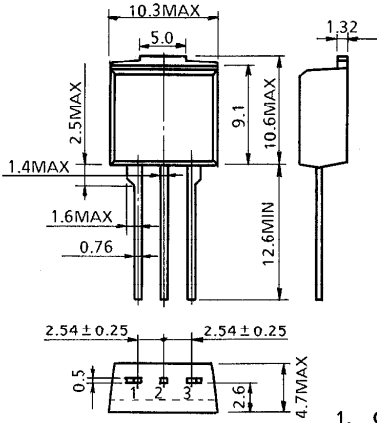
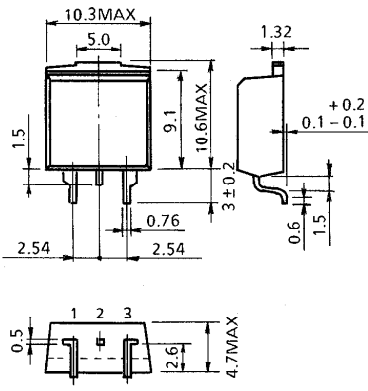
TOSHIBA THYRISTOR SILICON PLANAR TYPE

SF5G48, SF5J48, USF5G48, USF5J48

MEDIUM POWER CONTROL APPLICATIONS.

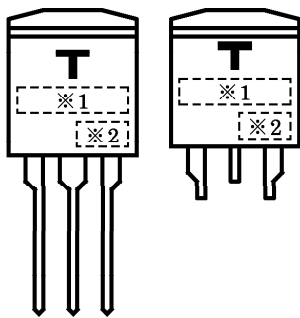
- Repetitive Peak Off-State Voltage : V_{DRM}
 - Repetitive Peak Reverse Voltage : V_{RRM}
 - Average On-State Current : $I_{T(AV)}=5A$
 - Gate Trigger Current : $I_{GT}=10mA$ Max.
- $\left. \begin{matrix} V_{DRM} \\ V_{RRM} \end{matrix} \right\} = 400, 600V$

Unit in mm

SF5G48-SF5J48	USF5G48-USF5J48
	
JEDEC —	JEDEC —
EIAJ —	EIAJ —
TOSHIBA 13-10J1B	TOSHIBA 13-10J2B

Weight : 1.7g

MARK



※ 1	MARK	F5G48	TYPE	SF5G48, USF5G48
		F5J48	NAME	SF5J48, USF5J48
※ 2	Lot Number			
	□ □ ← Month (Starting from Alphabet A) ← Year (Last Number of the Christian Era)			

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● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

MAXIMUM RATINGS

CHARACTERISTIC		SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage and Repetitive Peak Reverse Voltage	SF5G48	V_{DRM}	400	V
	USF5G48			
	SF5J48	V_{RRM}	600	
	USF5J48			
Non-Repetitive Peak Reverse Voltage (Non-Repetitive < 5ms $T_j = 0 \sim 125^\circ\text{C}$)	SF5G48	V_{RSM}	500	V
	USF5G48			
	SF5J48		720	
	USF5J48			
Average On-State Current		$I_{\text{T(AV)}}$	5	A
R.M.S On-State Current		$I_{\text{T(RMS)}}$	7.8	A
Peak One Cycle Surge On-State Current (Non-Repetitive)		I_{TSM}	80 (50Hz)	A
			88 (60Hz)	
I^2t Limit Value ($t = 1 \sim 10\text{ms}$)		I^2t	32	A^2s
Critical Rate of Rise of On-State Current (Note 1)		di/dt	100	$\text{A} / \mu\text{s}$
Peak Gate Power Dissipation		P_{GM}	5	W
Average Gate Power Dissipation		$P_{\text{G(AV)}}$	0.5	W
Peak Forward Gate Voltage		V_{FGM}	10	V
Peak Reverse Gate Voltage		V_{RGM}	-5	V
Peak Forward Gate Current		I_{GM}	2	A
Junction Temperature		T_j	$-40 \sim 125$	$^\circ\text{C}$
Storage Temperature Range		T_{stg}	$-40 \sim 125$	$^\circ\text{C}$

(Note1) $V_{\text{DRM}} = 0.5 \times \text{Rated}$
 $I_{\text{TM}} \leq 15\text{A}$
 $T_{\text{gw}} \geq 10\mu\text{s}$
 $T_{\text{gr}} \leq 250\text{ns}$
 $i_{\text{gp}} = I_{\text{GT}} \times 2.0$

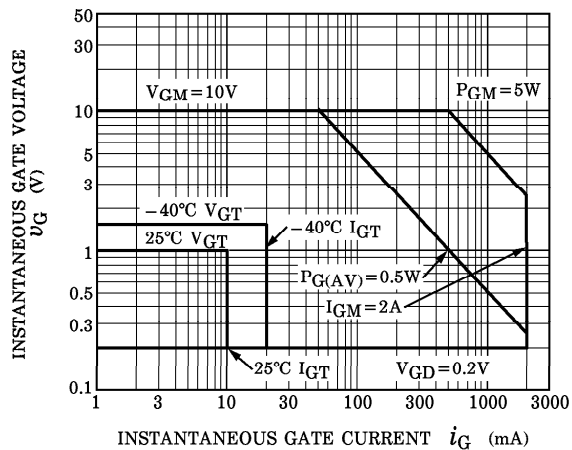
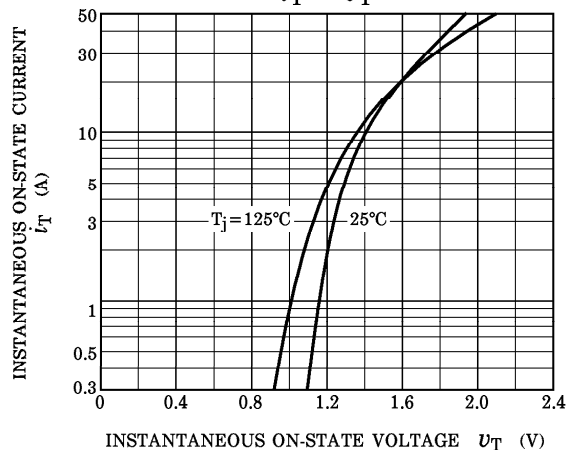
ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Repetitive Peak Off-State Current and Repetitive Peak Reverse	I_{DRM} I_{RRM}	$V_{\text{DRM}} = V_{\text{RRM}} = \text{Rated}$	—	—	10	μA
Peak On-State Voltage	V_{TM}	$I_{\text{TM}} = 15\text{A}$	—	—	1.5	V
Gate Trigger Voltage	V_{GT}	$V_{\text{D}} = 6\text{V}, R_{\text{L}} = 10\Omega$	—	—	1.0	V
Gate Trigger Current	I_{GT}		—	—	10	mA
Gate Non-Trigger Voltage	V_{GD}	$V_{\text{D}} = \text{Rated} \times 2/3, T_c = 125^\circ\text{C}$	0.2	—	—	V
Critical Rate of Rise of Off-State Voltage	dv/dt	$V_{\text{DRM}} = \text{Rated}, T_c = 125^\circ\text{C}$ Exponential Rise	—	50	—	$\text{V} / \mu\text{s}$
Holding Current	I_{H}	$V_{\text{D}} = 6\text{V}, I_{\text{TM}} = 1\text{A}$	—	—	40	mA
Latching Current	I_{L}	$V_{\text{D}} = 6\text{V}, f = 50\text{Hz}$ $t_{\text{gw}} = 50\mu\text{s}, i_{\text{G}} = 30\text{mA}$	—	—	50	mA
Thermal Resistance	$R_{\text{th(j-c)}}$	Junction to Case, DC	—	—	3.2	$^\circ\text{C} / \text{W}$

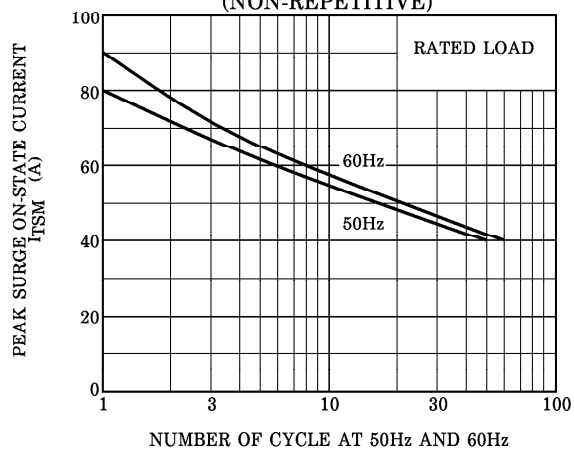
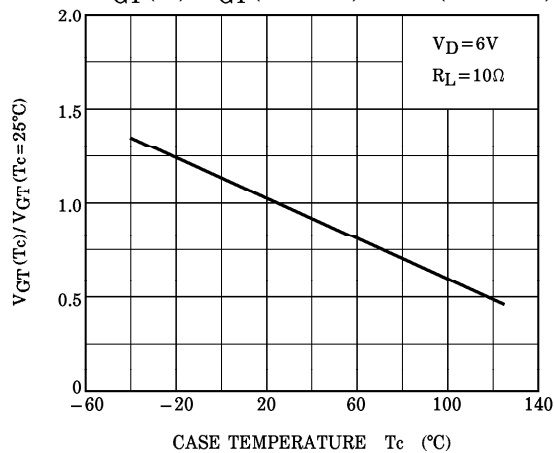
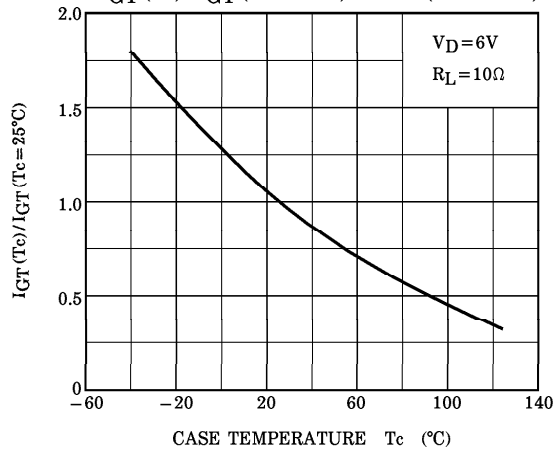
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GATE TRIGGER CHARACTERISTIC

 $i_T - v_T$ 

SURGE ON-STATE CURRENT (NON-REPETITIVE)

 $V_{GT}(T_c) / V_{GT}(T_c = 25^\circ C) - T_c$ (TYPICAL) $I_{GT}(T_c) / I_{GT}(T_c = 25^\circ C) - T_c$ (TYPICAL) $I_H(T_c) / I_H(T_c = 25^\circ C) - T_c$ (TYPICAL)