

# Dual Matched 40 V, 6.0 A, Low $V_{CE(sat)}$ PNP Transistor

## NSS40300MDR2G, NSV40300MDR2G

These transistors are part of the **onsemi** e<sup>2</sup>PowerEdge family of Low  $V_{CE(sat)}$  transistors. They are assembled to create a pair of devices highly matched in all parameters, including ultra low saturation voltage  $V_{CE(sat)}$ , high current gain and Base/Emitter turn on voltage.

Typical applications are current mirrors, differential amplifiers, DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e<sup>2</sup>PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

### Features

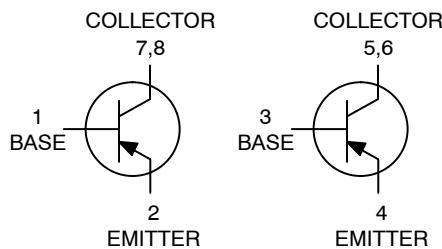
- Current Gain Matching to 10%
- Base Emitter Voltage Matched to 2 mV
- AEC-Q101 Qualified and PPAP Capable
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These are Pb-Free Devices\*

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

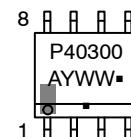
| Rating                         | Symbol    | Max                        | Unit |
|--------------------------------|-----------|----------------------------|------|
| Collector-Emitter Voltage      | $V_{CEO}$ | -40                        | Vdc  |
| Collector-Base Voltage         | $V_{CBO}$ | -40                        | Vdc  |
| Emitter-Base Voltage           | $V_{EBO}$ | -7.0                       | Vdc  |
| Collector Current – Continuous | $I_C$     | -3.0                       | A    |
| Collector Current – Peak       | $I_{CM}$  | -6.0                       | A    |
| Electrostatic Discharge        | ESD       | HBM Class 3B<br>MM Class C |      |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**40 VOLTS  
6.0 AMPS  
PNP LOW  $V_{CE(sat)}$  TRANSISTOR  
EQUIVALENT  $R_{DS(on)}$  80 m $\Omega$**



### MARKING DIAGRAM



P40300 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

| Device        | Package             | Shipping <sup>†</sup>  |
|---------------|---------------------|------------------------|
| NSS40300MDR2G | SOIC-8<br>(Pb-Free) | 2,500 /<br>Tape & Reel |
| NSV40300MDR2G | SOIC-8<br>(Pb-Free) | 2,500 /<br>Tape & Reel |

<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

\* For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, [SOLDERRM/D](#).

# NSS40300MDR2G, NSV40300MDR2G

## THERMAL CHARACTERISTICS

| Characteristic  | Symbol                | Max         | Unit        |
|---|-----------------------|-------------|-------------|
| <b>SINGLE HEATED</b>  |                       |             |             |
| Total Device Dissipation (Note 1)<br>$T_A = 25^\circ\text{C}$<br>Derate above 25 °C | $P_D$                 | 576<br>4.6  | mW<br>mW/°C |
| Thermal Resistance<br>Junction-to-Ambient (Note 1)                                  | $R_{\theta,JA}$       | 217         | °C/W        |
| Total Device Dissipation (Note 2)<br>$T_A = 25^\circ\text{C}$<br>Derate above 25 °C | $P_D$                 | 676<br>5.4  | mW<br>mW/°C |
| Thermal Resistance<br>Junction-to-Ambient (Note 2)                                  | $R_{\theta,JA}$       | 185         | °C/W        |
| <b>DUAL HEATED (Note 3)</b>   |                       |             |             |
| Total Device Dissipation (Note 1)<br>$T_A = 25^\circ\text{C}$<br>Derate above 25 °C | $P_D$                 | 653<br>5.2  | mW<br>mW/°C |
| Thermal Resistance<br>Junction-to-Ambient (Note 1)                                  | $R_{\theta,JA}$       | 191         | °C/W        |
| Total Device Dissipation (Note 2)<br>$T_A = 25^\circ\text{C}$<br>Derate above 25 °C | $P_D$                 | 783<br>6.3  | mW<br>mW/°C |
| Thermal Resistance<br>Junction-to-Ambient (Note 2)                                  | $R_{\theta,JA}$       | 160         | °C/W        |
| Junction and Storage Temperature Range  | $T_J, T_{\text{stg}}$ | -55 to +150 | °C          |

1. FR-4 @ 10 mm<sup>2</sup>, 1 oz. copper traces, still air.

2. FR-4 @ 100 mm<sup>2</sup>, 1 oz. copper traces, still air.

3. Dual heated values assume total power is the sum of two equally powered devices.

# NSS40300MDR2G, NSV40300MDR2G

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C unless otherwise noted)

| Characteristic  | Symbol   | Min                             | Typ                                  | Max                                  | Unit             |
|---|--|---------------------------------|--------------------------------------|--------------------------------------|------------------|
| <b>OFF CHARACTERISTICS</b>  |  |                                 |                                      |                                      |                  |
| Collector-Emitter Breakdown Voltage<br>(I <sub>C</sub> = -10 mA <sub>dc</sub> , I <sub>B</sub> = 0)   | V <sub>(BR)CEO</sub>                               | -40                             | -                                    | -                                    | V <sub>dc</sub>  |
| Collector-Base Breakdown Voltage<br>(I <sub>C</sub> = -0.1 mA <sub>dc</sub> , I <sub>E</sub> = 0)   | V <sub>(BR)CBO</sub>                               | -40                             | -                                    | -                                    | V <sub>dc</sub>  |
| Emitter-Base Breakdown Voltage<br>(I <sub>E</sub> = -0.1 mA <sub>dc</sub> , I <sub>C</sub> = 0)   | V <sub>(BR)EBO</sub>                               | -7.0                            | -                                    | -                                    | V <sub>dc</sub>  |
| Collector Cutoff Current<br>(V <sub>CB</sub> = -40 V <sub>dc</sub> , I <sub>E</sub> = 0)  | I <sub>CBO</sub>                                   | -                               | -                                    | -0.1                                 | μA <sub>dc</sub> |
| Emitter Cutoff Current<br>(V <sub>EB</sub> = -6.0 V <sub>dc</sub> )   | I <sub>EBO</sub>                                   | -                               | -                                    | -0.1                                 | μA <sub>dc</sub> |
| <b>ON CHARACTERISTICS</b>   |  |                                 |                                      |                                      |                  |
| DC Current Gain (Note 4)<br>(I <sub>C</sub> = -10 mA, V <sub>CE</sub> = -2.0 V)<br>(I <sub>C</sub> = -500 mA, V <sub>CE</sub> = -2.0 V)<br>(I <sub>C</sub> = -1.0 A, V <sub>CE</sub> = -2.0 V)<br>(I <sub>C</sub> = -2.0 A, V <sub>CE</sub> = -2.0 V)<br>(I <sub>C</sub> = -2.0 A, V <sub>CE</sub> = -2.0 V) (Note 5) | $h_{FE}$<br><br>$h_{FE(1)}/h_{FE(2)}$              | 250<br>220<br>180<br>150<br>0.9 | 380<br>340<br>300<br>230<br>0.99     | -                                    | -                |
| Collector-Emitter Saturation Voltage (Note 4)<br>(I <sub>C</sub> = -0.1 A, I <sub>B</sub> = -0.010 A)<br>(I <sub>C</sub> = -1.0 A, I <sub>B</sub> = -0.100 A)<br>(I <sub>C</sub> = -1.0 A, I <sub>B</sub> = -0.010 A)<br>(I <sub>C</sub> = -2.0 A, I <sub>B</sub> = -0.200 A)   | V <sub>CE(sat)</sub>                               | -<br>-<br>-<br>-                | -0.013<br>-0.075<br>-0.130<br>-0.135 | -0.017<br>-0.095<br>-0.170<br>-0.170 | V                |
| Base-Emitter Saturation Voltage (Note 4)<br>(I <sub>C</sub> = -1.0 A, I <sub>B</sub> = -0.01 A)   | V <sub>BE(sat)</sub>                               | -                               | -0.780                               | -0.900                               | V                |
| Base-Emitter Turn-on Voltage (Note 4)<br>(I <sub>C</sub> = -0.1 A, V <sub>CE</sub> = -2.0 V)<br>(I <sub>C</sub> = -0.1 A, V <sub>CE</sub> = -2.0 V) (Note 6)  | V <sub>BE(on)</sub><br><br>$V_{BE(1)} - V_{BE(2)}$ | -<br>-<br>-<br>-                | -0.660<br>0.3                        | -0.750<br>2.0                        | V<br>mV          |
| Cutoff Frequency<br>(I <sub>C</sub> = -100 mA, V <sub>CE</sub> = -5.0 V, f = 100 MHz)   | f <sub>T</sub>                                     | 100                             | -                                    | -                                    | MHz              |
| Input Capacitance (V <sub>EB</sub> = -0.5 V, f = 1.0 MHz)   | C <sub>ibo</sub>                                   | -                               | 250                                  | 300                                  | pF               |
| Output Capacitance (V <sub>CB</sub> = -3.0 V, f = 1.0 MHz)  | C <sub>obo</sub>                                   | -                               | 50                                   | 65                                   | pF               |

## SWITCHING CHARACTERISTICS

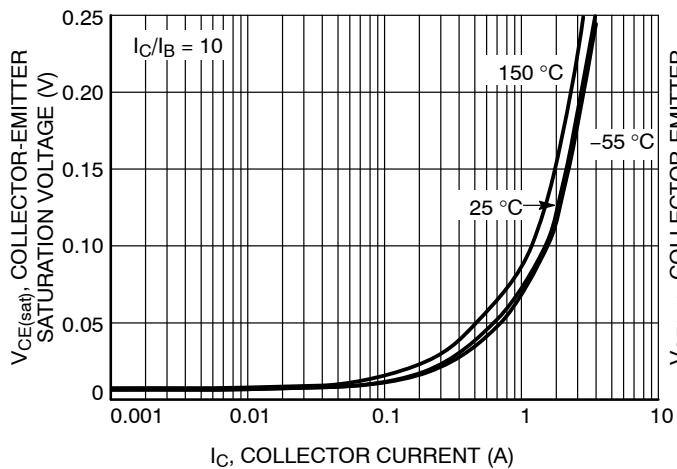
|   |                |   |   |     |    |
|---|----------------|---|---|-----|----|
| Delay (V <sub>CC</sub> = -30 V, I <sub>C</sub> = -750 mA, I <sub>B1</sub> = -15 mA)   | t <sub>d</sub> | - | - | 60  | ns |
| Rise (V <sub>CC</sub> = -30 V, I <sub>C</sub> = -750 mA, I <sub>B1</sub> = -15 mA)    | t <sub>r</sub> | - | - | 120 | ns |
| Storage (V <sub>CC</sub> = -30 V, I <sub>C</sub> = -750 mA, I <sub>B1</sub> = -15 mA) | t <sub>s</sub> | - | - | 400 | ns |
| Fall (V <sub>CC</sub> = -30 V, I <sub>C</sub> = -750 mA, I <sub>B1</sub> = -15 mA)    | t <sub>f</sub> | - | - | 130 | ns |

4. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%.

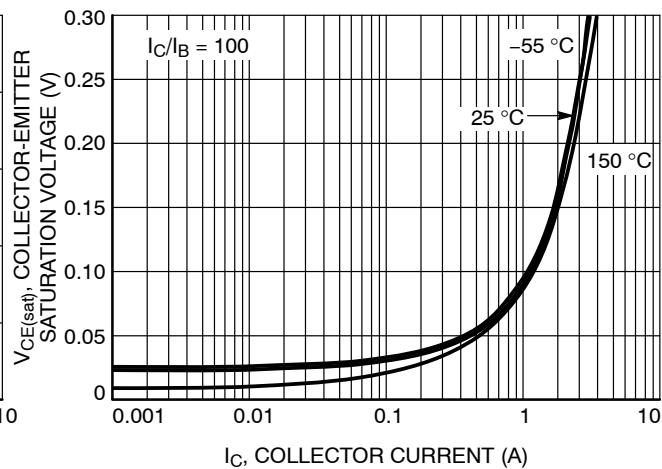
5.  $h_{FE(1)}/h_{FE(2)}$  is the ratio of one transistor compared to the other transistor within the same package. The smaller  $h_{FE}$  is used as numerator.

6.  $V_{BE(1)} - V_{BE(2)}$  is the absolute difference of one transistor compared to the other transistor within the same package.

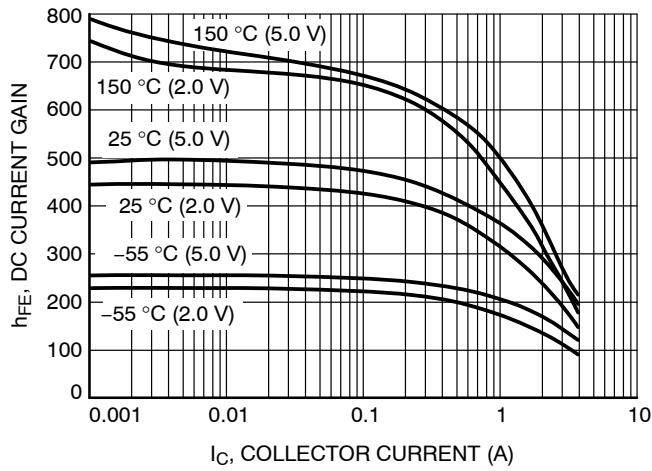
**TYPICAL CHARACTERISTICS**



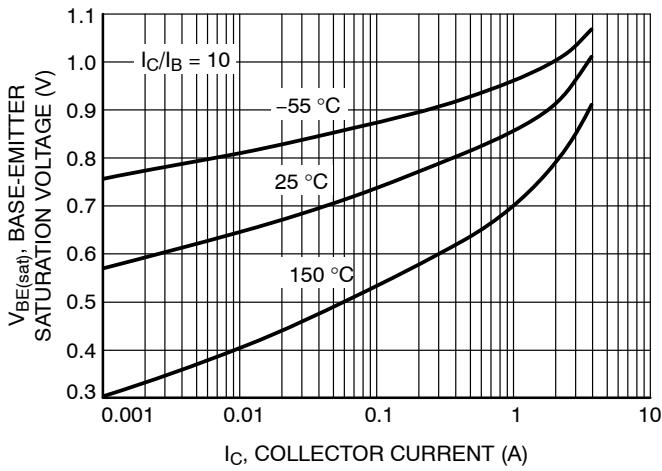
**Figure 1. Collector Emitter Saturation Voltage vs. Collector Current**



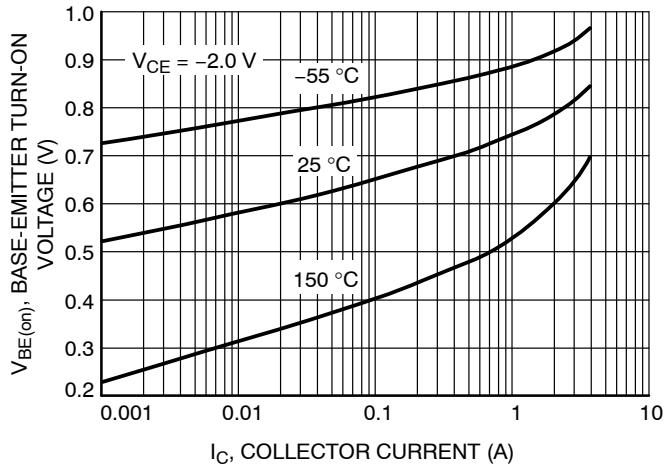
**Figure 2. Collector Emitter Saturation Voltage vs. Collector Current**



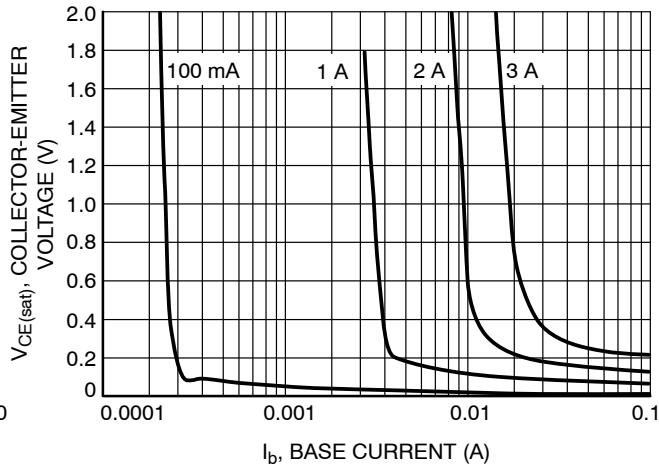
**Figure 3. DC Current Gain vs. Collector Current**



**Figure 4. Base Emitter Saturation Voltage vs. Collector Current**

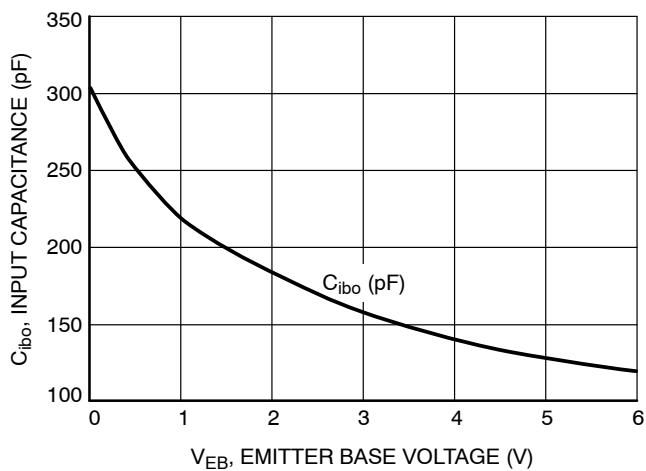


**Figure 5. Base Emitter Turn-On Voltage vs. Collector Current**

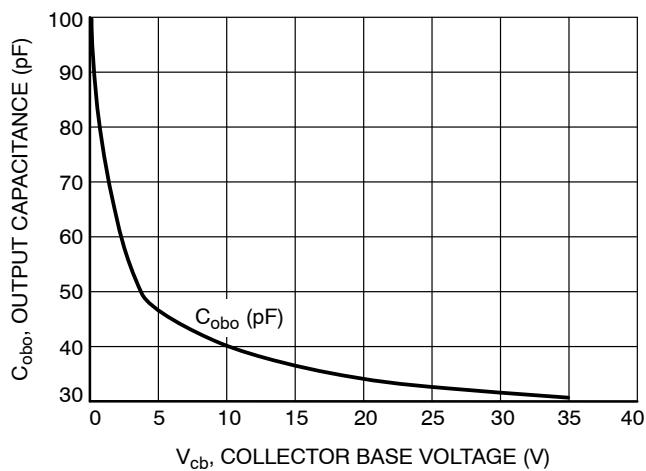


**Figure 6. Saturation Region**

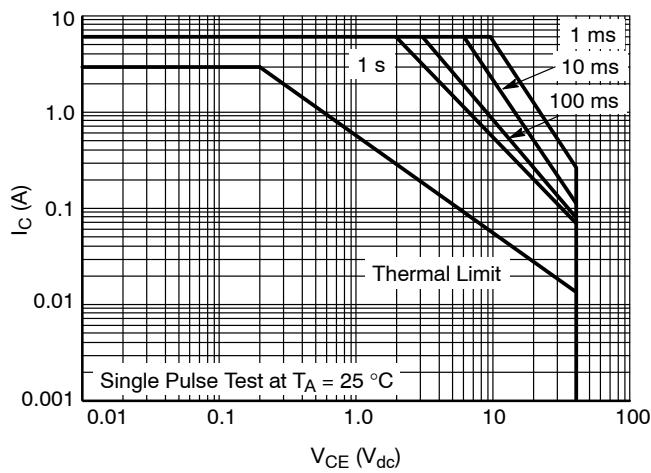
**TYPICAL CHARACTERISTICS**



**Figure 7. Input Capacitance**



**Figure 8. Output Capacitance**



**Figure 9. Safe Operating Area**

# **NSS40300MDR2G, NSV40300MDR2G**

## **REVISION HISTORY**

| <b>Revision</b> | <b>Description of Changes</b>                     | <b>Date</b> |
|-----------------|---|-------------|
| 3               | Rebranded the Data Sheet to <b>onsemi</b> format. | 11/6/2025   |

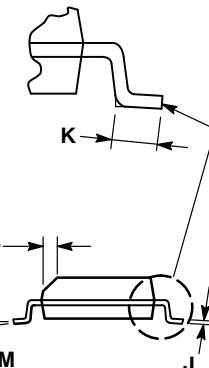
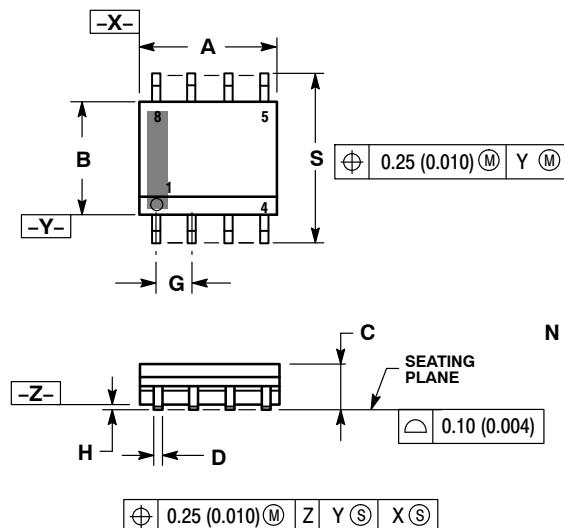
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011

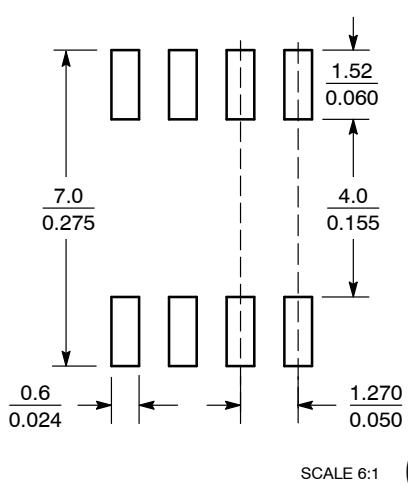


## NOTES:

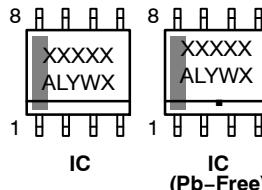
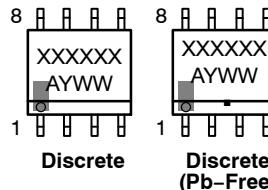
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0 °         | 8 °  | 0 °       | 8 °   |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

## SOLDERING FOOTPRINT\*



SCALE 6:1 (mm/inches)

GENERIC  
MARKING DIAGRAM\*

XXXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

|                  |             |   |
|------------------|-------------|---|
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| DESCRIPTION:     | SOIC-8 NB   | PAGE 1 OF 2   |

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

|  |   |   |   |
|--|---|---|---|
| STYLE 1:<br>PIN 1. Emitter<br>2. Collector<br>3. Collector<br>4. Emitter<br>5. Emitter<br>6. Base<br>7. Base<br>8. Emitter   | STYLE 2:<br>PIN 1. Collector, Die, #1<br>2. Collector, #1<br>3. Collector, #2<br>4. Collector, #2<br>5. Base, #2<br>6. Emitter, #2<br>7. Base, #1<br>8. Emitter, #1               | STYLE 3:<br>PIN 1. Drain, Die #1<br>2. Drain, #1<br>3. Drain, #2<br>4. Drain, #2<br>5. Gate, #2<br>6. Source, #2<br>7. Gate, #1<br>8. Source, #1                            | STYLE 4:<br>PIN 1. Anode<br>2. Anode<br>3. Anode<br>4. Anode<br>5. Anode<br>6. Anode<br>7. Anode<br>8. Common Cathode   |
| STYLE 5:<br>PIN 1. Drain<br>2. Drain<br>3. Drain<br>4. Drain<br>5. Gate<br>6. Gate<br>7. Source<br>8. Source   | STYLE 6:<br>PIN 1. Source<br>2. Drain<br>3. Drain<br>4. Source<br>5. Source<br>6. Gate<br>7. Gate<br>8. Source  | STYLE 7:<br>PIN 1. Input<br>2. External Bypass<br>3. Third Stage Source<br>4. Ground<br>5. Drain<br>6. Gate 3<br>7. Second Stage Vd<br>8. First Stage Vd                    | STYLE 8:<br>PIN 1. Collector, Die #1<br>2. Base, #1<br>3. Base, #2<br>4. Collector, #2<br>5. Collector, #2<br>6. Emitter, #2<br>7. Emitter, #1<br>8. Collector, #1                              |
| STYLE 9:<br>PIN 1. Emitter, Common<br>2. Collector, Die #1<br>3. Collector, Die #2<br>4. Emitter, Common<br>5. Emitter, Common<br>6. Base, Die #2<br>7. Base, Die #1<br>8. Emitter, Common | STYLE 10:<br>PIN 1. Ground<br>2. Bias 1<br>3. Output<br>4. Ground<br>5. Ground<br>6. Bias 2<br>7. Input<br>8. Ground  | STYLE 11:<br>PIN 1. Source 1<br>2. Gate 1<br>3. Source 2<br>4. Gate 2<br>5. Drain 2<br>6. Drain 2<br>7. Drain 1<br>8. Drain 1   | STYLE 12:<br>PIN 1. Source<br>2. Source<br>3. Source<br>4. Gate<br>5. Drain<br>6. Drain<br>7. Drain<br>8. Drain   |
| STYLE 13:<br>PIN 1. N.C.<br>2. Source<br>3. Source<br>4. Gate<br>5. Drain<br>6. Drain<br>7. Drain<br>8. Drain  | STYLE 14:<br>PIN 1. N-Source<br>2. N-Gate<br>3. P-Source<br>4. P-Gate<br>5. P-Drain<br>6. P-Drain<br>7. N-Drain<br>8. N-Drain   | STYLE 15:<br>PIN 1. Anode 1<br>2. Anode 1<br>3. Anode 1<br>4. Anode 1<br>5. Cathode, Common<br>6. Cathode, Common<br>7. Cathode, Common<br>8. Cathode, Common               | STYLE 16:<br>PIN 1. Emitter, Die #1<br>2. Base, Die #1<br>3. Emitter, Die #2<br>4. Base, Die #2<br>5. Collector, Die #2<br>6. Collector, Die #2<br>7. Collector, Die #1<br>8. Collector, Die #1 |
| STYLE 17:<br>PIN 1. VCC<br>2. V2OUT<br>3. V1OUT<br>4. TXE<br>5. RXE<br>6. VEE<br>7. GND<br>8. ACC  | STYLE 18:<br>PIN 1. Anode<br>2. Anode<br>3. Source<br>4. Gate<br>5. Drain<br>6. Drain<br>7. Cathode<br>8. Cathode   | STYLE 19:<br>PIN 1. Source 1<br>2. Gate 1<br>3. Source 2<br>4. Gate 2<br>5. Drain 2<br>6. Mirror 2<br>7. Drain 1<br>8. Mirror 1   | STYLE 20:<br>PIN 1. Source (N)<br>2. Gate (N)<br>3. Source (P)<br>4. Gate (P)<br>5. Drain<br>6. Drain<br>7. Drain<br>8. Drain   |
| STYLE 21:<br>PIN 1. Cathode 1<br>2. Cathode 2<br>3. Cathode 3<br>4. Cathode 4<br>5. Cathode 5<br>6. Common Anode<br>7. Common Anode<br>8. Cathode 6  | STYLE 22:<br>PIN 1. I/O Line 1<br>2. Common Cathode/VCC<br>3. Common Cathode/VCC<br>4. I/O Line 3<br>5. Common Anode/GND<br>6. I/O Line 4<br>7. I/O Line 5<br>8. Common Anode/GND | STYLE 23:<br>PIN 1. Line 1 IN<br>2. Common Anode/GND<br>3. Common Anode/GND<br>4. Line 2 IN<br>5. Line 2 OUT<br>6. Common Anode/GND<br>7. Common Anode/GND<br>8. Line 1 OUT | STYLE 24:<br>PIN 1. Base<br>2. Emitter<br>3. Collector/Anode<br>4. Collector/Anode<br>5. Cathode<br>6. Cathode<br>7. Collector/Anode<br>8. Collector/Anode                                      |
| STYLE 25:<br>PIN 1. VIN<br>2. N/C<br>3. REXT<br>4. GND<br>5. IOUT<br>6. IOUT<br>7. IOUT<br>8. IOUT   | STYLE 26:<br>PIN 1. GND<br>2. dv/dt<br>3. Enable<br>4. ILIMIT<br>5. Source<br>6. Source<br>7. Source<br>8. VCC  | STYLE 27:<br>PIN 1. ILIMIT<br>2. OVLO<br>3. UVLO<br>4. INPUT+<br>5. Source<br>6. Source<br>7. Source<br>8. Drain  | STYLE 28:<br>PIN 1. SW_TO_GND<br>2. DASIC_OFF<br>3. DASIC_SW_DET<br>4. GND<br>5. V_MON<br>6. VBUCK<br>7. VBUCK<br>8. VIN  |
| STYLE 29:<br>PIN 1. Base, Die #1<br>2. Emitter, #1<br>3. Base, #2<br>4. Emitter, #2<br>5. Collector, #2<br>6. Collector, #2<br>7. Collector, #1<br>8. Collector, #1                        | STYLE 30:<br>PIN 1. Drain 1<br>2. Drain 1<br>3. Gate 2<br>4. Source 2<br>5. Source 1/Drain 2<br>6. Source 1/Drain 2<br>7. Source 1/Drain 2<br>8. Gate 1                           |   |   |

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