

Dual Matched 40 V, 6.0 A, Low $V_{CE(sat)}$ PNP Transistor

NSS40300MDR2G, NSV40300MDR2G

These transistors are part of the **onsemi** e²PowerEdge family of Low $V_{CE(sat)}$ transistors. They are assembled to create a pair of devices highly matched in all parameters, including ultra low saturation voltage $V_{CE(sat)}$, high current gain and Base/Emitter turn on voltage.

Typical applications are current mirrors, differential amplifiers, DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e²PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- Current Gain Matching to 10%
- Base Emitter Voltage Matched to 2 mV
- AEC-Q101 Qualified and PPAP Capable
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These are Pb-Free Devices*

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	-40	Vdc
Collector-Base Voltage	V_{CBO}	-40	Vdc
Emitter-Base Voltage	V_{EBO}	-7.0	Vdc
Collector Current – Continuous	I_C	-3.0	A
Collector Current – Peak	I_{CM}	-6.0	A
Electrostatic Discharge	ESD	HBM Class 3B MM Class C	

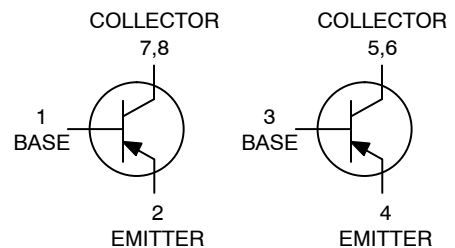
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

* For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, [SOLDDRM/D](#).

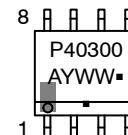
40 VOLTS
6.0 AMPS
PNP LOW $V_{CE(sat)}$ TRANSISTOR
EQUIVALENT $R_{DS(on)}$ 80 m Ω



SOIC-8
CASE 751
STYLE 29



MARKING DIAGRAM



P40300 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NSS40300MDR2G	SOIC-8 (Pb-Free)	2,500 / Tape & Reel
NSV40300MDR2G	SOIC-8 (Pb-Free)	2,500 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
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SINGLE HEATED

Total Device Dissipation (Note 1) $T_A = 25\text{ }^{\circ}\text{C}$ Derate above $25\text{ }^{\circ}\text{C}$	P_D	576 4.6	mW mW/ $^{\circ}\text{C}$
Thermal Resistance Junction-to-Ambient (Note 1)	$R_{\theta JA}$	217	$^{\circ}\text{C/W}$
Total Device Dissipation (Note 2) $T_A = 25\text{ }^{\circ}\text{C}$ Derate above $25\text{ }^{\circ}\text{C}$	P_D	676 5.4	mW mW/ $^{\circ}\text{C}$
Thermal Resistance Junction-to-Ambient (Note 2)	$R_{\theta JA}$	185	$^{\circ}\text{C/W}$

DUAL HEATED (Note 3)

Total Device Dissipation (Note 1) $T_A = 25\text{ }^{\circ}\text{C}$ Derate above $25\text{ }^{\circ}\text{C}$	P_D	653 5.2	mW mW/ $^{\circ}\text{C}$
Thermal Resistance Junction-to-Ambient (Note 1)	$R_{\theta JA}$	191	$^{\circ}\text{C/W}$
Total Device Dissipation (Note 2) $T_A = 25\text{ }^{\circ}\text{C}$ Derate above $25\text{ }^{\circ}\text{C}$	P_D	783 6.3	mW mW/ $^{\circ}\text{C}$
Thermal Resistance Junction-to-Ambient (Note 2)	$R_{\theta JA}$	160	$^{\circ}\text{C/W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^{\circ}\text{C}$

1. FR-4 @ 10 mm², 1 oz. copper traces, still air.

2. FR-4 @ 100 mm², 1 oz. copper traces, still air.

3. Dual heated values assume total power is the sum of two equally powered devices.

NSS40300MDR2G, NSV40300MDR2G

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector- Emitter Breakdown Voltage (I _C = -10 mA, I _B = 0)	V _{(BR)CEO}	-40	-	-	Vdc
Collector- Base Breakdown Voltage (I _C = -0.1 mA, I _E = 0)	V _{(BR)CBO}	-40	-	-	Vdc
Emitter - Base Breakdown Voltage (I _E = -0.1 mA, I _C = 0)	V _{(BR)EBO}	-7.0	-	-	Vdc
Collector Cutoff Current (V _{CB} = -40 Vdc, I _E = 0)	I _{CBO}	-	-	-0.1	μAdc
Emitter Cutoff Current (V _{EB} = -6.0 Vdc)	I _{EBO}	-	-	-0.1	μAdc

ON CHARACTERISTICS

DC Current Gain (Note 4) (I _C = -10 mA, V _{CE} = -2.0 V) (I _C = -500 mA, V _{CE} = -2.0 V) (I _C = -1.0 A, V _{CE} = -2.0 V) (I _C = -2.0 A, V _{CE} = -2.0 V) (I _C = -2.0 A, V _{CE} = -2.0 V) (Note 5)	h _{FE} h _{FE(1)} /h _{FE(2)}	250 220 180 150 0.9	380 340 300 230 0.99	- - - - -	
Collector- Emitter Saturation Voltage (Note 4) (I _C = -0.1 A, I _B = -0.010 A) (I _C = -1.0 A, I _B = -0.100 A) (I _C = -1.0 A, I _B = -0.010 A) (I _C = -2.0 A, I _B = -0.200 A)	V _{CE(sat)}	- - - -	-0.013 -0.075 -0.130 -0.135	-0.017 -0.095 -0.170 -0.170	V
Base- Emitter Saturation Voltage (Note 4) (I _C = -1.0 A, I _B = -0.01 A)	V _{BE(sat)}	-	-0.780	-0.900	V
Base- Emitter Turn-on Voltage (Note 4) (I _C = -0.1 A, V _{CE} = -2.0 V) (I _C = -0.1 A, V _{CE} = -2.0 V) (Note 6)	V _{BE(on)} V _{BE(1)} - V _{BE(2)}	- -	-0.660 0.3	-0.750 2.0	V mV
Cutoff Frequency (I _C = -100 mA, V _{CE} = -5.0 V, f = 100 MHz)	f _T	100	-	-	MHz
Input Capacitance (V _{EB} = -0.5 V, f = 1.0 MHz)	C _{ibo}	-	250	300	pF
Output Capacitance (V _{CB} = -3.0 V, f = 1.0 MHz)	C _{obo}	-	50	65	pF

SWITCHING CHARACTERISTICS

Delay (V _{CC} = -30 V, I _C = -750 mA, I _{B1} = -15 mA)	t _d	-	-	60	ns
Rise (V _{CC} = -30 V, I _C = -750 mA, I _{B1} = -15 mA)	t _r	-	-	120	ns
Storage (V _{CC} = -30 V, I _C = -750 mA, I _{B1} = -15 mA)	t _s	-	-	400	ns
Fall (V _{CC} = -30 V, I _C = -750 mA, I _{B1} = -15 mA)	t _f	-	-	130	ns

4. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%.

5. h_{FE(1)}/h_{FE(2)} is the ratio of one transistor compared to the other transistor within the same package. The smaller h_{FE} is used as numerator.

6. V_{BE(1)} - V_{BE(2)} is the absolute difference of one transistor compared to the other transistor within the same package.

TYPICAL CHARACTERISTICS

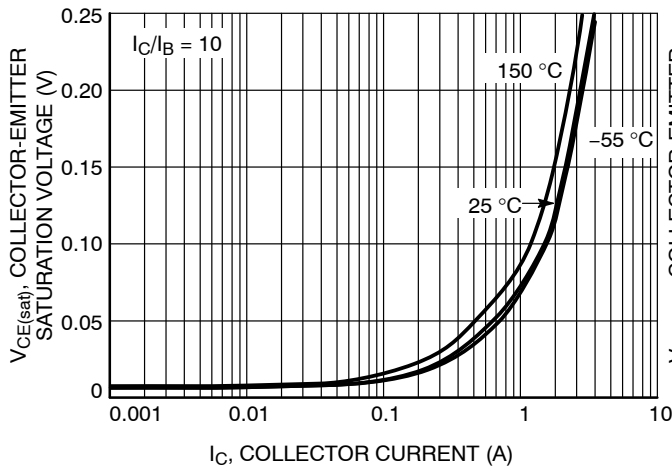


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

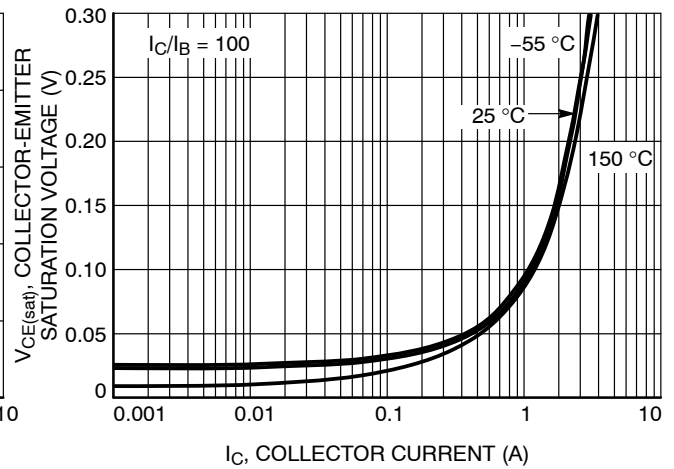


Figure 2. Collector Emitter Saturation Voltage vs. Collector Current

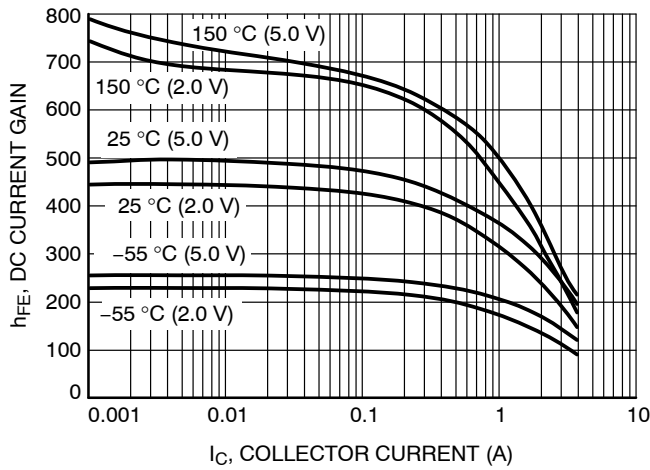


Figure 3. DC Current Gain vs. Collector Current

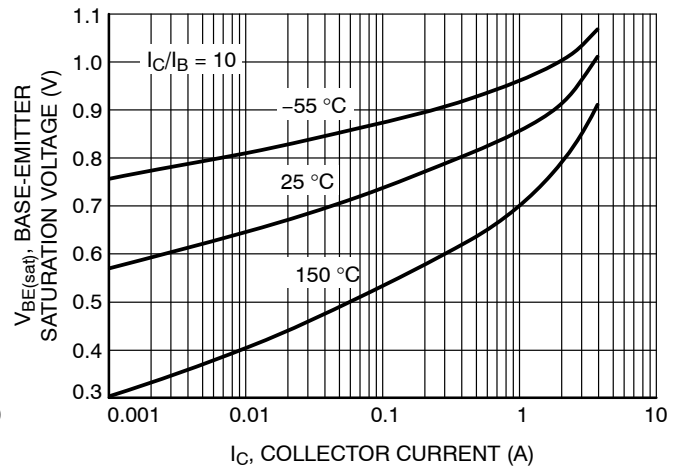


Figure 4. Base Emitter Saturation Voltage vs. Collector Current

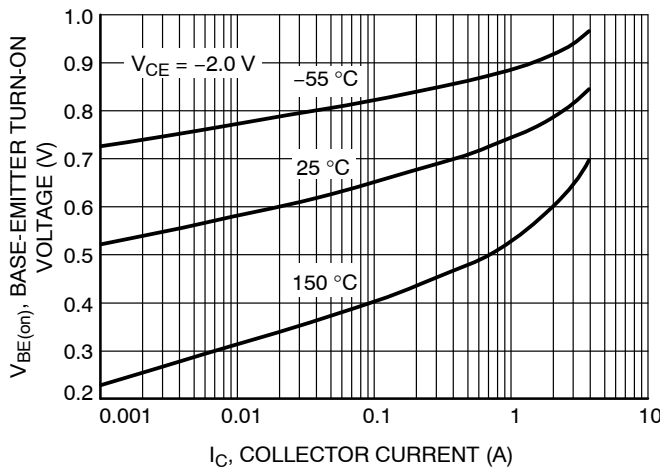


Figure 5. Base Emitter Turn-On Voltage vs. Collector Current

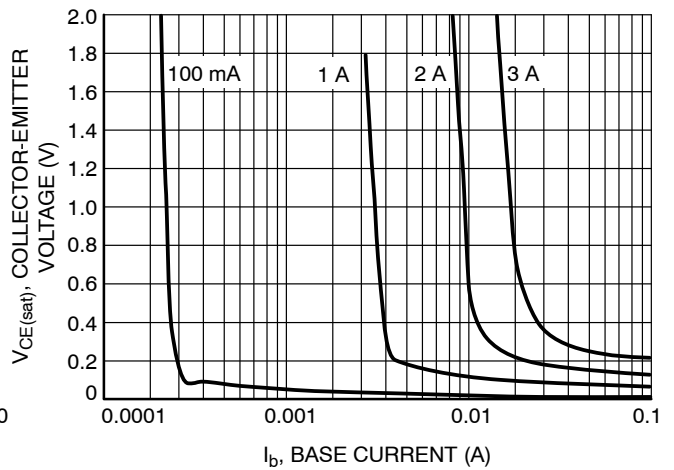


Figure 6. Saturation Region

TYPICAL CHARACTERISTICS

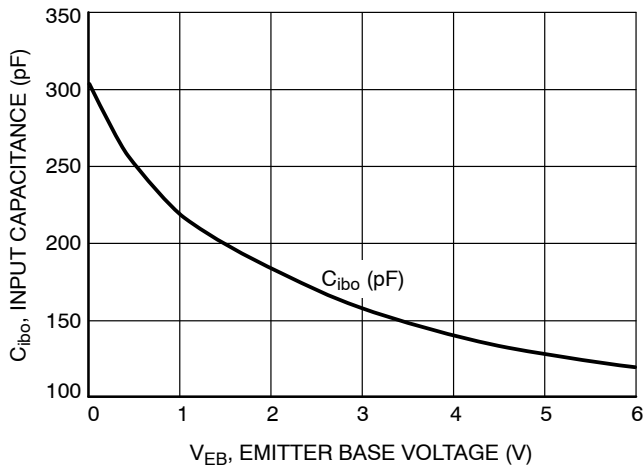


Figure 7. Input Capacitance

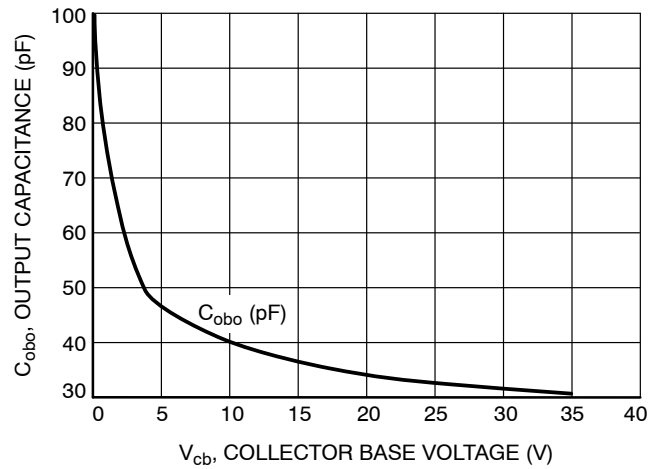


Figure 8. Output Capacitance

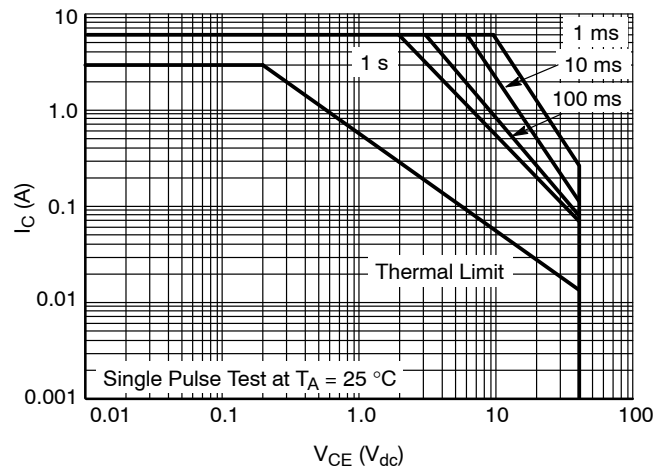


Figure 9. Safe Operating Area

NSS40300MDR2G, NSV40300MDR2G

REVISION HISTORY

Revision	Description of Changes	Date
3	Rebranded the Data Sheet to onsemi format.	11/6/2025

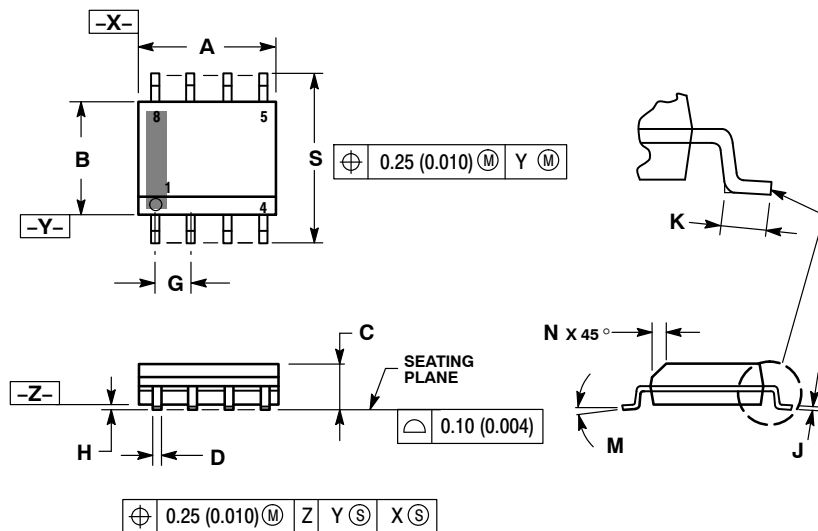
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC
MARKING DIAGRAM*



SCALE 6:1 (mm/inches)



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

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