

May 1997

Features

- 10A, 30V
- $r_{DS(ON)} = 0.200\Omega$
- *Temperature Compensating* PSPICE Model
- PSPICE Thermal Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFD10P03L	TO-251AA	10P03L
RFD10P03LSM	TO-252AA	10P03L
RFP10P03L	TO-220AB	F10P03L

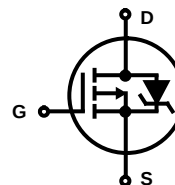
NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-252AA variant in tape and reel, i.e. RFD10P03LSM9A..

Formerly developmental type TA49205.

Description

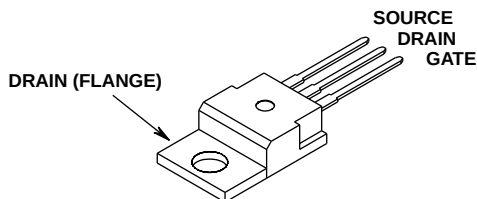
These products are P-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Symbol

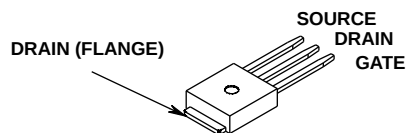


Packaging

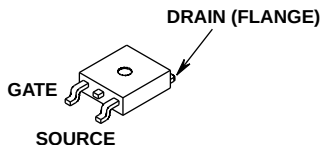
JEDEC TO-220AB



JEDEC TO-251AA



JEDEC TO-252AA



RFD10P03L, RFD10P03LSM, RFP10P03L

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

	RFD10P03L, RFD10P03LSM, RFP10P03L	UNITS
Drain to Source Voltage	V_{DSS}	-30 V
Drain to Gate Voltage ($R_{GS} = 20\text{K}\Omega$)	V_{DGR}	-30 V
Gate to Source Voltage	V_{GS}	± 10 V
Drain Current		
RMS Continuous	I_D	10 A
Pulsed Drain Current	I_{DM}	See Figure 5
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve
Power Dissipation	P_D	65 W
Derate Above 25°C		0.43 W/ $^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175 $^{\circ}\text{C}$
Maximum Lead Temperature for Soldering (0.063in (1.6mm) from case for 10s)	T_L	300 $^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V		-30	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA		-1	-	-2	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -30V,	T _C = 25°C	-	-	-1	μA
		V _{GS} = 0V	T _C = 150°C	-	-	-50	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±10V		-	-	±100	nA
Drain to Source On Resistance (Note 1)	r _{DS(ON)}	I _D = 10A, V _{GS} = -5V		-	-	0.200	Ω
		I _D = 10A, V _{GS} = -4.5V				0.220	Ω
Turn-On Time	t _{ON}	V _{DD} = 15V, I _D ≅ 10A R _L = 1.5Ω, R _{GS} = 5Ω, V _{GS} = -5V		-	-	100	ns
Turn-On Delay Time	t _{d(ON)}			-	15	-	ns
Rise Time	t _r			-	50	-	ns
Turn-Off Delay Time	t _{d(OFF)}			-	35	-	ns
Fall Time	t _f			-	20	-	ns
Turn-Off Time	t _{OFF}			-	-	80	ns
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0 to -10V	V _{DD} = -24V, I _D ≅ 10A, R _L = 2.4Ω	-	25	30	nC
Gate Charge at -5V	Q _{g(-5)}	V _{GS} = 0 to -5V		-	13	16	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0 to -1V		-	1.2	1.5	nC
Input Capacitance	C _{ISS}	V _{DS} = -25V, V _{GS} = 0V f = 1MHz		-	1035	-	pF
Output Capacitance	C _{OSS}			-	340	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	35	-	pF
Thermal Resistance, Junction to Case	R _{θJC}			-	-	2.30	°C/W
Thermal Resistance, Junction to Ambient	R _{θJA}	RFD10P03L, RFD10P03LSM		-	-	100	°C/W
		RFP10P03L				80	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Forward Voltage	V_{SD}	$I_{SD} = -10\text{A}$	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	$I_{SD} = -10\text{A}, dI_{SD}/dt = -100\text{A}/\mu\text{s}$	-	-	75	ns

NOTE:

1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

Typical Performance Curves Unless Otherwise Specified

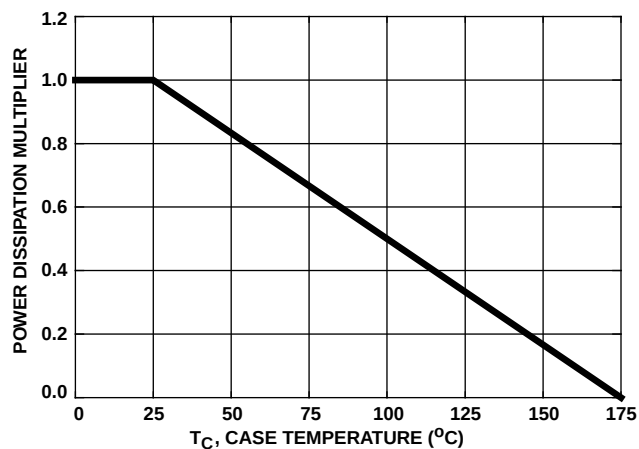


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

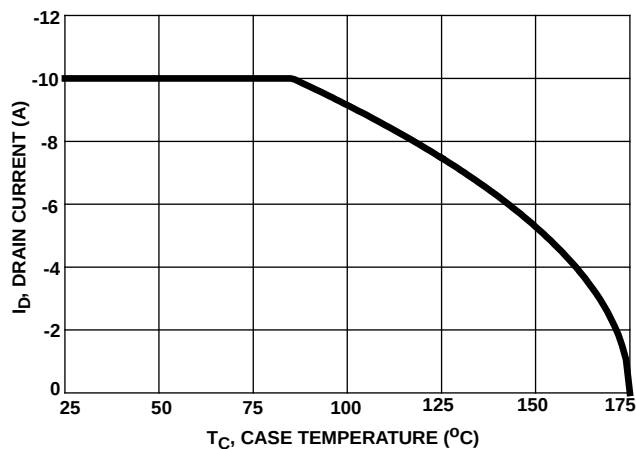


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

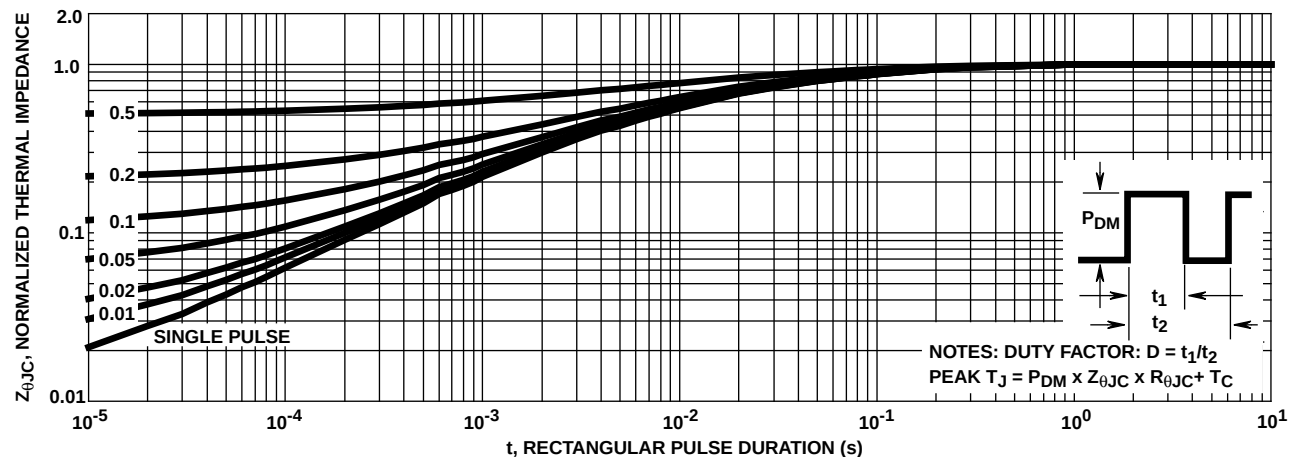


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

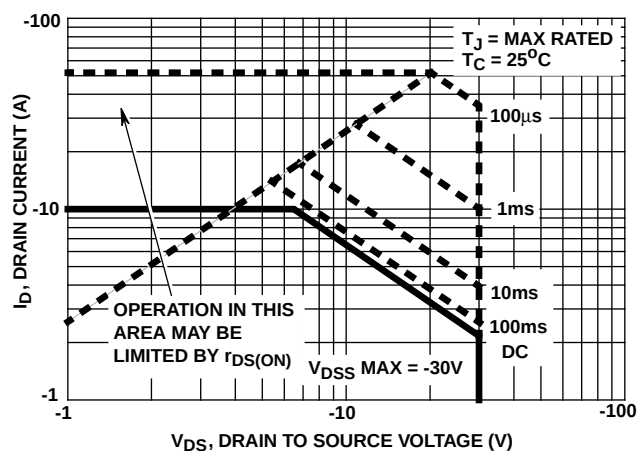


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

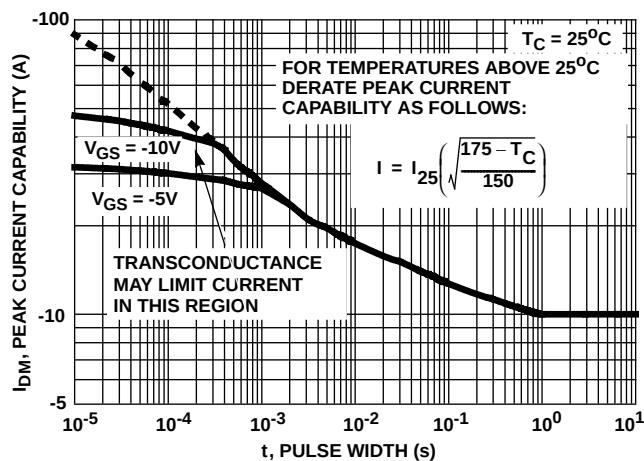
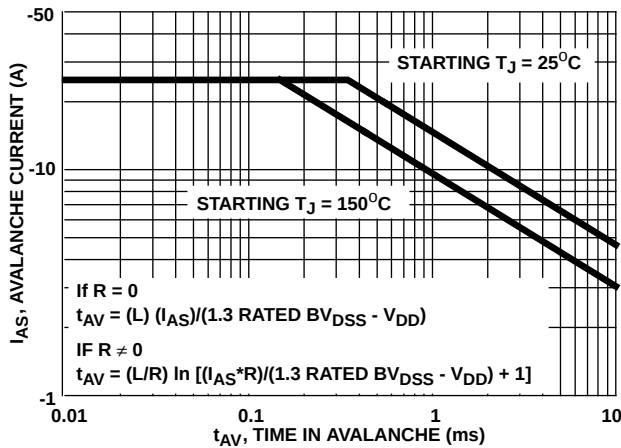


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

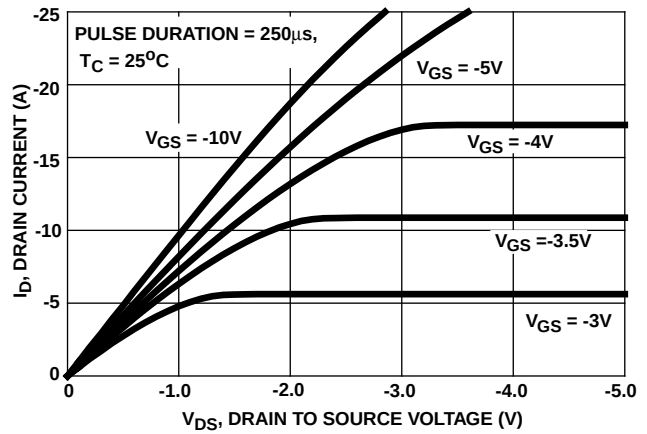


FIGURE 7. SATURATION CHARACTERISTICS

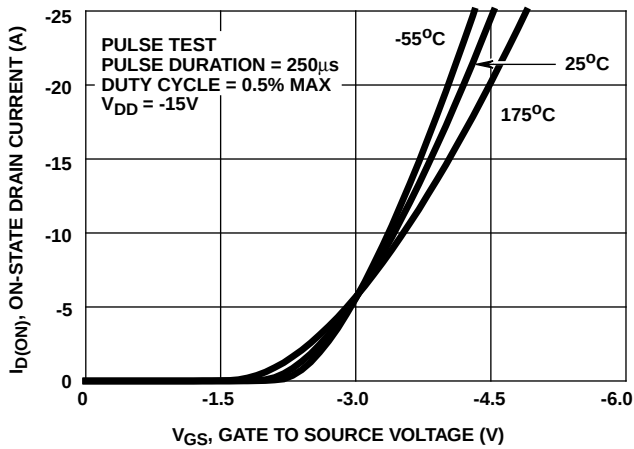


FIGURE 8. TRANSFER CHARACTERISTICS

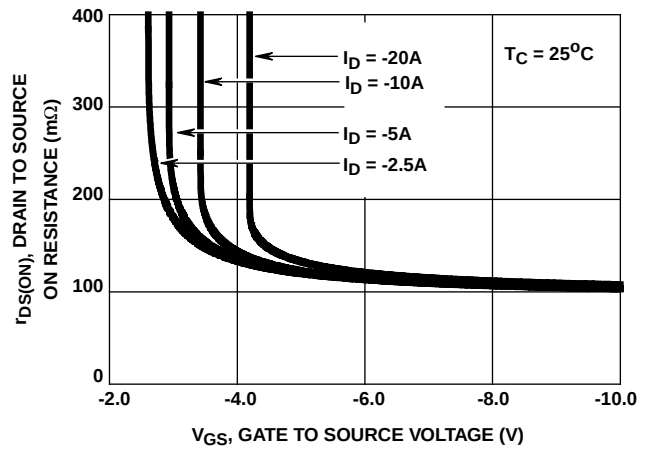


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

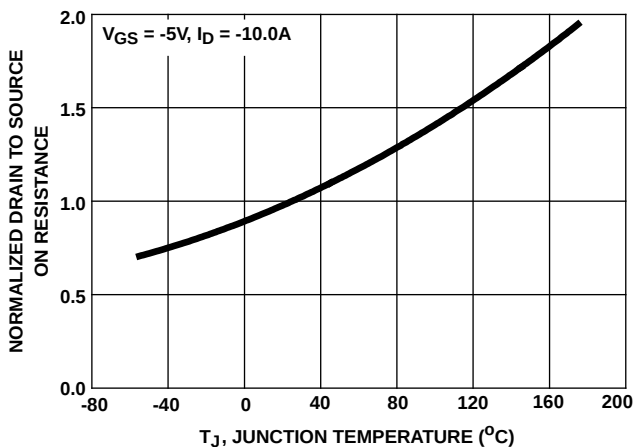


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

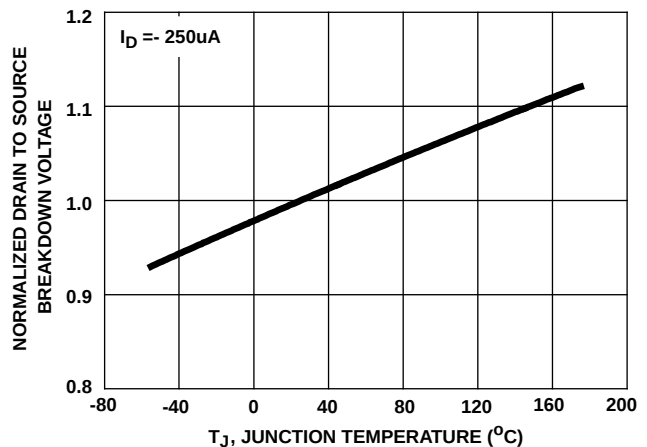


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

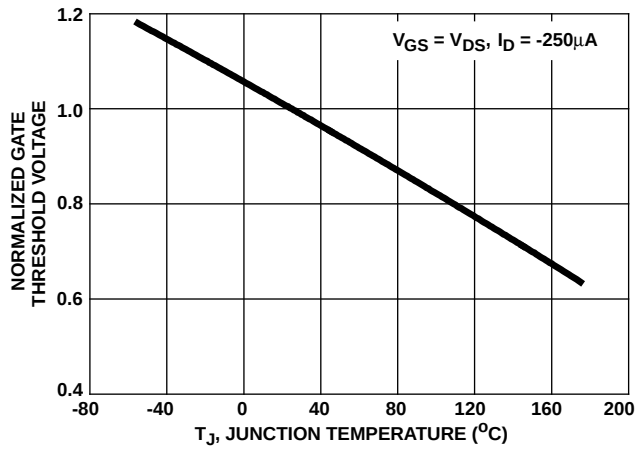


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

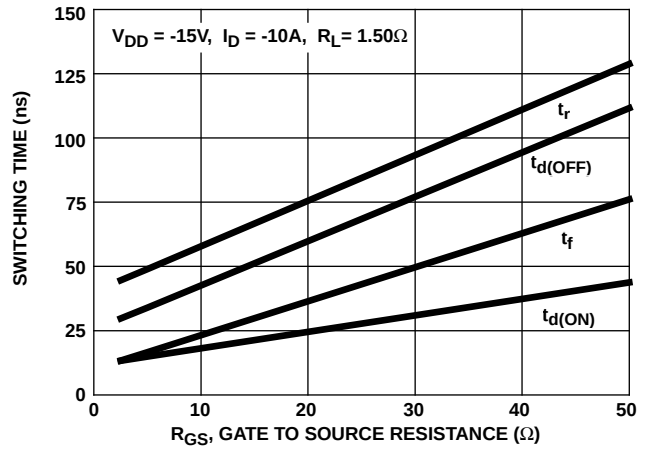
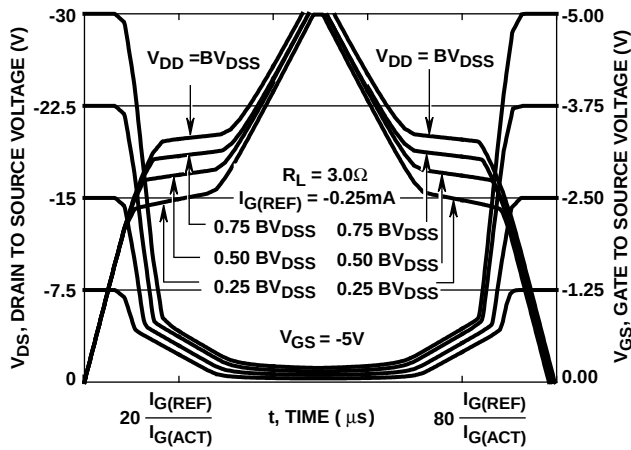


FIGURE 13. SWITCHING TIME vs GATE RESISTANCE



NOTE: Refer to Application Notes AN7254 and AN7260.

FIGURE 14. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

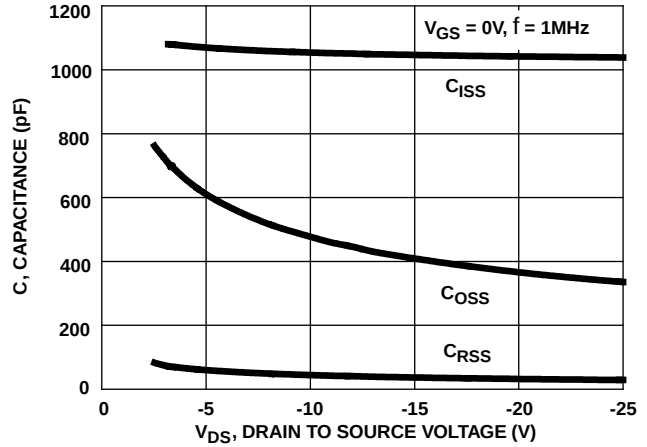


FIGURE 15. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Test Circuits and Waveforms

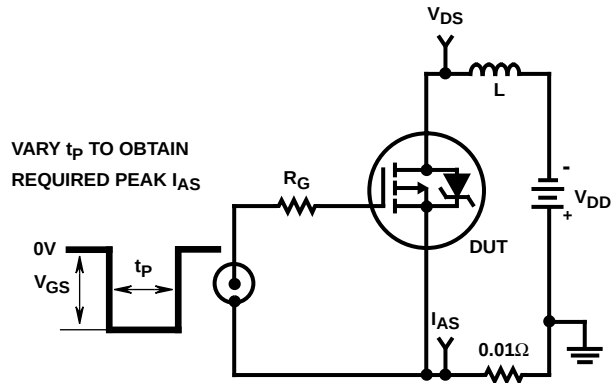


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

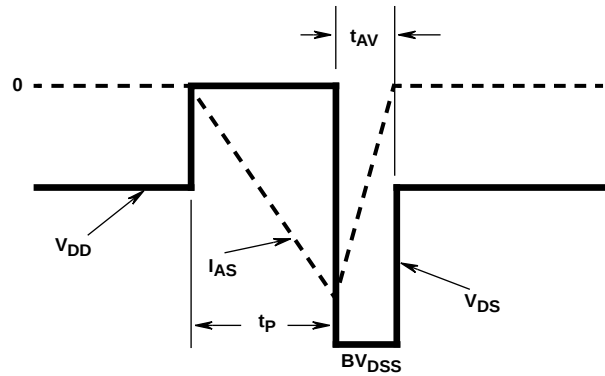


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

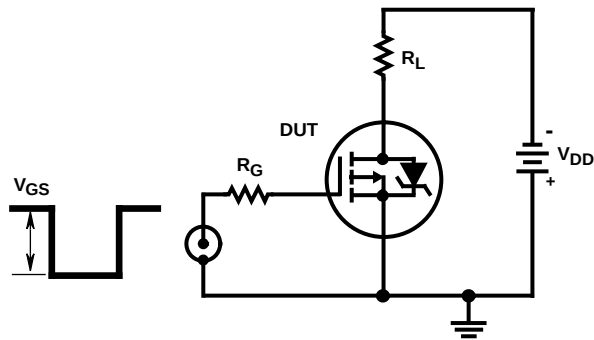


FIGURE 18. SWITCHING TIME TEST CIRCUIT

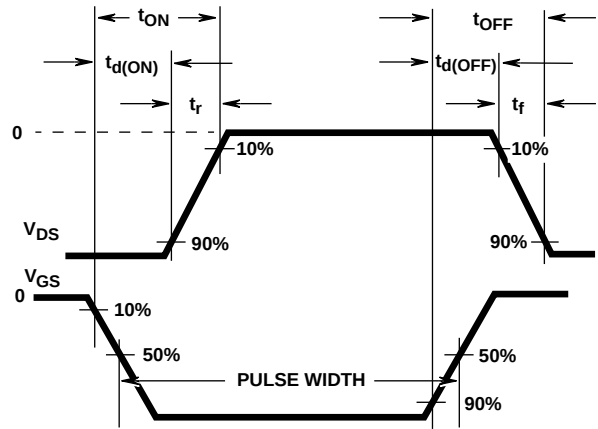


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

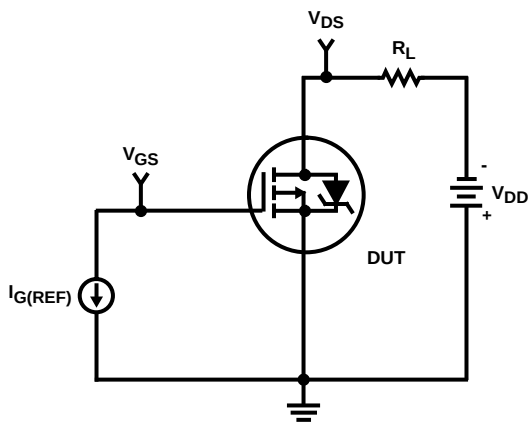


FIGURE 20. GATE CHARGE TEST CIRCUIT

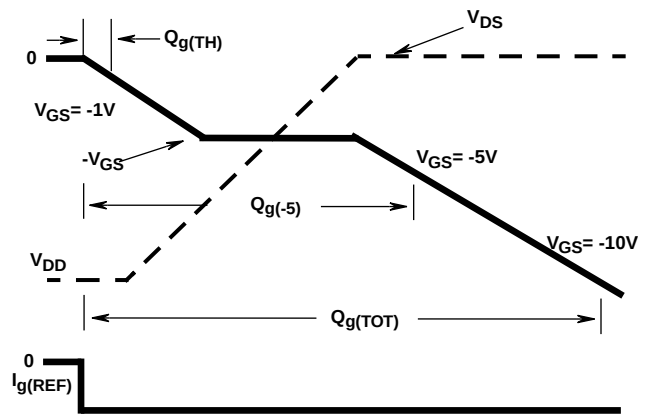


FIGURE 21. GATE CHARGE WAVEFORMS

PSpice Electrical Model

.SUBCKT RFD10P03L 2 1 3 REV 22 Aug 96

CA 12 8 1.29e-9
CB 15 14 9.90e-10
CIN 6 8 1.01e-9

DBODY 5 7 DBODYMOD
DBREAK 7 11 DBREAKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -36.49
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTHRES 6 21 19 8 1
EVTEMP 6 20 18 22 1

IT 8 17 1

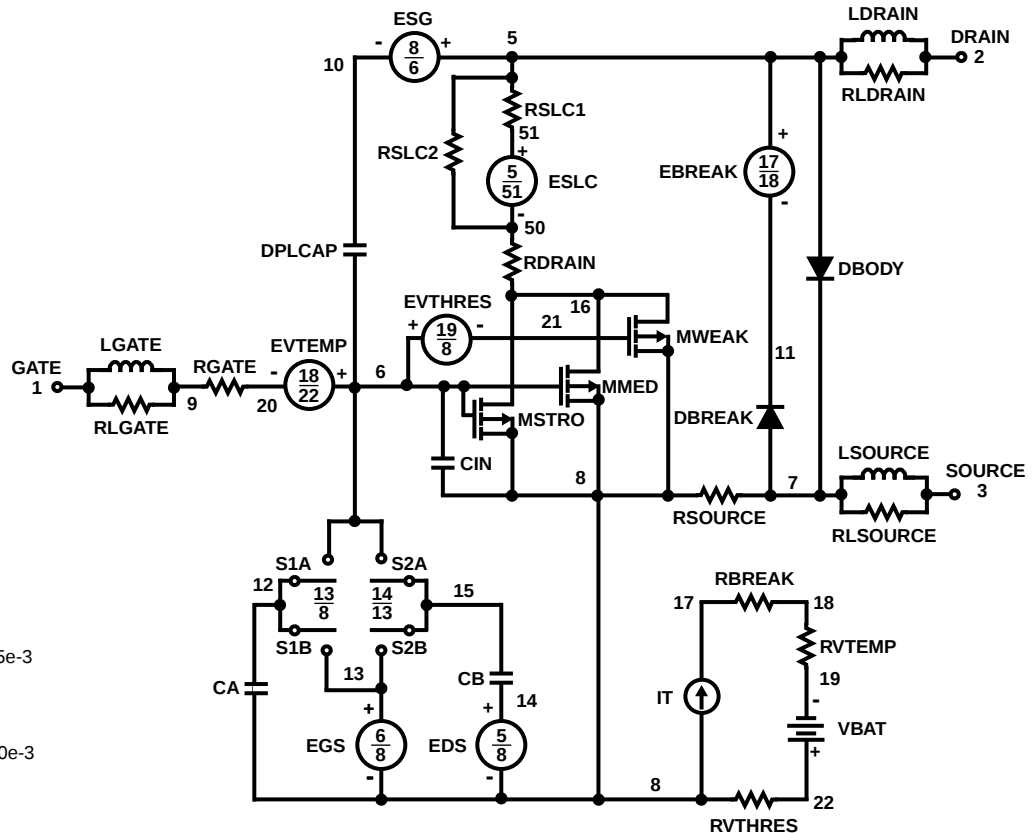
LDRAIN 2 5 1e-9
LGATE 1 9 3.40e-9
LSOURCE 3 7 3.22e-9

MMED 16 6 8 8 MmedMOD
MSTRO 16 6 8 8 MstroMOD
MWEAK 16 21 8 8 MweakMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 68.25e-3
RGATE 9 20 2.54
RSLC1 5 51 RSCLMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSourceMOD 25.00e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1



ESCL 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*33),5.0))}

.MODEL DBODYMOD D (IS=9.15e-13 RS=3.25e-2 IKF=0.05 N=0.97 TRS1=4.11e-5 TRS2=2.03e-6 CJO=1.13e-9 M=0.40 TT=3.72e-8)
.MODEL DBREAKMOD D (RS=2.62e-1 TRS1=1.74e-3 TRS2=-3.81e-6)
.MODEL DPLCAPMOD D (CJO=1.46e-10 IS=1e-30 N=10 M=0.50)
.MODEL MSTRONGMOD PMOS (VTO=-1.95 KP=11.60 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MMEDMOD PMOS (VTO=-1.65 KP=1.00 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=2.54)
.MODEL MWEAKMOD PMOS (VTO=-1.43 KP=0.09 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=25.4 RS=0.1)
.MODEL RBREAKMOD RES (TC1=9.17e-4 TC2=-2.74e-7)
.MODEL RDRAINMOD RES (TC1=6.35e-3 TC2=1.98e-5)
.MODEL RSOURCEMOD RES (TC1=0 TC2=0)
.MODEL RSCLMOD RES (TC1=2e-3 TC2=0)
.MODEL RVTHRESMOD RES (TC1=1.23e-3 TC2=1.97e-6)
.MODEL RVTEMPMOD RES (TC1=-1.18e-3 TC2=1.44e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=4.80 VOFF=1.80)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.80 VOFF=4.80)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.40 VOFF=-3.40)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.40 VOFF=-0.40)
ENDS

For further discussion of the PSPICE model consult A New PSPICE Sub-circuit for the Power MOSFet Featuring Global Temperature Options; authored by William J. Hepp and C. Frank Wheatley.

PSpice Thermal Model

REV 29 Aug 96

RFP10P03L

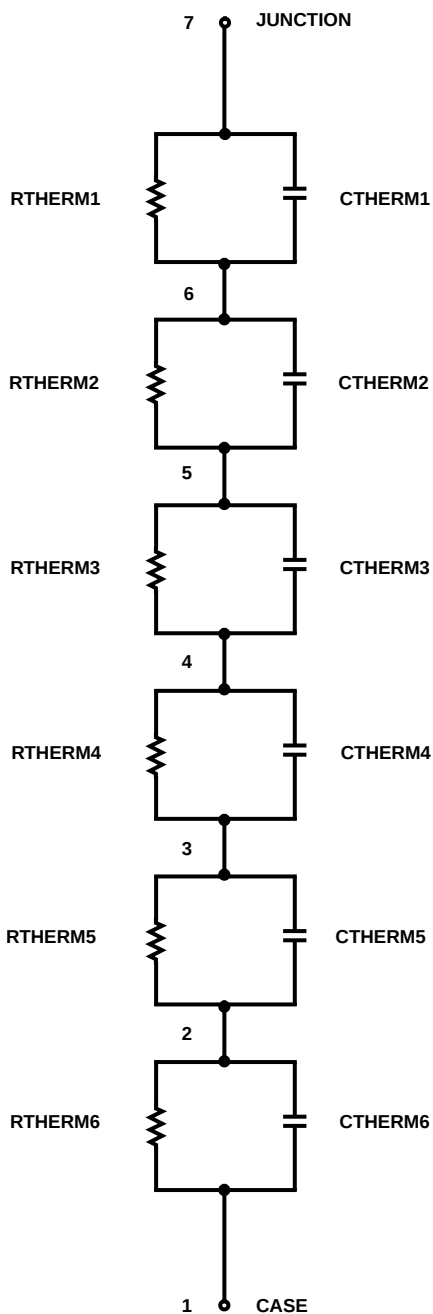
CTHERM1 7 6 5.00e-7
CTHERM2 6 5 5.35e-4
CTHERM3 5 4 5.50e-4
CTHERM4 4 3 1.75e-3
CTHERM5 3 2 1.25e-2
CTHERM6 2 1 0.45

RTHERM1 7 6 1.00e-2
RTHERM2 6 5 2.05e-2
RTHERM3 5 4 5.39e-2
RTHERM4 4 3 5.45e-1
RTHERM5 3 2 1.01
RTHERM6 2 1 0.50

RFD10P03L, RFD10P03LSM

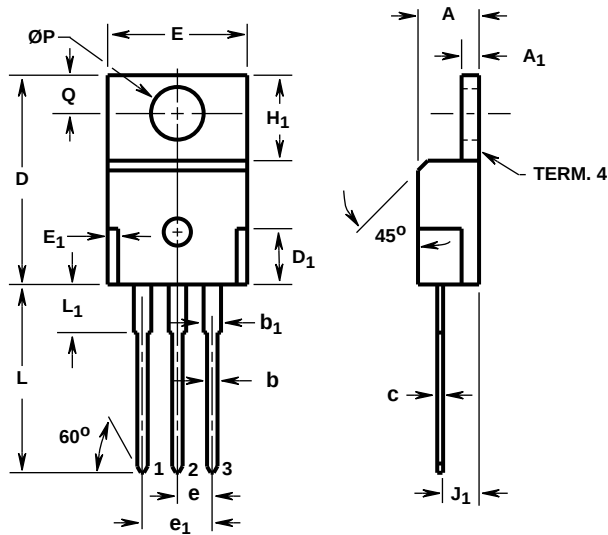
CTHERM1 7 6 5.00e-7
CTHERM2 6 5 5.35e-4
CTHERM3 5 4 5.50e-4
CTHERM4 4 3 1.75e-3
CTHERM5 3 2 1.25e-2
CTHERM6 2 1 0.11

RTHERM1 7 6 1.00e-2
RTHERM2 6 5 2.05e-2
RTHERM3 5 4 5.39e-2
RTHERM4 4 3 5.45e-1
RTHERM5 3 2 1.01
RTHERM6 2 1 0.50



TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



LEAD NO. 1 - GATE
 LEAD NO. 2 - DRAIN
 LEAD NO. 3 - SOURCE
 TERM. 4 - DRAIN

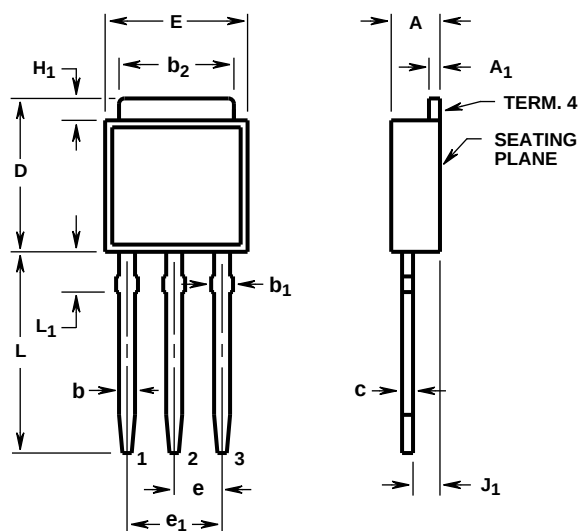
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D ₁	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E ₁	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.235	0.255	5.97	6.47	-
J ₁	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.130	0.150	3.31	3.81	2
$\varnothing P$	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L₁.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

TO-251AA

3 LEAD JEDEC TO-251AA PLASTIC PACKAGE



LEAD NO. 1 - GATE
LEAD NO. 2 - DRAIN
LEAD NO. 3 - SOURCE
TERM. 4 - DRAIN

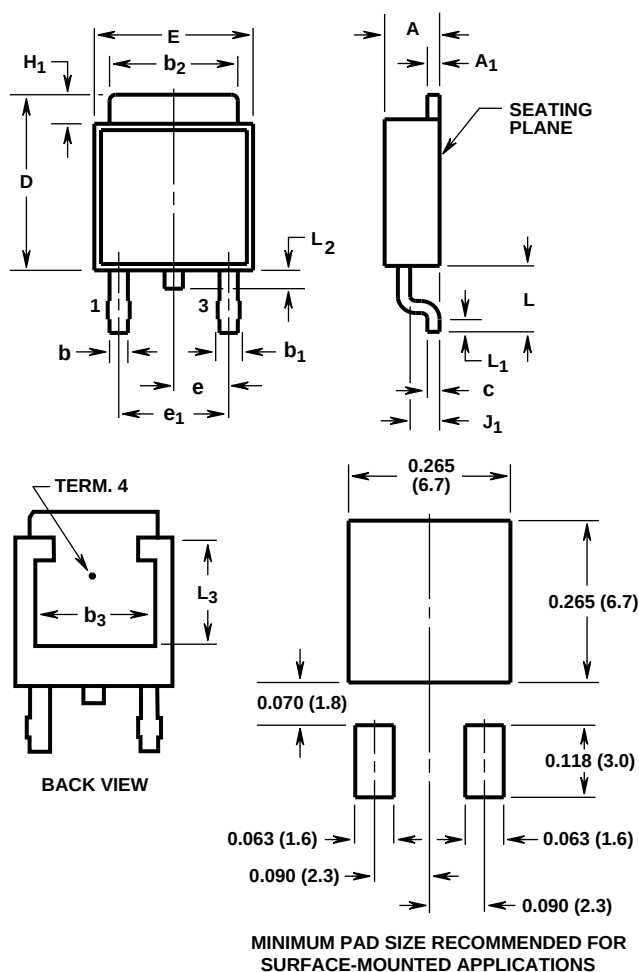
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A ₁	0.018	0.022	0.46	0.55	3, 4
b	0.028	0.032	0.72	0.81	3, 4
b ₁	0.033	0.040	0.84	1.01	3
b ₂	0.205	0.215	5.21	5.46	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		5
e ₁	0.180 BSC		4.57 BSC		5
H ₁	0.035	0.045	0.89	1.14	-
J ₁	0.040	0.045	1.02	1.14	6
L	0.355	0.375	9.02	9.52	-
L ₁	0.075	0.090	1.91	2.28	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-251AA outline dated 9-88.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 10-95.

TO-252AA

SURFACE MOUNT JEDEC TO-252AA PLASTIC PACKAGE



LEAD NO. 1 - GATE
 LEAD NO. 3 - SOURCE
 TERM. 4 - DRAIN

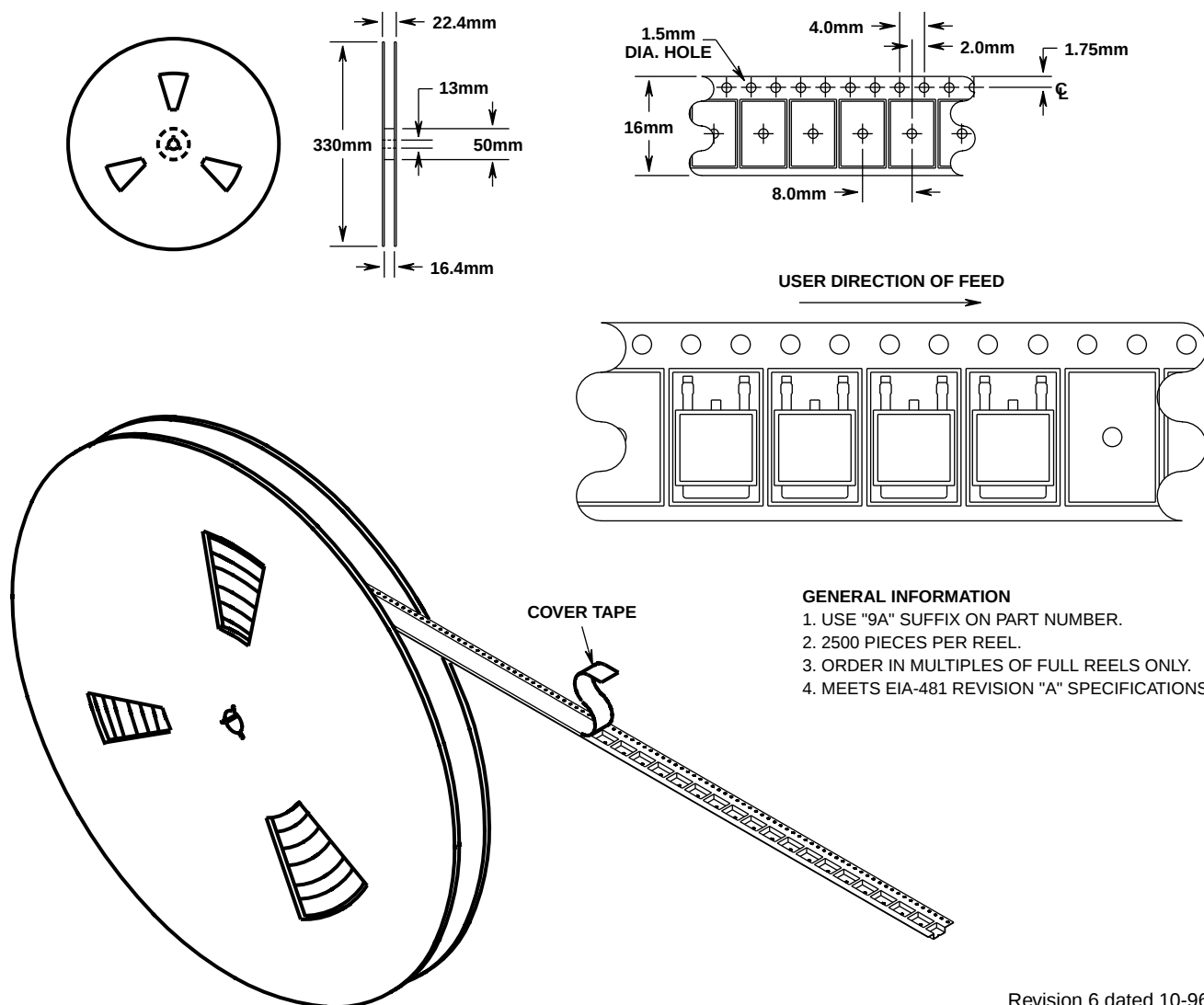
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A ₁	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b ₁	0.033	0.040	0.84	1.01	4
b ₂	0.205	0.215	5.21	5.46	4, 5
b ₃	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		7
e ₁	0.180 BSC		4.57 BSC		7
H ₁	0.035	0.045	0.89	1.14	-
J ₁	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L ₁	0.020	-	0.51	-	4, 6
L ₂	0.025	0.040	0.64	1.01	3
L ₃	0.170	-	4.32	-	2

NOTES:

- These dimensions are within allowable dimensions of Rev. B of JEDEC TO-252AA outline dated 9-88.
- L₃ and b₃ dimensions establish a minimum mounting surface for terminal 4.
- Solder finish uncontrolled in this area.
- Dimension (without solder).
- Add typically 0.002 inches (0.05mm) for solder plating.
- L₁ is the terminal length for soldering.
- Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
- Controlling dimension: Inch.
- Revision 6 dated 10-96.

TO-252AA

16mm TAPE AND REEL



GENERAL INFORMATION

1. USE "9A" SUFFIX ON PART NUMBER.
2. 2500 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 6 dated 10-96

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Harris Semiconductor products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Harris is believed to be accurate and reliable. However, no responsibility is assumed by Harris or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Harris or its subsidiaries.

Sales Office Headquarters

For general information regarding Harris Semiconductor and its products, call **1-800-4-HARRIS**

NORTH AMERICA

Harris Semiconductor
P. O. Box 883, Mail Stop 53-210
Melbourne, FL 32902
TEL: 1-800-442-7747
(407) 729-4984
FAX: (407) 729-5321

EUROPE

Harris Semiconductor
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Harris Semiconductor PTE Ltd.
No. 1 Tannery Road
Cencon 1, #09-01
Singapore 1334
TEL: (65) 748-4200
FAX: (65) 748-0400

