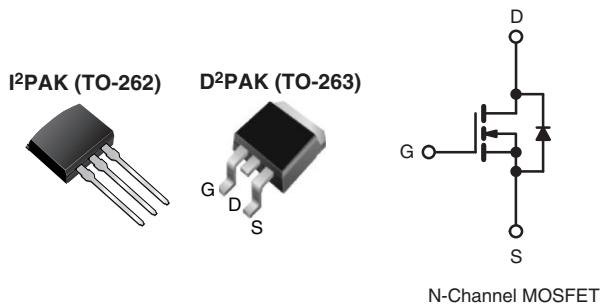


Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	900	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	8.0
Q_g (Max.) (nC)	38	
Q_{gs} (nC)	4.7	
Q_{gd} (nC)	21	
Configuration	Single	



FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount (IRFBF20S, SiHFBF20S)
- Low-Profile Through-Hole (IRFBF20L, SiHFBF20L)
- Available in Tape and Reel (IRFBF20S, SiHFBF20S)
- Dynamic dV/dt Rating
- 150 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK is a surface mount power package capable of the accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application. The through-hole version (IRFBF20L, SiHFBF20L) is available for low-profile applications.

ORDERING INFORMATION				
Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHFBF20S-GE3	SiHFBF20STR-GE3 ^a	SiHFBF20STR-GE3 ^a	SiHFBF20L-GE3
Lead (Pb)-free	IRFBF20SPbF	IRFBF20STRLPbF ^a	IRFBF20STRR-GE3 ^a	IRFBF20LPbF
	SiHFBF20S-E3	SiHFBF20STR-E3 ^a	SiHFBF20STR-E3 ^a	SiHFBF20L-E3

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage ^e			V_{DS}	900	V
Gate-Source Voltage ^e			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25$ °C	I_D	1.7	A
		$T_C = 100$ °C		1.1	
Pulsed Drain Current ^{a,e}			I_{DM}	6.8	
Linear Derating Factor				0.43	W/°C
Single Pulse Avalanche Energy ^{b,e}			E_{AS}	180	mJ
Repetitive Avalanche Current ^a			I_{AR}	1.7	A
Repetitive Avalanche Energy ^a			E_{AR}	5.4	mJ
Maximum Power Dissipation	$T_C = 25$ °C		P_D	54	W
	$T_A = 25$ °C			3.1	
Peak Diode Recovery dV/dt ^{c,e}			dV/dt	1.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	
Mounting Torque	6-32 or M3 screw			10	N

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. $V_{DD} = 50$ V; starting $T_J = 25$ °C, $L = 117$ mH, $R_g = 25$ Ω , $I_{AS} = 1.7$ A (see fig. 12).
- c. $I_{SD} \leq 1.7$ A, $dI/dt \leq 70$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- d. 1.6 mm from case.
- e. Uses IRFBF20, SiHFBF20 data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) ^a	R_{thJA}	-	40	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Case	R_{thJC}	-	2.3	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25^{\circ}\text{C}$, unless otherwise noted)

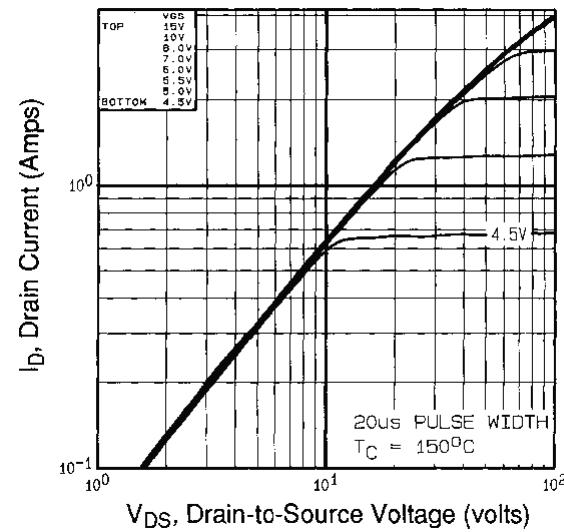
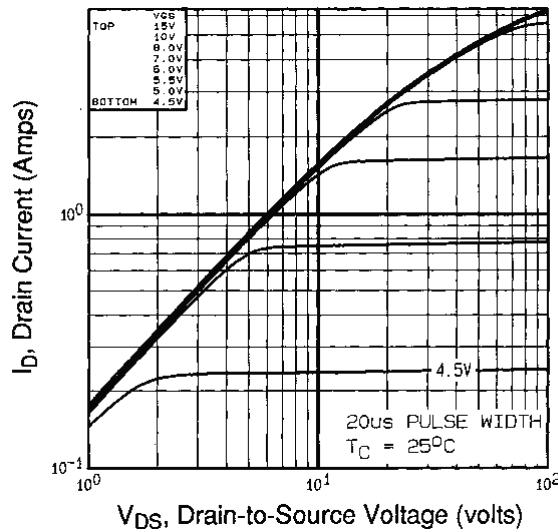
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$, $I_D = 250 \mu\text{A}$		900	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = 1 \text{ mA}$		-	1.1	-	$\text{mV}/^{\circ}\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		2.0	-	4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 900 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	100	μA	
		$V_{DS} = 720 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^{\circ}\text{C}$		-	-	500		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 1.0 \text{ A}^b$	-	-	8.0	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50 \text{ V}$, $I_D = 1.0 \text{ A}^b$		0.6	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5		-	490	-	pF	
Output Capacitance	C_{oss}			-	55	-		
Reverse Transfer Capacitance	C_{rss}			-	18	-		
Total Gate Charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 1.7 \text{ A}$, $V_{DS} = 360 \text{ V}$, see fig. 6 and 13 ^b	-	-	38	nC	
Gate-Source Charge	Q_{gs}			-	-	4.7		
Gate-Drain Charge	Q_{gd}			-	-	21		
Turn-On Delay Time	$t_{d(on)}$			-	8.0	-		
Rise Time	t_r	$V_{DD} = 450 \text{ V}$, $I_D = 1.7 \text{ A}$, $R_g = 18 \Omega$, $V_{GS} = 10 \text{ V}$, see fig. 10 ^b		-	21	-	ns	
Turn-Off Delay Time	$t_{d(off)}$			-	56	-		
Fall Time	t_f			-	32	-		

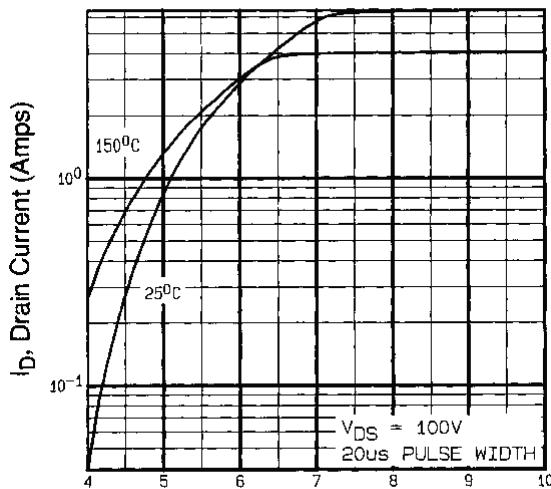
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	1.7	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	6.8	
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}$, $I_S = 1.7 \text{ A}$, $V_{GS} = 0 \text{ V}$ ^b	-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}$, $I_F = 1.7 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$ ^b	-	350	530	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.85	1.3	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

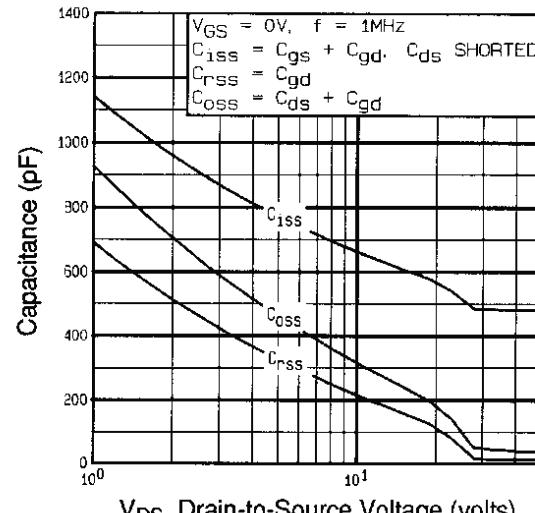
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2 \%$.
- Uses IRFBF20/SiHFBF20 data and test conditions.

TYPICAL CHARACTERISTICS (25°C , unless otherwise noted)




V_{GS}, Gate-to-Source Voltage (volts)

Fig. 3 - Typical Transfer Characteristics



V_{DS}, Drain-to-Source Voltage (volts)

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

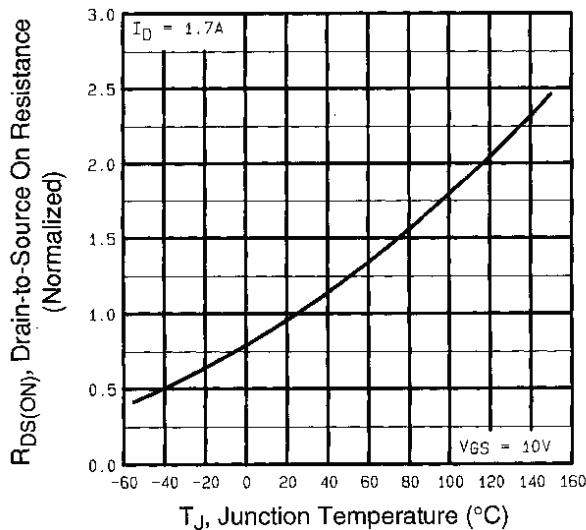


Fig. 4 - Normalized On-Resistance vs. Temperature

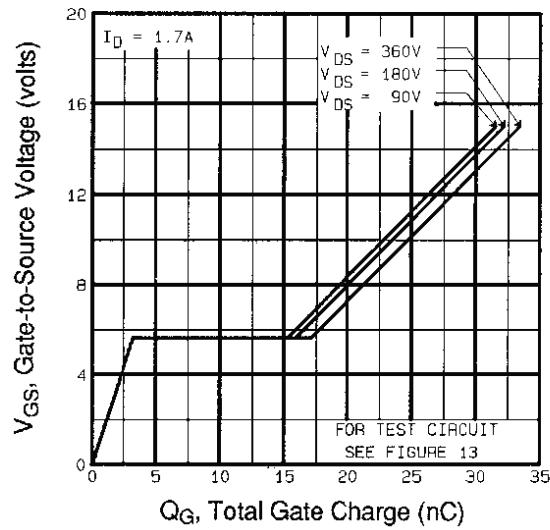


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

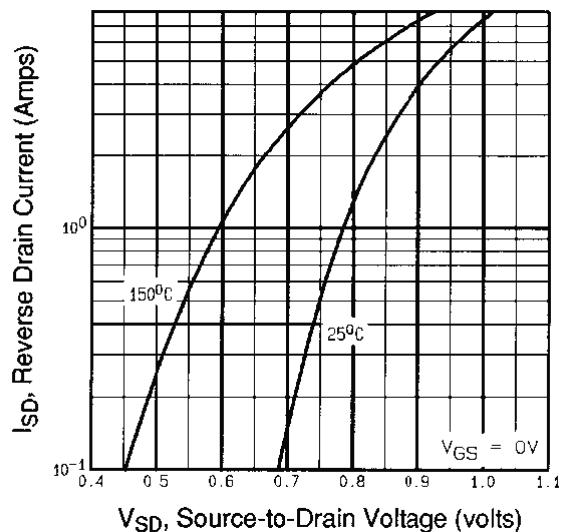


Fig. 7 - Typical Source-Drain Diode Forward Voltage

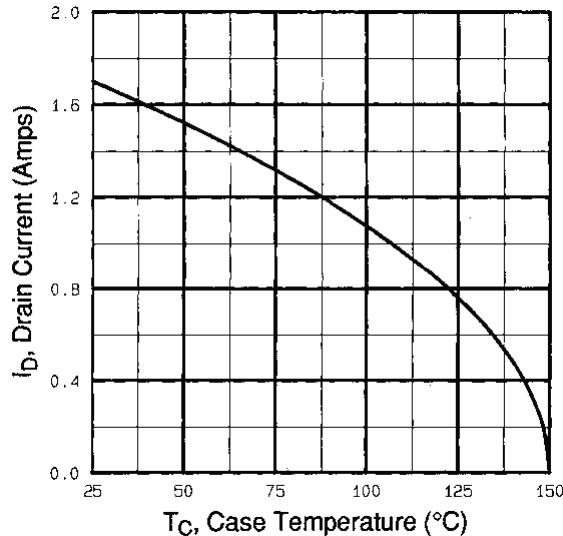


Fig. 9 - Maximum Drain Current vs. Case Temperature

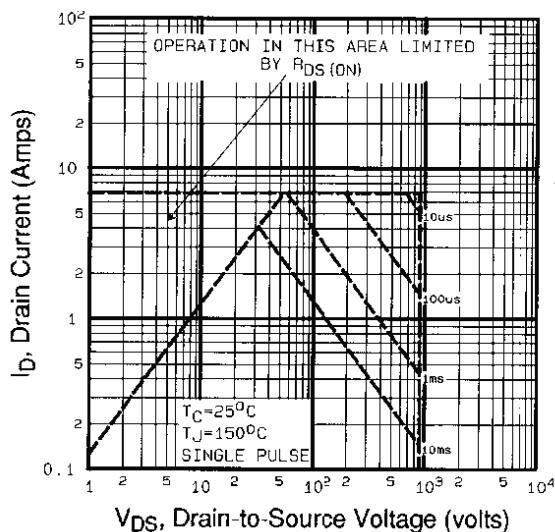


Fig. 8 - Maximum Safe Operating Area

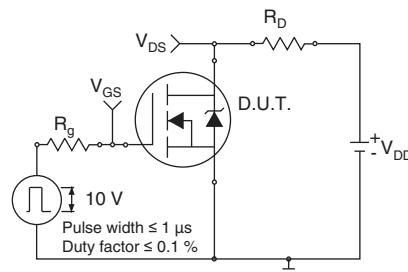


Fig. 10a - Switching Time Test Circuit

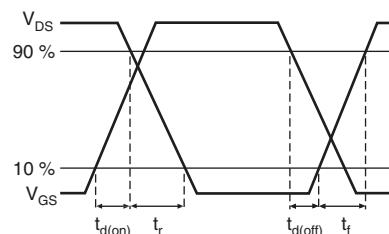


Fig. 10b - Switching Time Waveforms

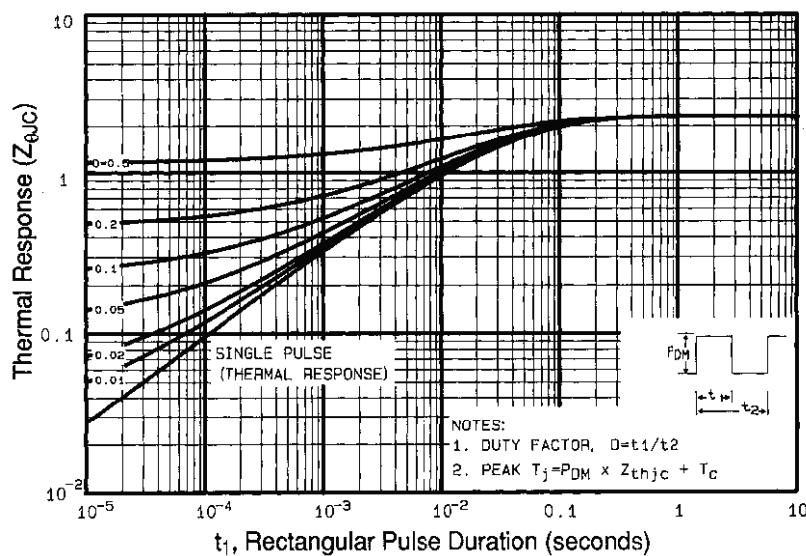


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

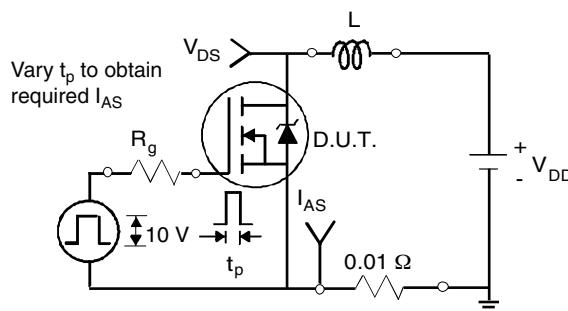


Fig. 12a - Unclamped Inductive Test Circuit

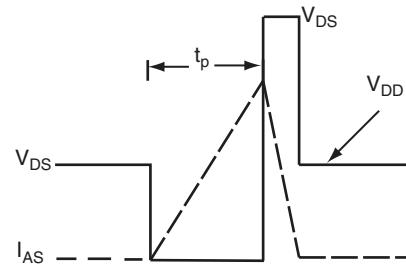


Fig. 12b - Unclamped Inductive Waveforms

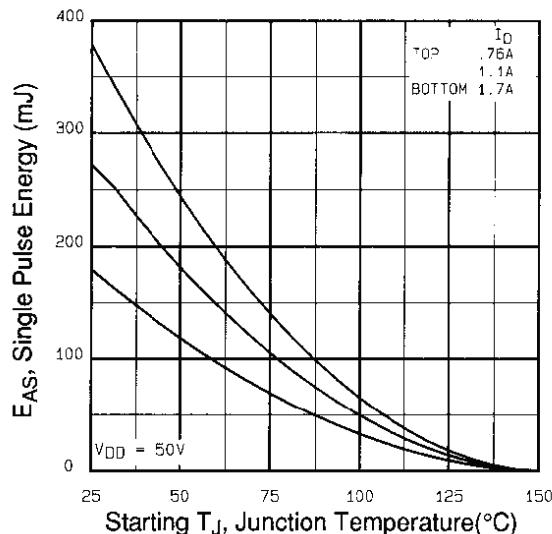


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

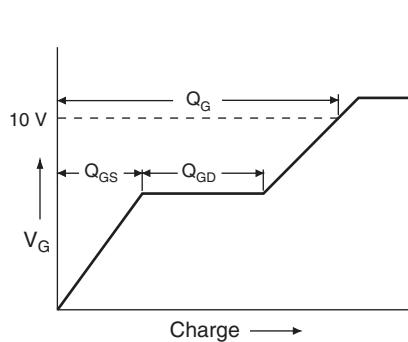


Fig. 13a - Basic Gate Charge Waveform

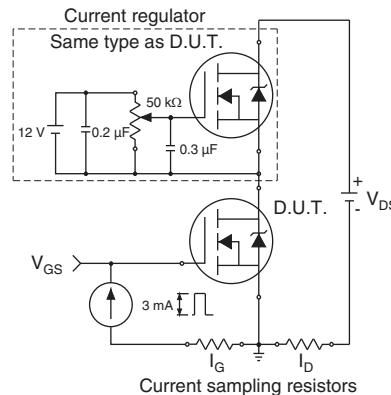


Fig. 13b - Gate Charge Test Circuit

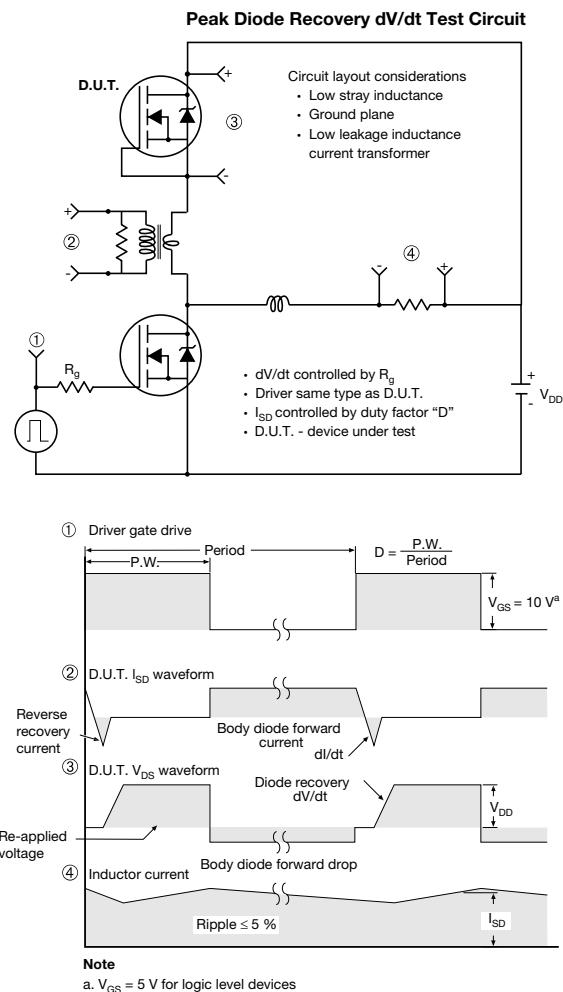
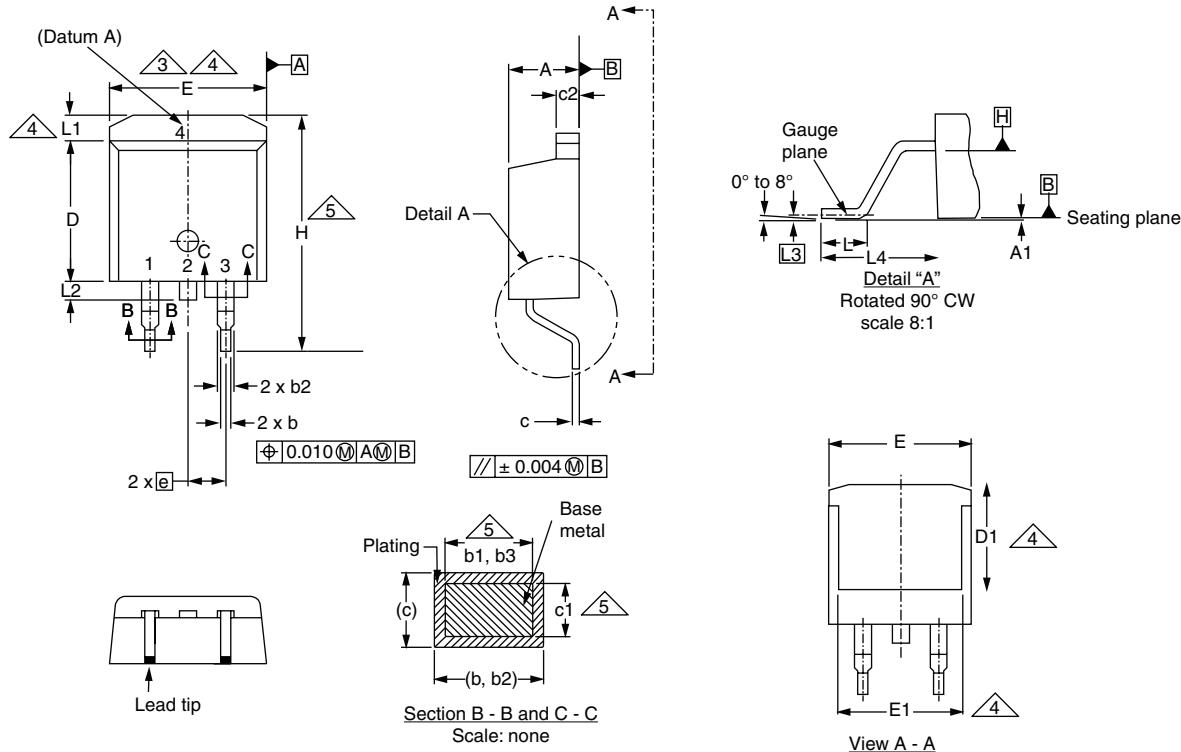


Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

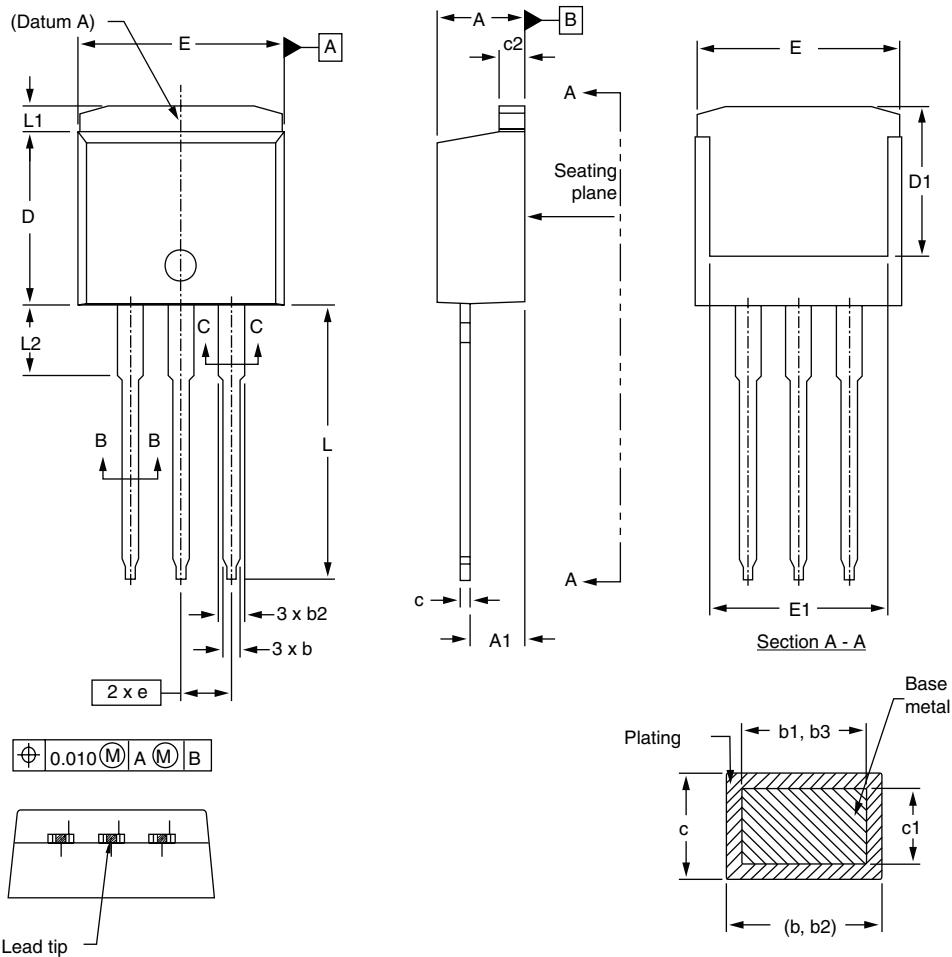
ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

I²PAK (TO-262) (HIGH VOLTAGE)



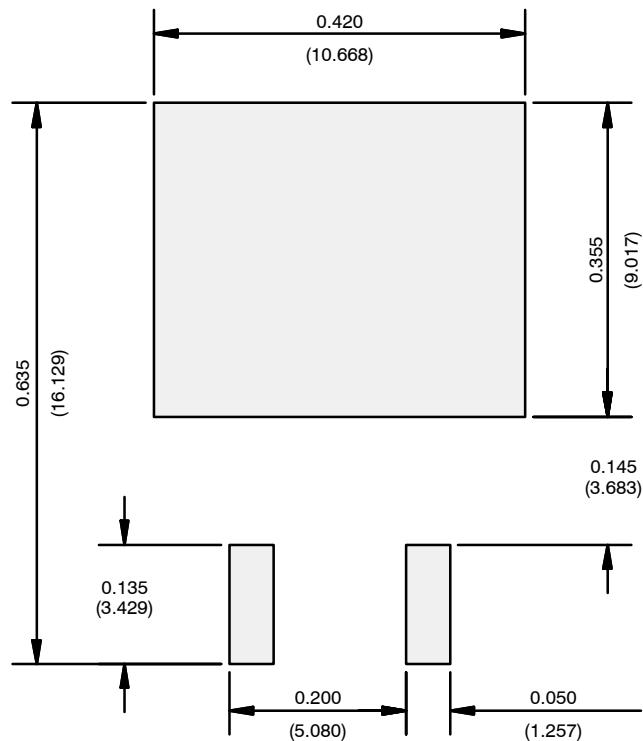
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead

Recommended Minimum Pads
Dimensions in Inches/(mm)

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