

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40175B

MSI

Quadruple D-type flip-flop

Product specification
File under Integrated Circuits, IC04

January 1995

Quadruple D-type flip-flop

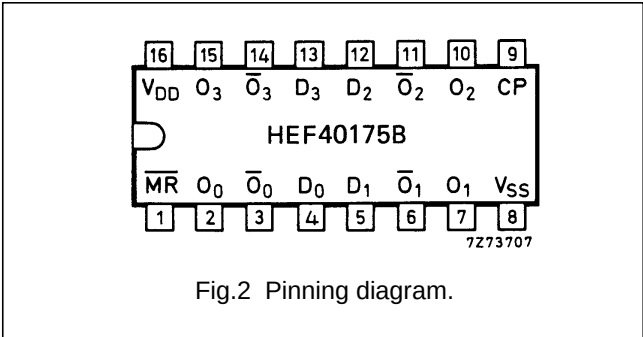
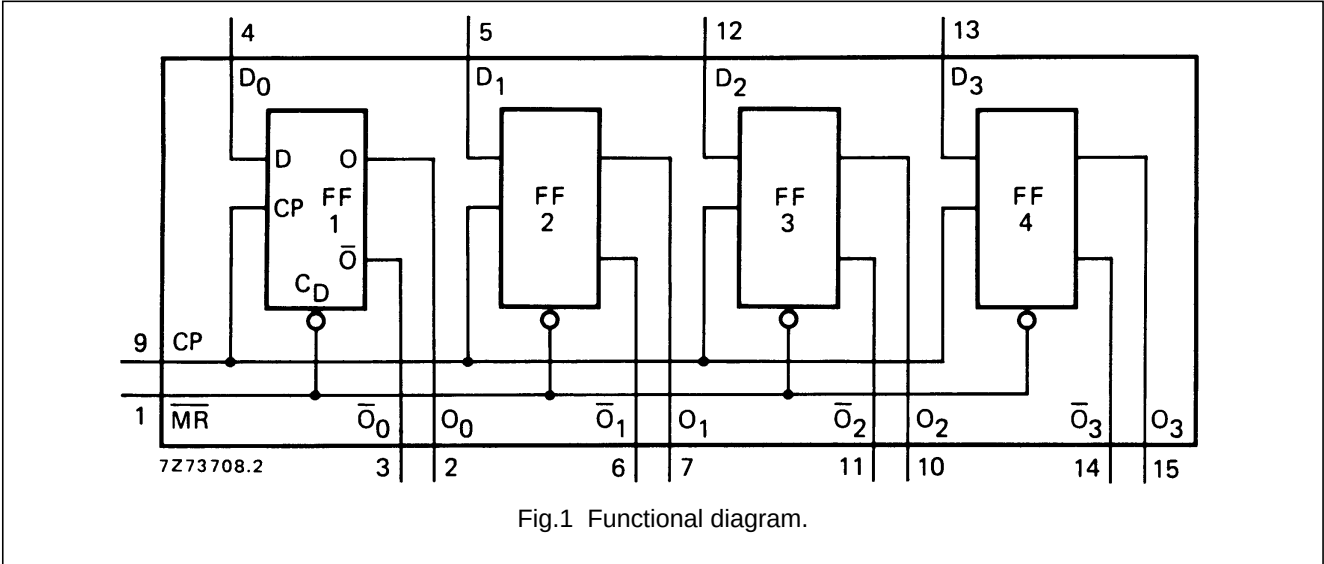
HEF40175B

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DESCRIPTION

The HEF40175B is a quadruple edge-triggered D-type flip-flop with four data inputs (D_0 to D_3), a clock input (CP), an overriding asynchronous master reset input ($\overline{MR}$), four buffered outputs (O_0 to O_3), and four complementary

buffered outputs ($\overline{O}_0$ to $\overline{O}_3$). Information on D_0 to D_3 is transferred to O_0 to O_3 on the LOW to HIGH transition of CP if $\overline{MR}$ is HIGH. When LOW, $\overline{MR}$ resets all flip-flops (O_0 to $O_3 = \text{LOW}$, $\overline{O}_0$ to $\overline{O}_3 = \text{HIGH}$), independent of CP and D_0 to D_3 .



PINNING

- D_0 to D_3 data inputs
- CP clock input (LOW to HIGH; edge-triggered)
- $\overline{MR}$ master reset input (active LOW)
- O_0 to O_3 buffered outputs
- $\overline{O}_0$ to $\overline{O}_3$ complementary buffered outputs

FUNCTION TABLE

INPUTS			OUTPUTS	
CP	D	$\overline{MR}$	O	$\overline{O}$
	H	H	H	L
	L	H	L	H
	X	H	no change	no change
X	X	L	L	H

Notes

- H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
- = positive-going transition
 = negative-going transition

HEF40175BP(N): 16-lead DIL; plastic (SOT38-1)
HEF40175BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF40175BT(D): 16-lead SO; plastic (SOT109-1)
(): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

Quadruple D-type flip-flop

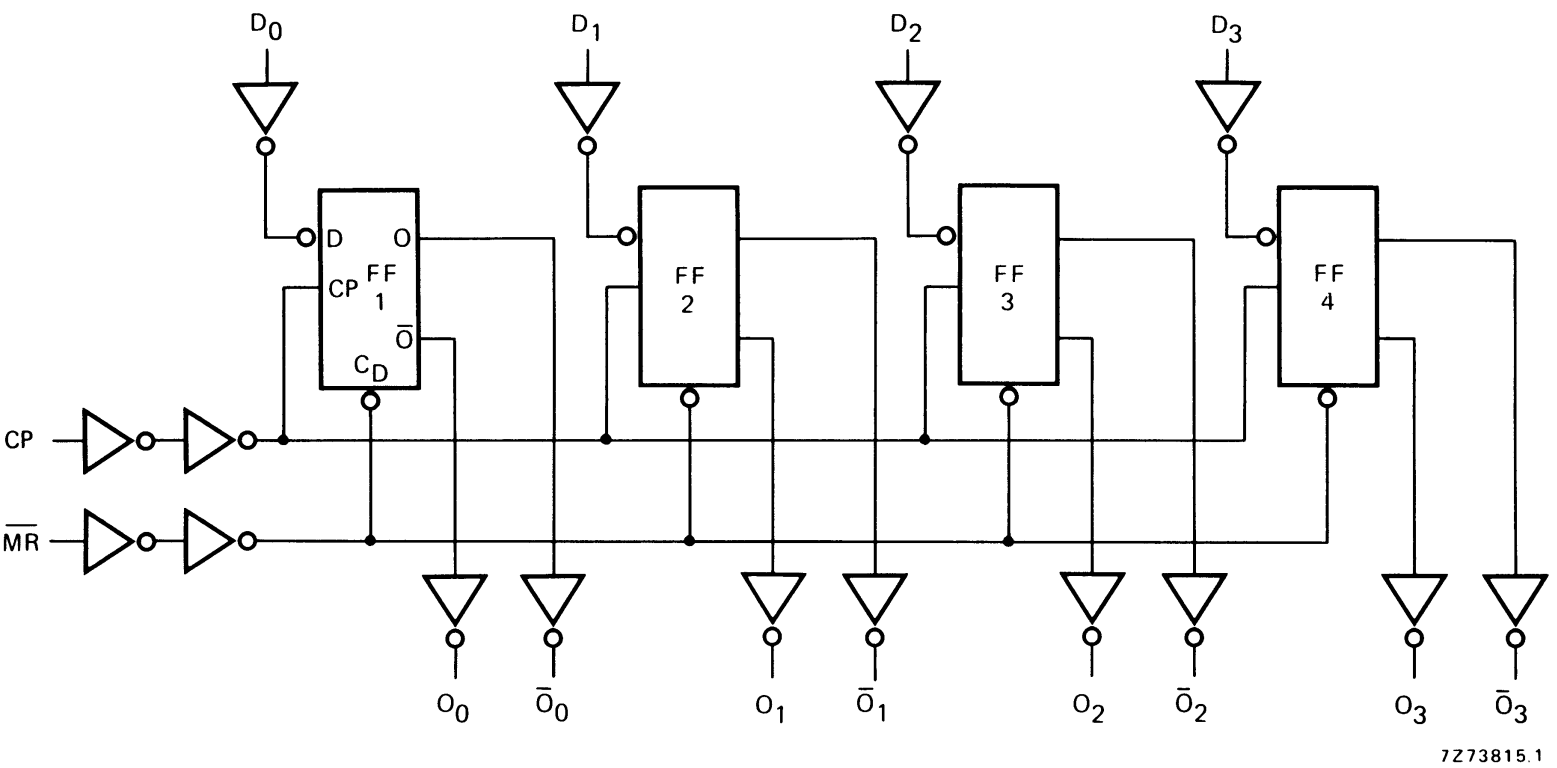
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Fig.3 Logic diagram.

Quadruple D-type flip-flop

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AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays $CP \rightarrow O_n, \overline{O}_n$ HIGH to LOW	5 10 15	t_{PHL}		80 35 25	160 70 50 ns	53 ns + (0,55 ns/pF) C_L 24 ns + (0,23 ns/pF) C_L 17 ns + (0,16 ns/pF) C_L
LOW to HIGH	5 10 15	t_{PLH}		70 30 25	140 65 45 ns	43 ns + (0,55 ns/pF) C_L 19 ns + (0,23 ns/pF) C_L 17 ns + (0,16 ns/pF) C_L
$\overline{MR} \rightarrow O_n$ HIGH to LOW	5 10 15	t_{PHL}		75 30 25	155 65 50 ns	48 ns + (0,55 ns/pF) C_L 19 ns + (0,23 ns/pF) C_L 17 ns + (0,16 ns/pF) C_L
$\overline{MR} \rightarrow \overline{O}_n$ LOW to HIGH	5 10 15	t_{PLH}		70 30 25	140 65 50 ns	43 ns + (0,55 ns/pF) C_L 19 ns + (0,23 ns/pF) C_L 17 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW	5 10 15	t_{THL}		60 30 20	120 60 40 ns	10 ns + (1,0 ns/pF) C_L 9 ns + (0,42 ns/pF) C_L 6 ns + (0,28 ns/pF) C_L
LOW to HIGH	5 10 15	t_{TLH}		60 30 20	120 60 40 ns	10 ns + (1,0 ns/pF) C_L 9 ns + (0,42 ns/pF) C_L 6 ns + (0,28 ns/pF) C_L
Set-up time $D_n \rightarrow CP$	5 10 15	t_{su}	60 20 15	30 10 5	ns ns ns	see also waveforms Fig.4
Hold time $D_n \rightarrow CP$	5 10 15	t_{hold}	25 10 10	-5 0 0	ns ns ns	
Minimum clock pulse width; LOW	5 10 15	t_{WCPL}	90 35 25	45 15 10	ns ns ns	
Minimum $\overline{MR}$ pulse width; LOW	5 10 15	t_{WMRL}	80 30 20	40 15 10	ns ns ns	
Recovery time for $\overline{MR}$	5 10 15	t_{RMR}	0 0 0	-30 -20 -15	ns ns ns	
Maximum clock pulse frequency	5 10 15	f_{max}	5 15 20	11 30 45	MHz MHz MHz	

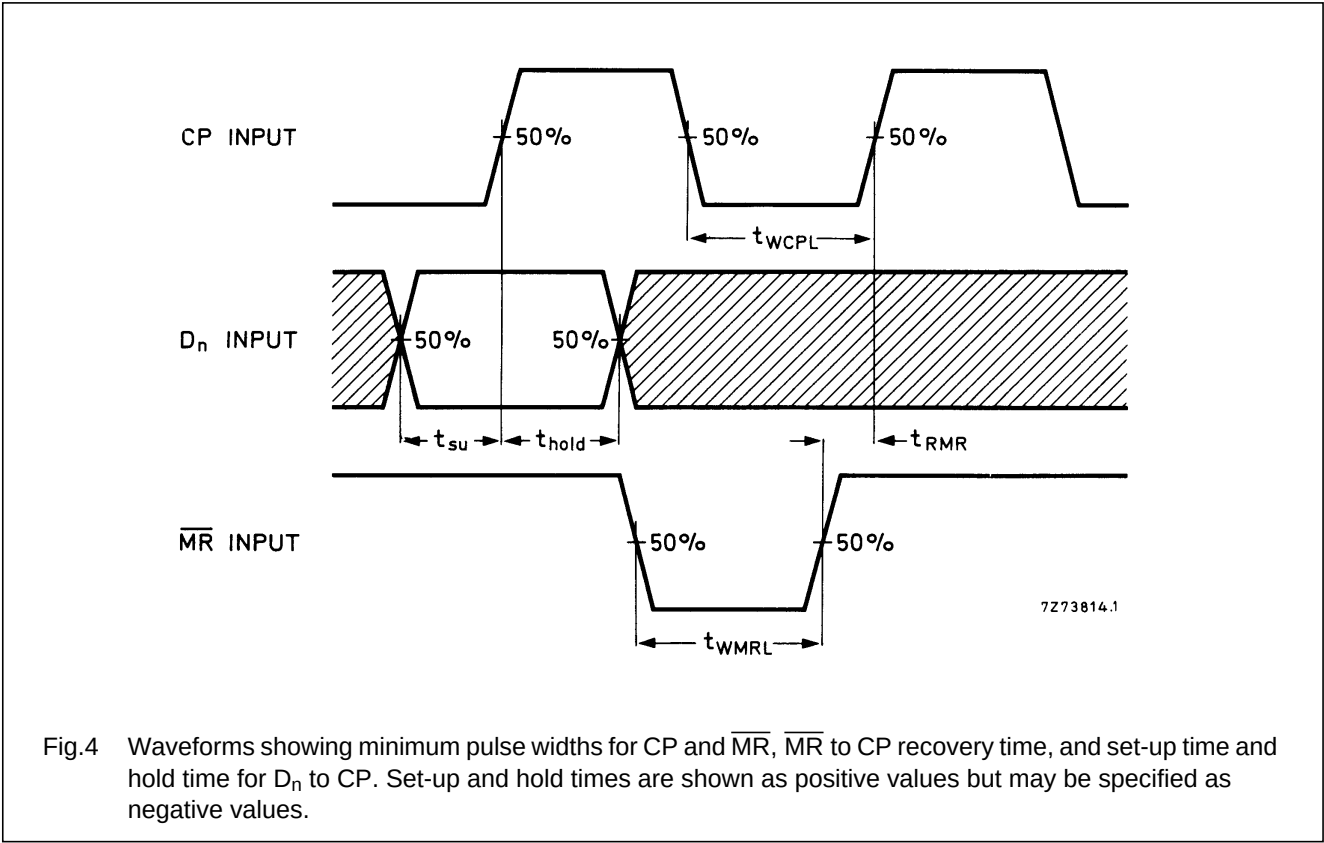
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V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	2000 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	8400 f _i + ∑ (f _o C _L) × V _{DD} ²	
	15	22 500 f _i + ∑ (f _o C _L) × V _{DD} ²	



APPLICATION INFORMATION

Some examples of applications for the HEF40175B are:

- Shift registers
- Buffer/storage register
- Pattern generator

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