

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Max  $t_{pd}$  of 4.8 ns at 3.3 V
- $\pm 24$ -mA Output Drive at 3.3 V
- B-Port Outputs Have Equivalent  $26\text{-}\Omega$  Series Resistors, So No External Resistors Are Required
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

## DESCRIPTION/ORDERING INFORMATION

This 12-bit to 24-bit registered bus exchanger is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH162268 is used for applications in which data must be transferred from a narrow high-speed bus to a wide, lower-frequency bus.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable (CLKEN) inputs are low. The select (SEL) line is synchronous with CLK and selects 1B or 2B input data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path, with a single storage register in the A-to-2B path. Proper control of these inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables (OEA, OEB). These control terminals are registered, so bus direction changes are synchronous with CLK.

The B outputs, which are designed to sink up to 12 mA, include equivalent  $26\text{-}\Omega$  resistors to reduce overshoot and undershoot.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^\circ\text{C}$ to $85^\circ\text{C}$	SSOP - DL	Tube	SN74ALVCH162268DL	ALVCH162268
		Tape and reel	SN74ALVCH162268DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCH162268GR	ALVCH162268
	VFBGA - GQL	Tape and reel	SN74ALVCH162268KR	VH2268
			74ALVCH162268ZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

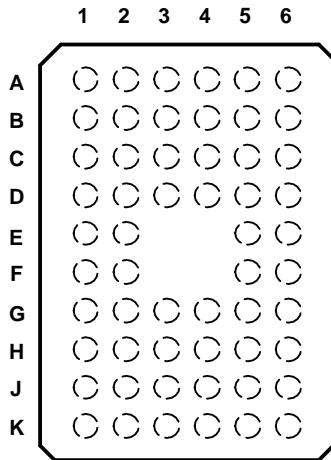
Widebus is a trademark of Texas Instruments.

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible, and  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to  $\overline{OE}$  being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

**GQL OR ZQL PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS**

	1	2	3	4	5	6
<b>A</b>	2B3	$\overline{CLKEN1B}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{CLKENA2}$	2B4
<b>B</b>	2B1	2B2	GND	GND	2B5	2B6
<b>C</b>	A2	A1	$V_{CC}$	$V_{CC}$	2B7	2B8
<b>D</b>	A4	A3	GND	GND	2B9	2B10
<b>E</b>	A6	A5			2B11	2B12
<b>F</b>	A7	A8			1B11	1B12
<b>G</b>	A9	A10	GND	GND	1B9	1B10
<b>H</b>	A11	A12	$V_{CC}$	$V_{CC}$	1B7	1B8
<b>J</b>	1B1	1B2	GND	GND	1B5	1B6
<b>K</b>	1B3	$\overline{CLKEN2B}$	$\overline{SEL}$	CLK	$\overline{CLKENA1}$	1B4

## FUNCTION TABLES

### OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

### A-TO-B STORAGE ( $\overline{OEB} = L$ )

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	$1B_0^{(1)}$	$2B_0^{(1)}$
L	L	↑	L	$L^{(2)}$	X
L	L	↑	H	$H^{(2)}$	X
X	L	↑	L	X	L
X	L	↑	H	X	H

- (1) Output level before the indicated steady-state input conditions were established
- (2) Two CLK edges are needed to propagate data.

### B-TO-A STORAGE ( $\overline{OEA} = L$ )

INPUTS						OUTPUT A
$\overline{CLKEN1B}$	$\overline{CLKEN2B}$	CLK	$\overline{SEL}$	1B	2B	
H	X	X	H	X	X	$A_0^{(1)}$
X	H	X	L	X	X	$A_0^{(1)}$
L	L	↑	H	L	X	L
L	L	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

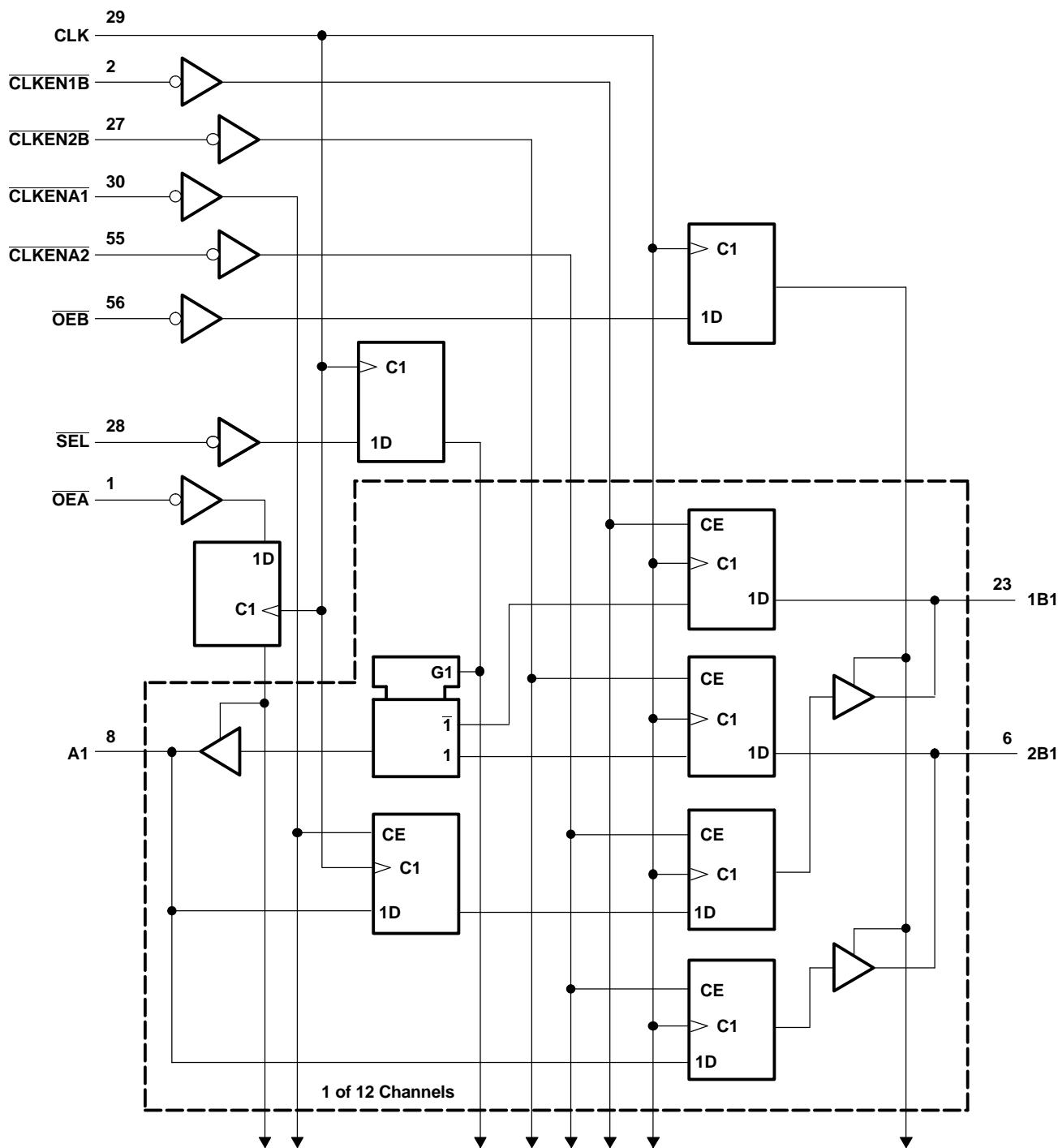
- (1) Output level before the indicated steady-state input conditions were established

**SN74ALVCH16226B**  
**12-BIT TO 24-BIT REGISTERED BUS EXCHANGER**  
**WITH 3-STATE OUTPUTS**

SCES018L—AUGUST 1995—REVISED SEPTEMBER 2004

 **TEXAS**  
**INSTRUMENTS**  
[www.ti.com](http://www.ti.com)

**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers shown are for the DGG and DL packages.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	4.6	V
$V_I$	Input voltage range	Except I/O ports <sup>(2)</sup>	-0.5	4.6	V
		I/O ports <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	
$V_O$	Output voltage range <sup>(2)(3)</sup>		-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$		-50	mA
$I_O$	Continuous output current			$\pm 50$	mA
	Continuous current through each $V_{CC}$ or GND			$\pm 100$	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package		64	°C/W
		DL package		56	
		GQL/ZQL package		42	
$T_{stg}$	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V, maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**SN74ALVCH162268**  
**12-BIT TO 24-BIT REGISTERED BUS EXCHANGER**  
**WITH 3-STATE OUTPUTS**

SCES018L—AUGUST 1995—REVISED SEPTEMBER 2004

 **TEXAS**  
**INSTRUMENTS**  
[www.ti.com](http://www.ti.com)

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	1.65	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0.8	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current (A port)	$V_{CC} = 1.65 \text{ V}$	-4	mA
		$V_{CC} = 2.3 \text{ V}$	-12	
		$V_{CC} = 2.7 \text{ V}$	-12	
		$V_{CC} = 3 \text{ V}$	-24	
	High-level output current (B port)	$V_{CC} = 1.65 \text{ V}$	-2	
		$V_{CC} = 2.3 \text{ V}$	-6	
		$V_{CC} = 2.7 \text{ V}$	-8	
		$V_{CC} = 3 \text{ V}$	-12	
$I_{OL}$	Low-level output current (A port)	$V_{CC} = 1.65 \text{ V}$	4	mA
		$V_{CC} = 2.3 \text{ V}$	12	
		$V_{CC} = 2.7 \text{ V}$	12	
		$V_{CC} = 3 \text{ V}$	24	
	Low-level output current (B port)	$V_{CC} = 1.65 \text{ V}$	2	
		$V_{CC} = 2.3 \text{ V}$	6	
		$V_{CC} = 2.7 \text{ V}$	8	
		$V_{CC} = 3 \text{ V}$	12	
$\Delta t/\Delta V$	Input transition rise or fall rate		10	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

(1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	A port	I <sub>OH</sub> = -100 $\mu$ A	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2		V
		I <sub>OH</sub> = -4 mA	1.65 V	1.2		
		I <sub>OH</sub> = -6 mA	2.3 V	2		
			2.3 V	1.7		
		I <sub>OH</sub> = -12 mA	2.7 V	2.2		
			3 V	2.4		
	B port	I <sub>OH</sub> = -24 mA	3 V	2		
		I <sub>OH</sub> = -100 $\mu$ A	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2		
		I <sub>OH</sub> = -2 mA	1.65 V	1.2		
		I <sub>OH</sub> = -4 mA	2.3 V	1.9		
			2.3 V	1.7		
		I <sub>OH</sub> = -6 mA	3 V	2.4		
V <sub>OL</sub>	A port	I <sub>OL</sub> = -8 mA	2.7 V	2		V
		I <sub>OL</sub> = -12 mA	3 V	2		
		I <sub>OL</sub> = 100 $\mu$ A	1.65 V to 3.6 V	0.2		
		I <sub>OL</sub> = 4 mA	1.65 V	0.45		
		I <sub>OL</sub> = 6 mA	2.3 V	0.4		
			2.3 V	0.7		
	B port	I <sub>OL</sub> = 12 mA	2.7 V	0.4		
		I <sub>OL</sub> = 24 mA	3 V	0.55		
		I <sub>OL</sub> = 100 $\mu$ A	1.65 V to 3.6 V	0.2		
		I <sub>OL</sub> = 2 mA	1.65 V	0.45		
		I <sub>OL</sub> = 4 mA	2.3 V	0.4		
			2.3 V	0.55		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V		±5	$\mu$ A	
I <sub>I(hold)</sub>	V <sub>I</sub> = 0.58 V	1.65 V	25			$\mu$ A
			-25			
	V <sub>I</sub> = 1.07 V	2.3 V	45			
			-45			
	V <sub>I</sub> = 0.7 V	3 V	75			
			-75			
	V <sub>I</sub> = 1.7 V	3.6 V		±500		
I <sub>OZ</sub> <sup>(3)</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V		±10	$\mu$ A	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V		40	$\mu$ A	
$\Delta I_{CC}$	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V		750	$\mu$ A	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	3.5	pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	9	pF	

 (1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 (3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**SN74ALVCH162268**  
**12-BIT TO 24-BIT REGISTERED BUS EXCHANGER**  
**WITH 3-STATE OUTPUTS**

SCES018L—AUGUST 1995—REVISED SEPTEMBER 2004

 **TEXAS**  
**INSTRUMENTS**  
[www.ti.com](http://www.ti.com)

**TIMING REQUIREMENTS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		<b>UNIT</b>	
		MIN	MAX	MIN	MAX	MIN	MAX		
$f_{clock}$	Clock frequency			120			125	150	MHz
$t_w$	Pulse duration, CLK high or low			3.3			3.3	3.3	ns
$t_{su}$	A data before $CLK\uparrow$	4.5			4			3.4	ns
	B data before $CLK\uparrow$	0.8			1.2			1	
	$\overline{SEL}$ before $CLK\uparrow$	1.4			1.6			1.3	
	$\overline{CLKENA1}$ or $\overline{CLKENA2}$ before $CLK\uparrow$	3.6			3.4			2.8	
	$\overline{CLKEN1B}$ or $\overline{CLKEN2B}$ before $CLK\uparrow$	3.2			3			2.5	
	$\overline{OE}$ before $CLK\uparrow$	4.2			3.9			3.2	
$t_h$	A data after $CLK\uparrow$	0			0			0.2	ns
	B data after $CLK\uparrow$	1.3			1.2			1.3	
	$\overline{SEL}$ after $CLK\uparrow$	1			1			1	
	$\overline{CLKENA1}$ or $\overline{CLKENA2}$ after $CLK\uparrow$	0.1			0.1			0.4	
	$\overline{CLKEN1B}$ or $\overline{CLKEN2B}$ after $CLK\uparrow$	0.1			0			0.5	
	$\overline{OE}$ after $CLK\uparrow$	0			0			0.2	

**SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

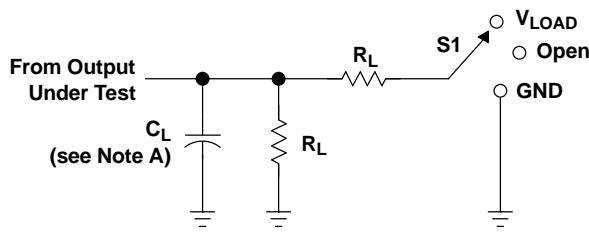
<b>PARAMETER</b>	<b>FROM (INPUT)</b>	<b>TO (OUTPUT)</b>	$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			
			TYP	MIN	MAX	MIN	MAX	MIN	MAX		
$f_{max}$				120			125			150	MHz
$t_{pd}$	CLK	B	8	1.6	6.1			5.9	1.8	5.4	ns
		A (1B)	8	1.6	5.8			5.4	1.7	4.8	
		A (2B)	8	1.6	5.8			5.3	1.8	4.8	
		A ( $\overline{SEL}$ )	11	2.5	7.3			6.5	2.4	5.8	
$t_{en}$	CLK	B	12	2.7	7.2			6.8	2.6	6.1	ns
		A	9	2	6.2			5.6	1.8	5.1	
$t_{dis}$	CLK	B	10	2.8	7.2			6.1	2.5	5.9	ns
		A	9	2	6.5			5.4	2.1	5	

**OPERATING CHARACTERISTICS**

$T_A = 25^\circ\text{C}$

	<b>PARAMETER</b>		<b>TEST CONDITIONS</b>	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 3.3 \text{ V}$	<b>UNIT</b>
				TYP	TYP	
$C_{pd}$	Power dissipation capacitance	Outputs enabled	$C_L = 50 \text{ pF}$ , $f = 10 \text{ MHz}$	87	120	pF
		Outputs disabled		80.5	118	

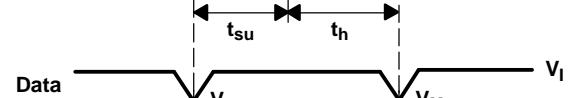
## PARAMETER MEASUREMENT INFORMATION



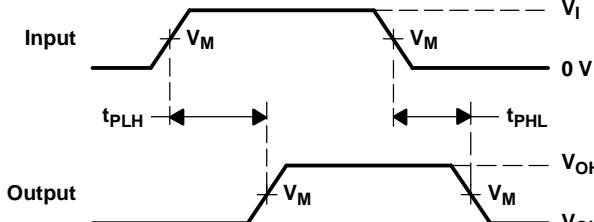
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT

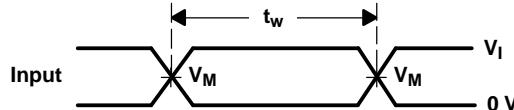
$V_{CC}$	INPUT		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_\Delta$
	$V_I$	$t_r/t_f$					
$1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



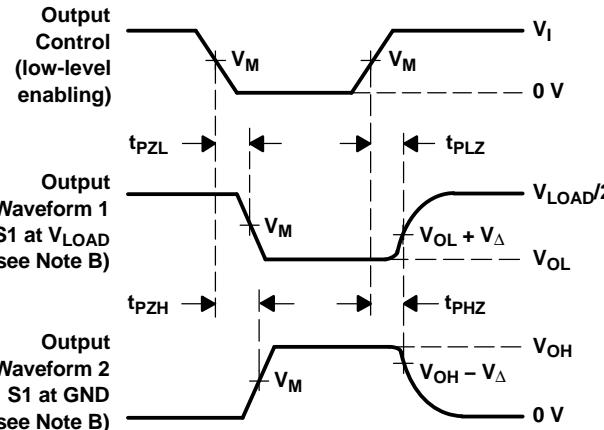
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74ALVCH162268DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162268	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
74ALVCH162268GRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162268	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
74ALVCH162268GRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162268	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74ALVCH162268DGGR	OBsolete	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
SN74ALVCH162268DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162268	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74ALVCH162268GR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162268	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and



www.ti.com

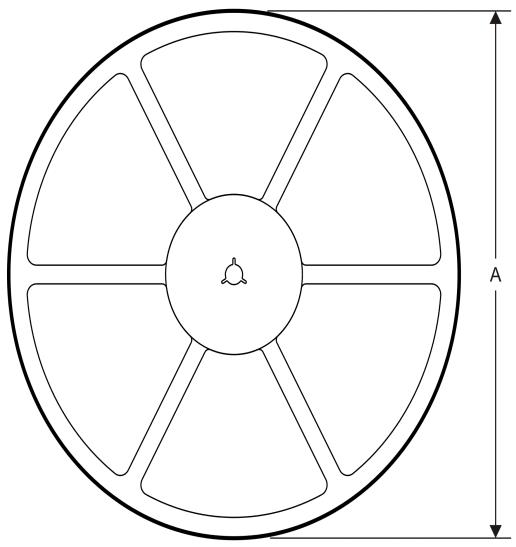
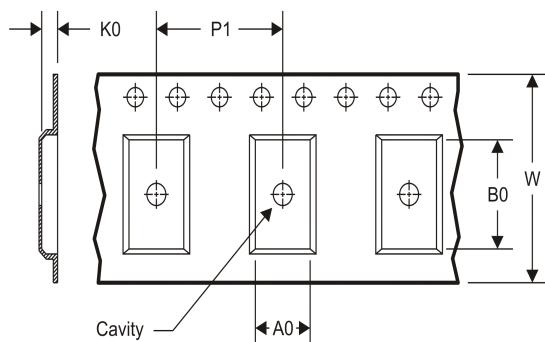
## PACKAGE OPTION ADDENDUM

11-Apr-2013

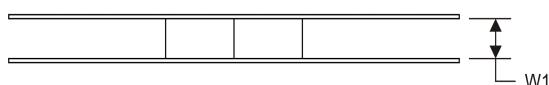
---

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers


**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH162268GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

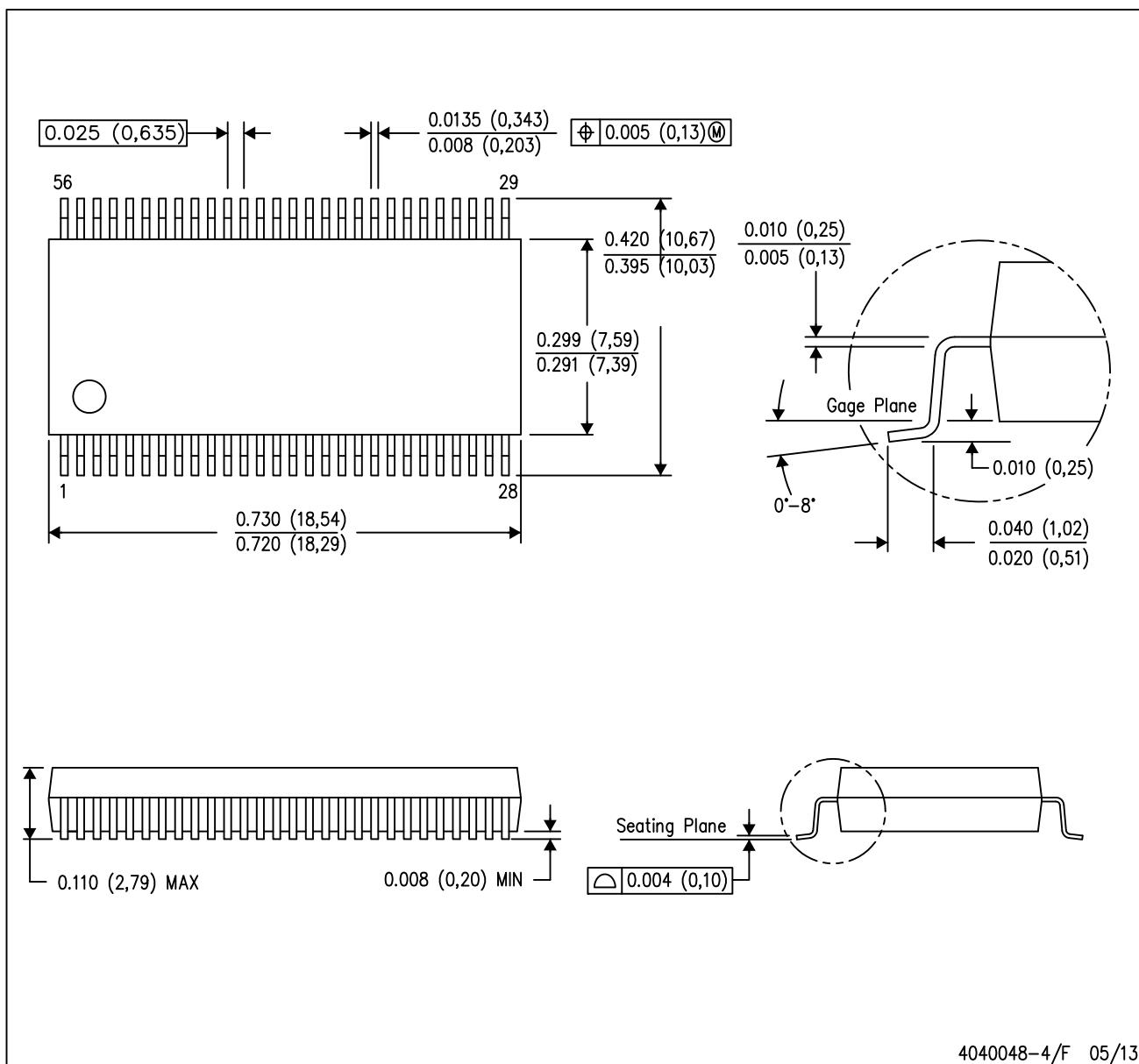
**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH162268GR	TSSOP	DGG	56	2000	367.0	367.0	45.0

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

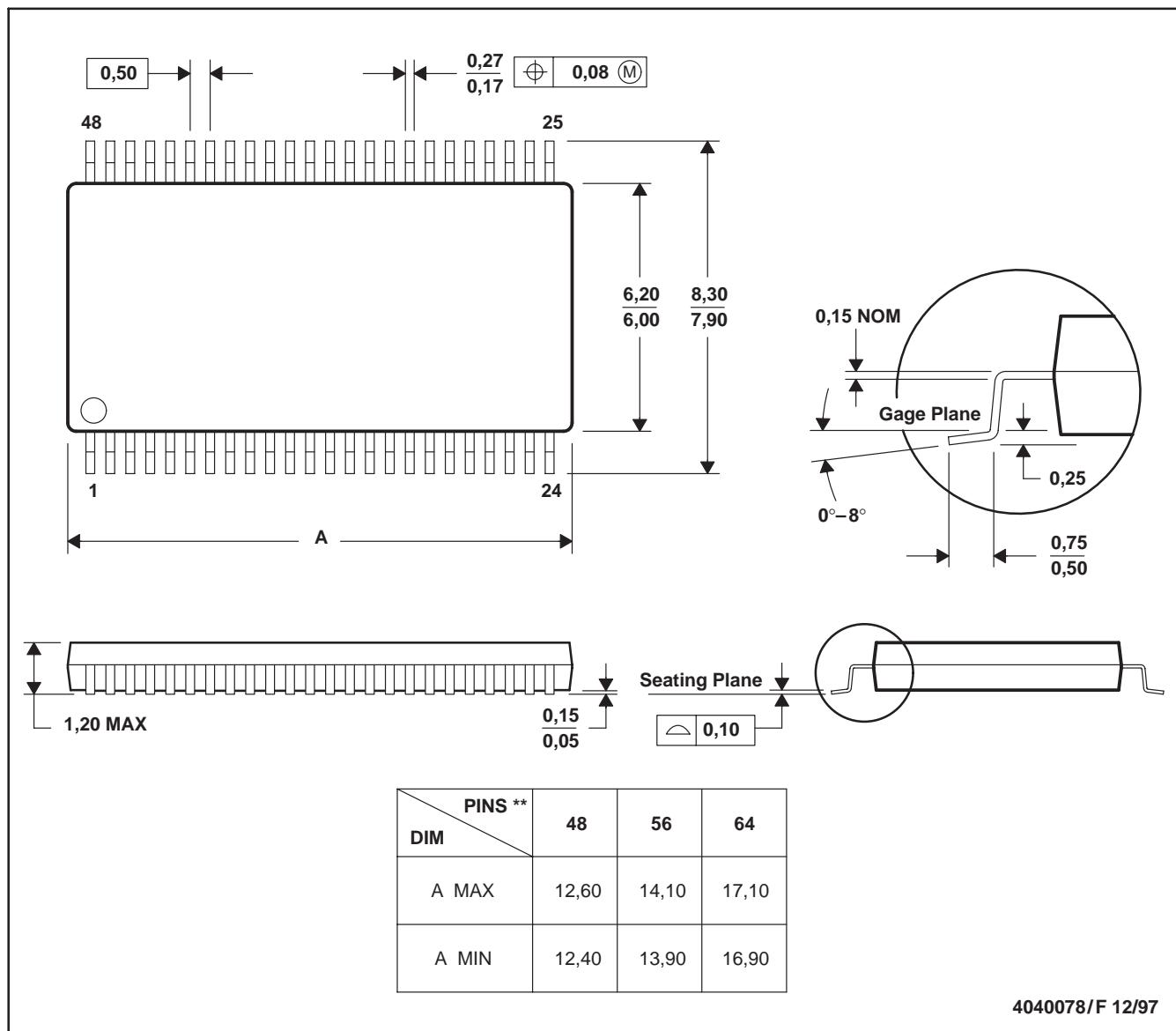
- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	Applications
Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>
	<b>TI E2E Community</b>
	<a href="http://e2e.ti.com">e2e.ti.com</a>