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How to Connect Multiple S/T or U ISDN Interfaces to a QUICC32 - *rev 0.6*

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INTRODUCTION

The MC145574 (S/T interface) and MC145572 (U interface) can be gluelessly interfaced to the members of the 68302 family, using the IDL or GCI protocols, to become low cost active ISDN terminals for one basic rate connection.

For applications that need to support more than one basic rate interface (LAN/WAN Bridges, PBX, line cards or Multiple Line Terminal Adaptors), a system solution using multiple MC145574 (S/T Interface) or MC145572 (U Interface) can be easily architectured around a QUICC32 (MC68MH360).

The QUICC32 and the QMC (QUICC's Multi-channel Controller) protocol are very useful for such ISDN applications when several logical channels are transferred over the same physical medium.

This application note shows how multiple MC145574 (S/T Interface) or MC145572 (U Interface) can be connected to a QUICC32. The application note describes the level 1 connections and explains the data flow through the devices.

No software issues will be addressed by this application note.

THE QMC PROTOCOL

The QMC protocol implemented on the QUICC32, based upon the IDL bus, generates a TDM (Time Division Multiplexed) bus with programmable timeslots for each ISDN interface.

Assume the creation of a 2 Mbit TDM with 32 timeslots each carrying 8 consecutive bits to form multiple 64 kbit/s channels. This is almost the same as a CEPT/E1 link.

Timeslot zero, TS0, is dedicated to the first B1-channel. TS1 to the first B2-channel and TS2 to the first D-channel. The D-channel has 8 bits reserved on the TDM link although only 2 are used. The remaining 6 bits are masked in the QMC Time Slot Assignment Table.

The reason for this is that the QMC microcode needs to process data on a 8-bits boundary to do a correct delineation between channels.

The second B1-channel is routed to TS3 and thus the whole TDM built up.

Up to 10 BRI's can be connected this way, each BRI using 3 timeslots of the TDM line allowing a maximum of 32 channels/timeslots.

Thanks to their on-chip time-slot assigner, the S/T and U interfaces, in IDL2 mode, can easily match the QMC bus structure: Both devices can be connected to a 2.048MHz IDL2 bus, and route the B1-channel, B2-channel and D-channel to any timeslot of that IDL2 bus.

Figure 1 shows the IDL2 bus configured to match the QMC protocol.

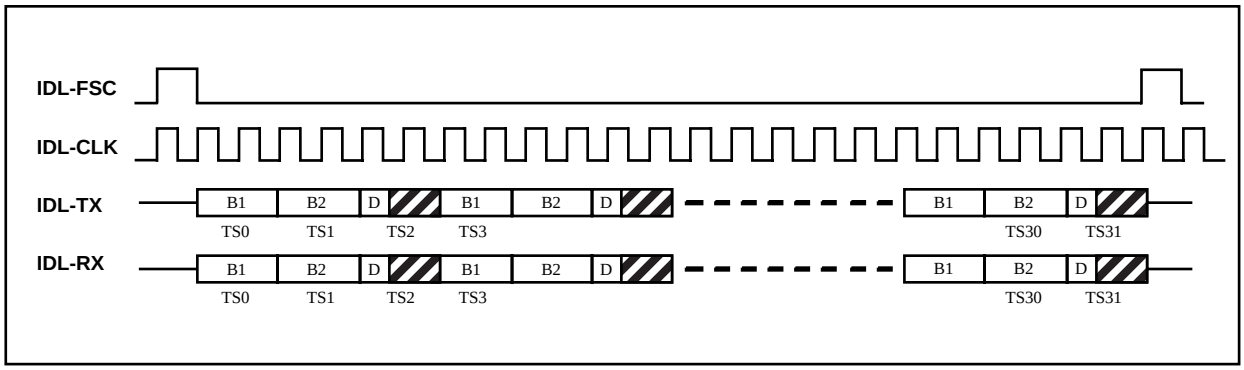

Figure 1: IDL2 bus structure for a connection to the QMC bus.

THE CONTROL AND STATUS INFORMATION

The control and status information is transferred between the QUICC32 and the ISDN interfaces via the SPI port in a out-of-band signalling method.

The MC145572 also has the option of an 8 bit parallel port for control and status transfer. In this case, the U interfaces could all be connected to the processor bus instead.

Figure 2a shows the connection between the QUICC32 and an S/T interface.

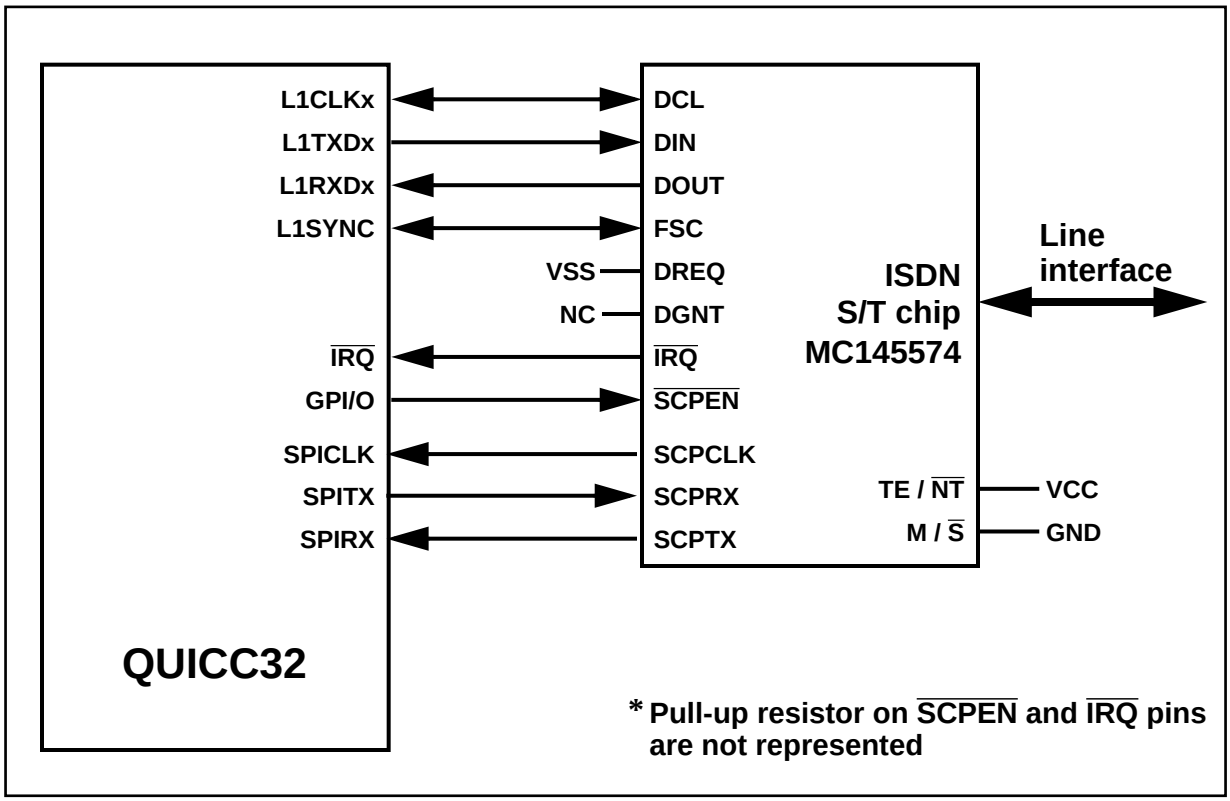

Figure 2a: IDL and SCP connections between the QUICC32 and the S/T interface

The QUICC32 is always a slave on the IDL/QCM bus (the DCL and FSC signals are inputs).

As it is explained in the next chapter, for that specific application the S/T interface must be configured in slave mode on the IDL bus and therefore the DCL and FSC signal need to be provided to both the QUICC32 and the S/T, from external circuitry.

The D-channel request/grant function is not required for this application, since it is assumed that each S/T will be directly connected to the NT1 (point to point configuration with only 1 TE connected to 1 NT).

The DGNT pin is left unconnected and the DREQ can be directly connected to VSS. As there is no contention on the D-channel, the «D-channel contention procedure» of the MC145574 should be disabled, by setting the bit 6 on the register BR7.

Figure 2b shows the connection between the QUICC32 and a U interface.

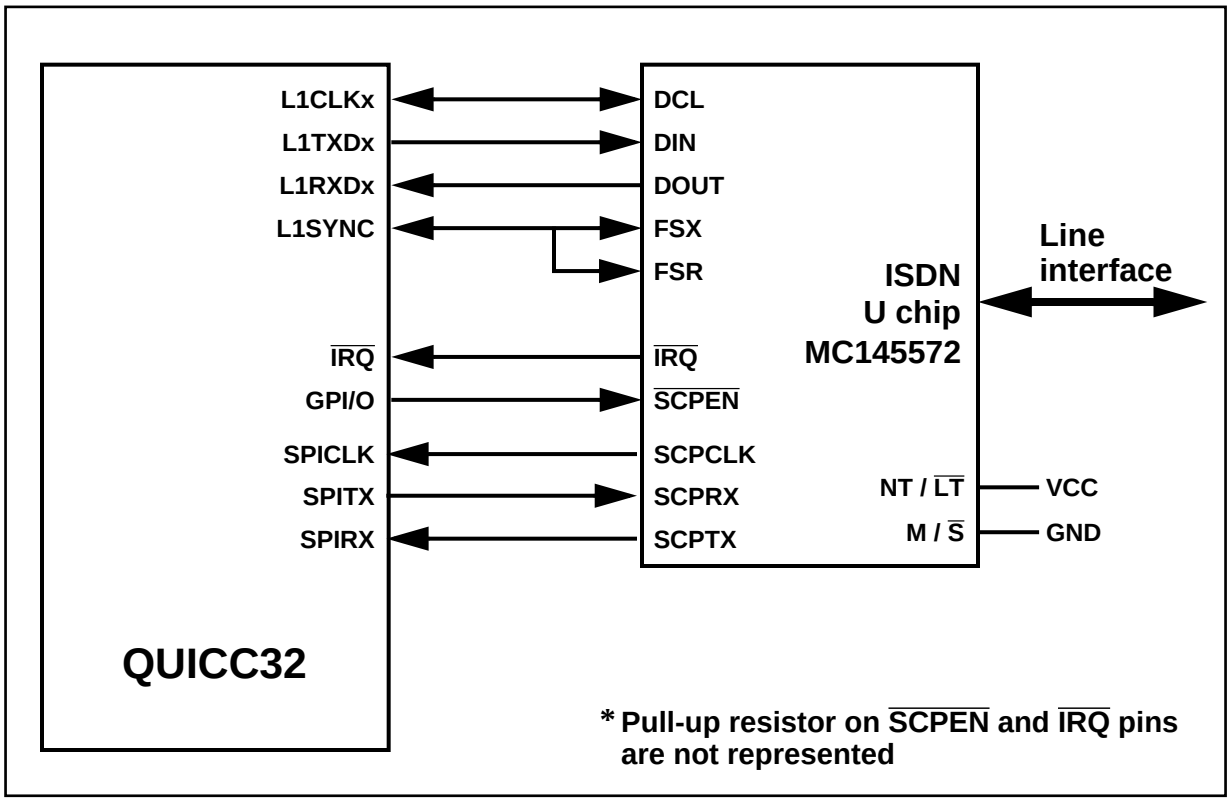

Figure 2b: IDL and SCP connections between the QUICC32 and the U interface

Likewise for the S/T interface example, the U interface must be configured in slave mode and therefore the DCL and FSC signals need to be provided to both the QUICC32 and the U interface.

In slave mode, the FSX and FSR pins of the MC145572 must be tied together.

There are no DREQ/DGRANT signals on the U interface.

DATA CLOCK (DCL) & FRAME SYNC (FSC) GENERATION:

The main consideration when connecting multiple interfaces to the same physical medium, is the clock and frame sync generation.

As stated earlier, the QUICC32 does not provide DCL and FSC. The U or S/T interface could be configured in Master Mode on the IDL bus and generate both DCL and FSC synchronised to the signal coming from the line interface.

In the case of a multiple interface architecture, and in order to have all the B and D channels synchronised on the same TDM bus, only one S/T or U interface should be configured as master and provide DCL and FSC to the QUICC32 and to all the other interfaces.

However, this concept works only if we can guarantee that the S/T or U interface configured as master is constantly in activated mode. Once Deactivated, the U or S/T cannot generate DCL and FSC synchronized with the network. As we can not have that guarantee, it is therefore necessary to configure all the transceivers in slave mode and to find another way to generate DCL and FSC.

DCL and FSC need to be synchronised to the network and cannot be derived from an independent source (e.g. crystal or oscillator). However, the S/T and U interfaces, even when they are configured as slave on the IDL bus, provide a way to generate these signals as it is explained in the following paragraphs.

1. MC145574 S/T Interface:

To facilitate the generation of the timing signals required by the slave IDL interface, a pin is provided in the S/T interface. That pin (TCLK) will output a clock synchronised to the received INFO transmitted by the NT. That clock is output only when the S/T interface is activated and when the DCL and FSC signals are present (both conditions are required simultaneousely). This TCLK pin can be used to provide network timing. Its frequency is selectable via the SCP.

The TCLK pin of the MC145574 is enabled by setting the bit 5 on the register OR7. Time frequency can be selected on the registers BR13 (bit 5) and BR7 (bit 2).

BR13(5)	BR7(2)	TCLK
0	0	2.56 MHz
0	1	2.048 MHz
1	0	1.536 MHz
1	1	512 KHz

The TCLK pin configured as a 2.048MHz clock, can be used as the DCL for the IDL bus.

Divided by 256, that signal can also be used to generate the 8kHz frame sync FSC. As that frame sync must have a pulse width situated between 1 DCL as a minimum, and 8 DCL as a maximum, some logic need to be added after the divider in order to generate a signal with a correct duty cycle.

Figure 3a and figure 3b show respectively a schematic and a timing diagram for the logic which could be used to generate a 8kHz FSC with a 1DCL width pulse, from a 2.048MHz clock (TCLK).

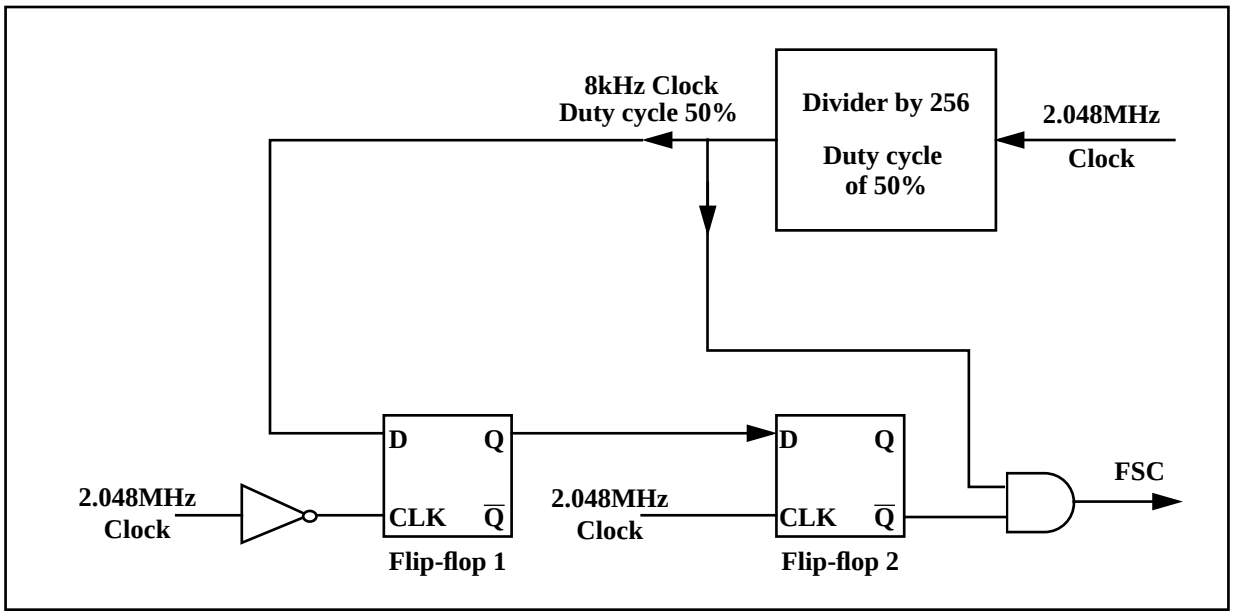

Figure 3a: FSC generation from a 2.048 MHz clock - Block diagram

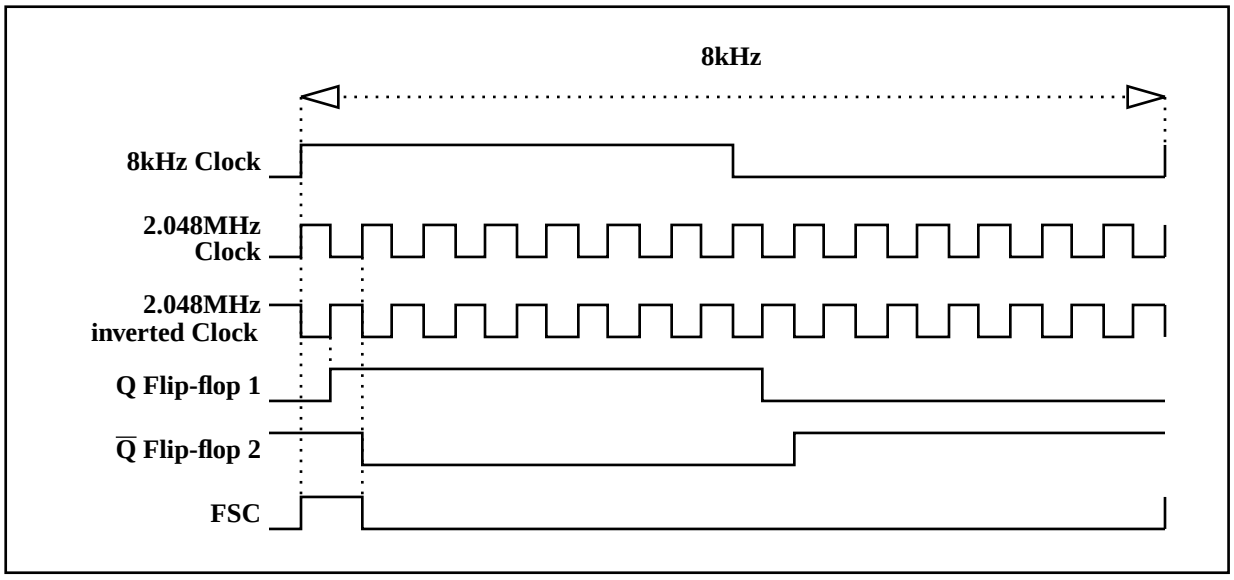

Figure 3b: FSC generation from a 2.048 MHz clock - Timing

Elastic buffers are included in the S/T interface, to allow it to operate with any phase relationship between the IDL frame sync and the network. These buffers allow the frame sync to wander with respect to the network up to 60µs peak-peak and exceed the requirements of Q.502 which states that wander up to 18µs peak-peak may arise over a 24 hours period.

Figure 4 is a block diagram showing the connection between 4 S/T interfaces and the QUICC32. The diagram would be the same for up to 10 S/T interfaces.

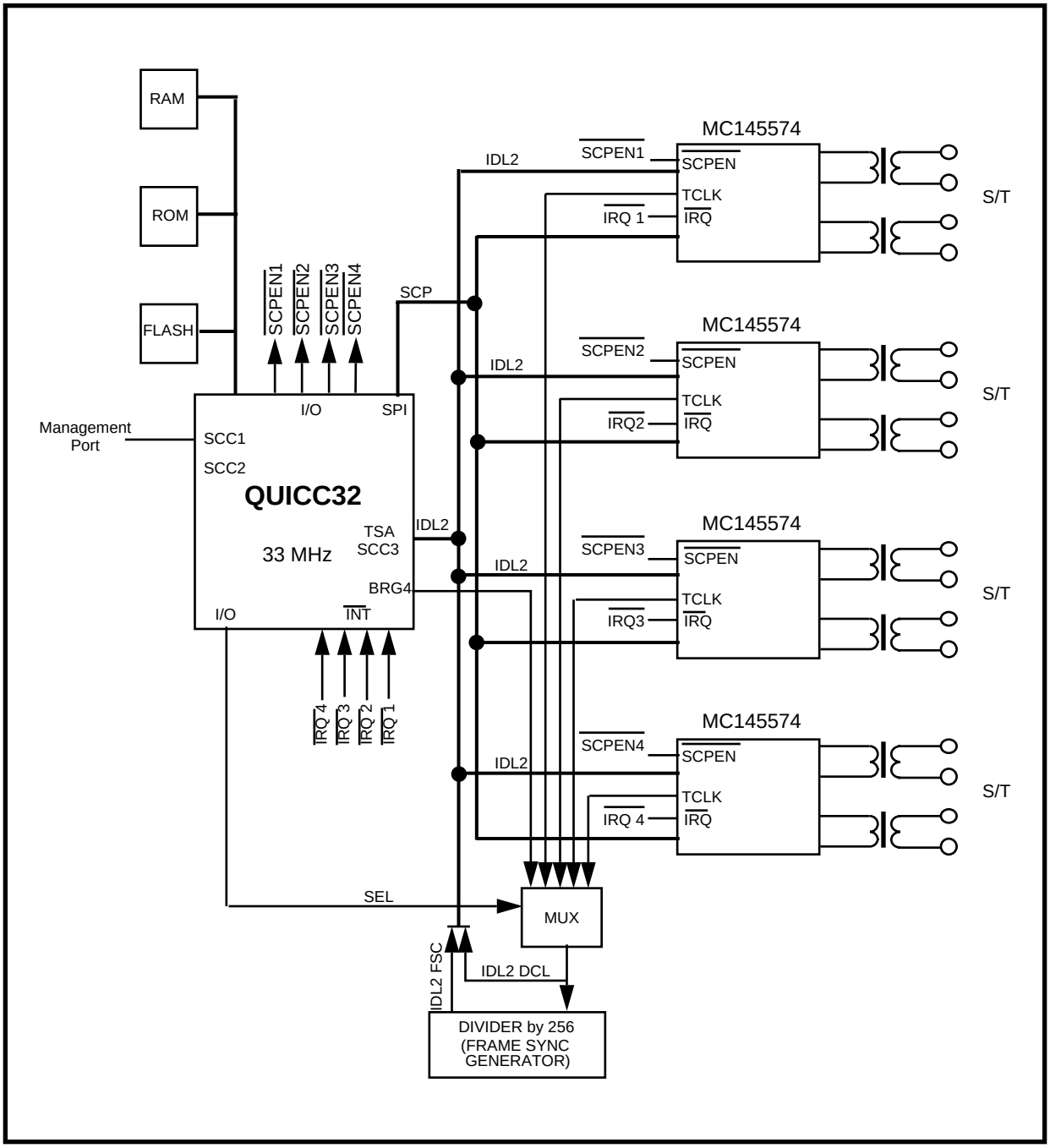

Figure 4: Connection between 4 S/T interfaces and the QUICC32

Activation procedure:

When none of the S/T transceivers are activated, no TCLK clock is generated. Once the first S/T is being activated, it will try to generate the TCLK signal. But in order to output that signal the S/T requires a DCL and a FSC.

To allow the generation of that TCLK signal, pseudo DCL and FSC signals could be generated using one of the Baud Rate Generator (BRG) of the QUICC32. The BRG can output a clock, which frequency is a division of the system clock of the QUICC32. The divider factor should be chosen so that the BRG frequency is close to 2048MHz. That clock should be feed to the Divider-by-256 circuitry previously used with the exact 2048MHz clock, to allow the generation of a pseudo DCL and a pseudo FSC.

A multiplexer commanded by the QUICC32, is required to select either the BRG pin or the TCLK pins of the S/T, to be the clock master to generate the DCL and FSC signals.

Then, when no S/T is activated the QUICC32 selects the BRG to be the clock master and the S/T interface receives the pseudo signals DCL and FSC (these 2 signals are not synchronized to the network but are not used to sample data!).

When the first S/T is being activated, it will be able to generate the TCLK signal (as it receives DCL & FSC). That S/T interface send an interrupt to the QUICC32 (IRQ3 - register NR3 bit 3 - which means that INFO2 has been received) indicating that the activation process has begun. The QUICC32 has then the ability to select, through the multiplexer, the TCLK pin of that MC145574 to be the timing master.

As shown in figure 5a & 5b the TCLK signal is present before the interruption, and there is at least 750µs between the IRQ and the received INFO4. So the QUICC32 has 750µs to react to the IRQ and to select, through the multiplexer, another clock master.

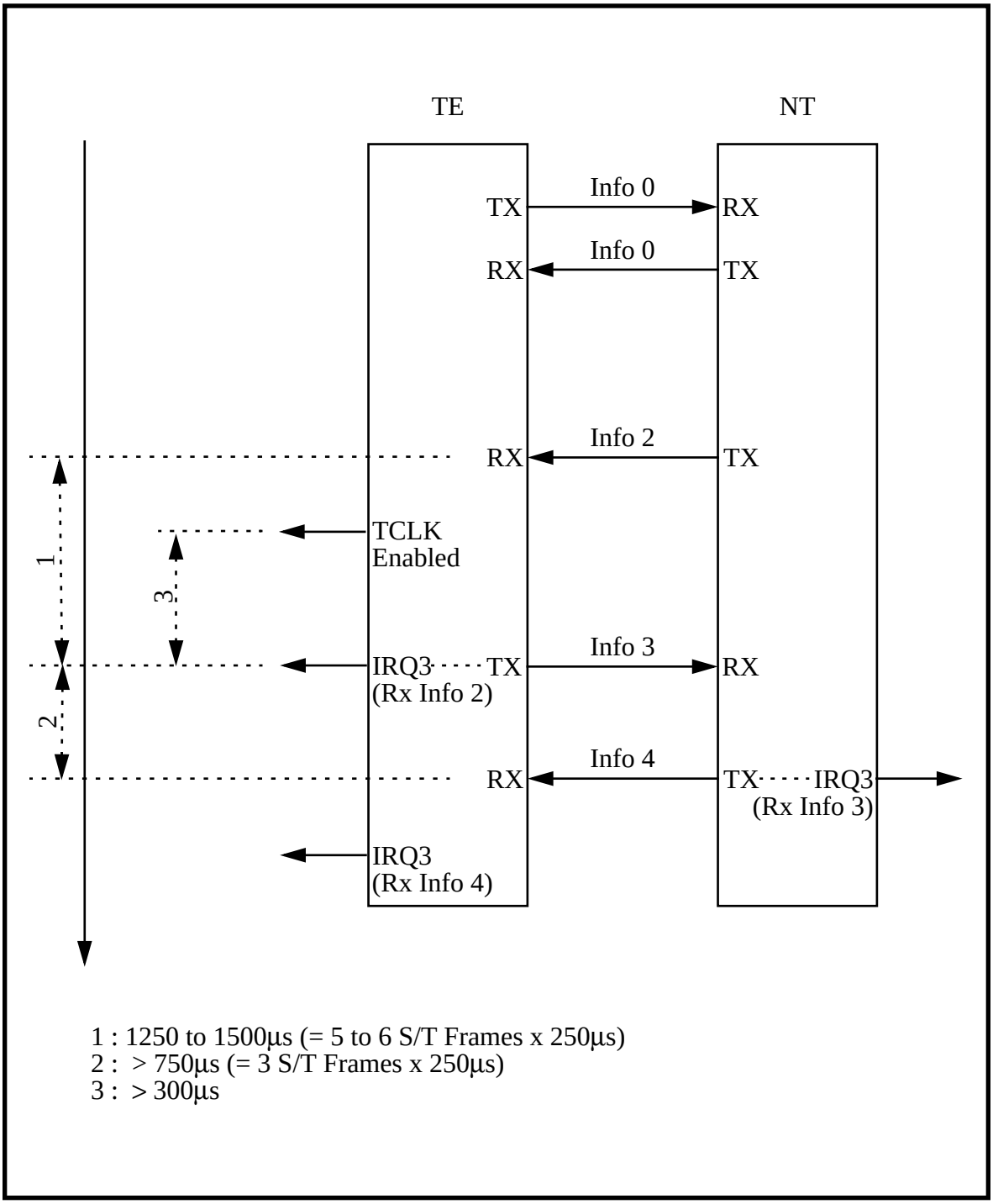

Figure 5a: Timing Diagram for an Activation Initiated by the NT

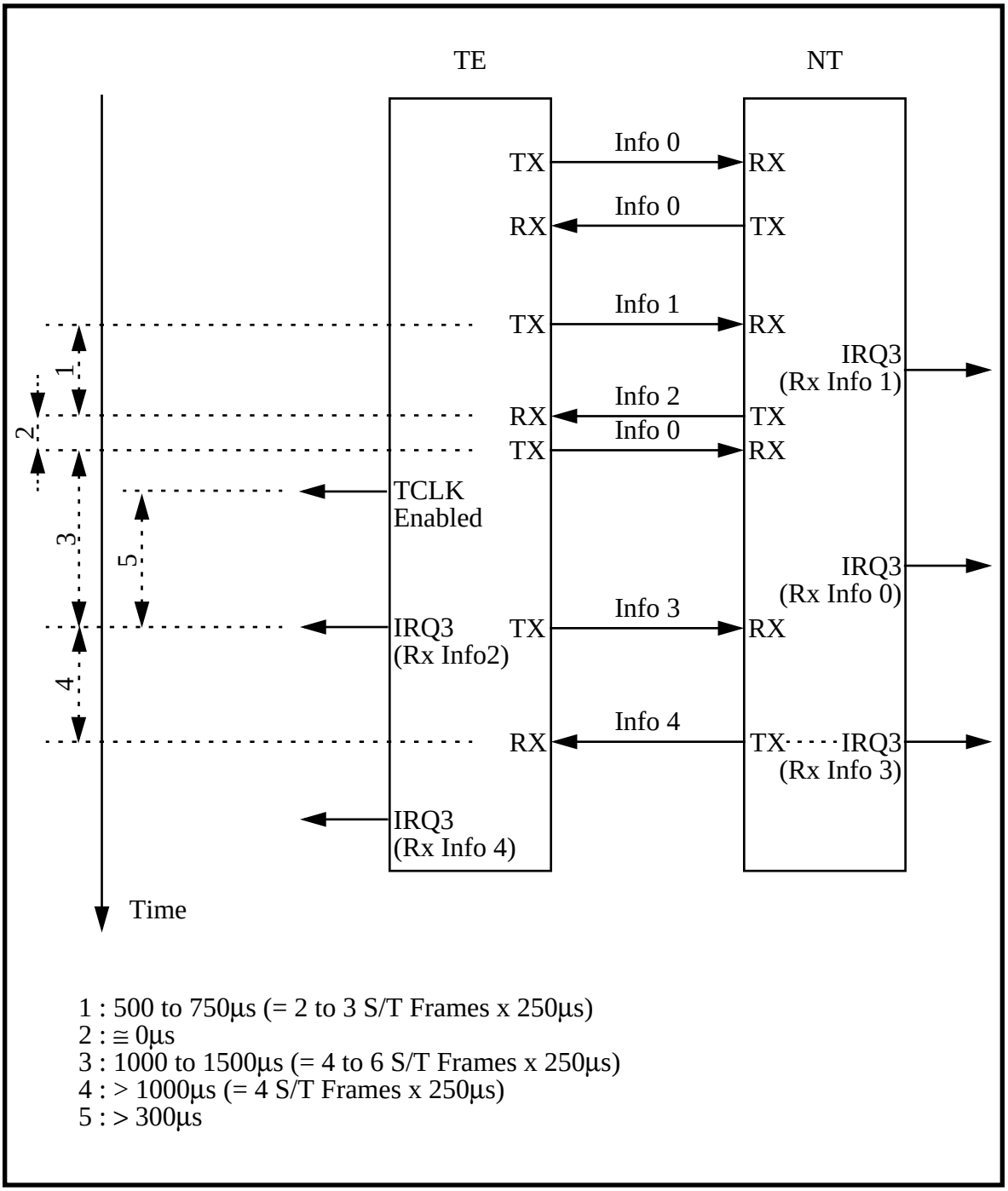

Figure 5b: Timing Diagram for an Activation Initiated by the TE

Desactivation procedure:

When the S/T interface whose TCLK is the timing master (selected on the multiplexer) is deactivated, the QUICC32 receives an interrupt indicating the deactivation status (IRQ3 - register

NR3 bit 3 - which means that INFO0 has been received). Then, if none of the other S/T are activated, the QUICC32 can select the BRG to be the clock master. If one (or more) S/T is activated, its TCLK pin must be selected to become the clock master.

As shown in figure 6 the TCLK signal is disabled about 72.8µs after the interruption. Therefore, the QUICC32 has 72.8µs to react to the IRQ and to select, through the multiplexer, another clock master.

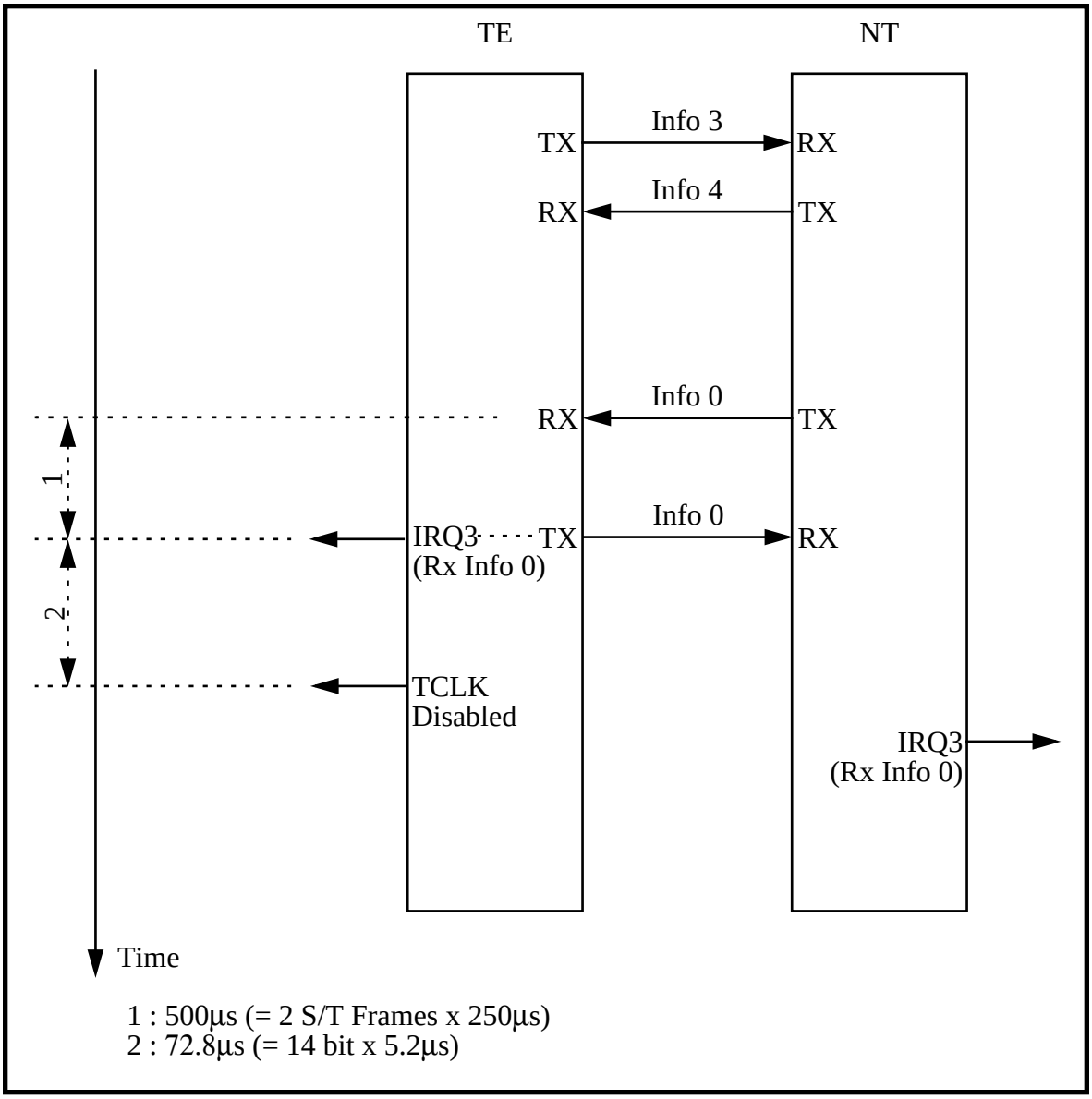

Figure 6: Timing Diagram for a Deactivation (Always Initiated by the NT)

2. MC145572 U Interface:

A pin which can output a clock synchronised to the network timing is also provided in the U interface (FREQREF pin).

That 2.048MHz clock (the frequency is not selectable) is enabled by setting bit 4 of OR8 in the MC145572 Register set.

The way the FREQREF pin operates is different than for the TCLK pin of the S/T interface.

When enabled, the FREQREF pin outputs the 2.048MHz clock, whatever the activation status of the U interface (but that clock is synchronize to the network only when the U interface is activated). That pin does not require the DCL & FSC signals, to be able to generate the clock.

As for the S/T interface, the FREQREF pin can be used as the DCL for the IDL bus. Divided by 256, that signal can also be used to generate the 8kHz frame sync FSC. The same kind of logic as for the S/T must be added to get a correct FSC duty cycle.

As for the S/T, elastic buffers are included to allow the U interface to operate with any phase relationship between the IDL frame sync and the network.

Figure 7 is a block diagram showing the connection between 4 U interfaces and the QUICC32. The diagram would be the same for up to 10 U interfaces.

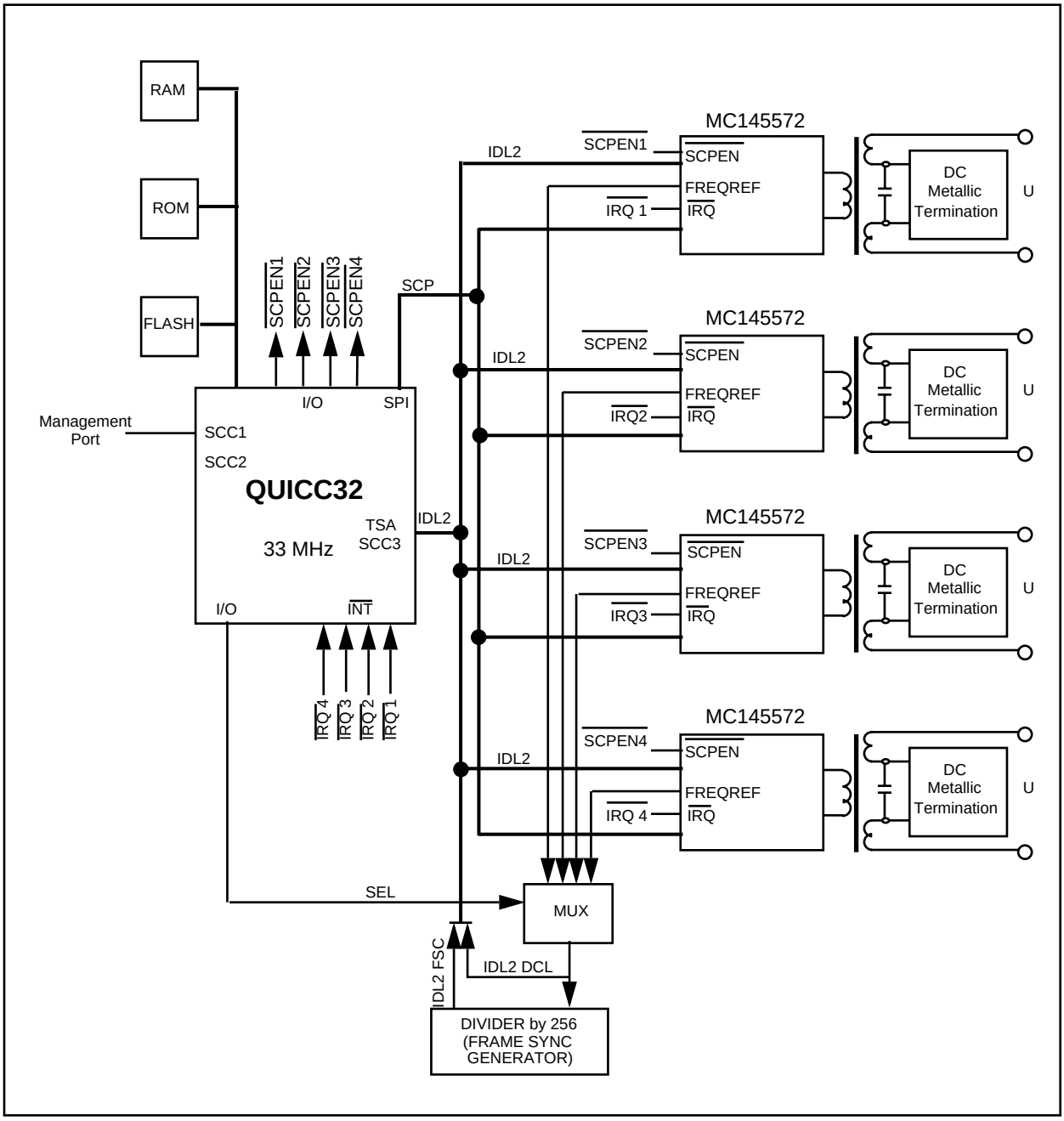

Figure 7: Connection between 4 U interfaces and the QUICC32

Activation procedure:

During the initialisation, the FREQREF pin of each U interface is enabled.

A multiplexer, commanded by the QUICC32, is used to select which U interface is the clock master.

When the first U interface is activated, its FREQREF pin becomes synchronised to the network. The MC145572 send an interrupt to the QUICC32 (IRQ1 - register NR3 bit 1 - which means that «uao = 1» has been received) indicating that the activation process has begun. Before responding to LT by «act = 1» (which will enable the data transfer), the QUICC32 has the ability to select, through the multiplexer, the FREQREF pin of that MC145572 to be the timing master.

As the QUICC32 has the initiative to enable the data transfer, there is no timing constraint to react to the interrupt.

Desactivation procedure:

According to the ANSI specification T1.601-1988, prior to deactivating, the LT should notify the NT of the pending deactivation by clearing the M4 channel dea bit towards the NT for at least three superframes. Then, deactivate the NT by sending a deactivation request.
The MC145572 has the ability to generate an interrupt after the reception of the third dea bit to 0, but also after the receiption of the second dea bit to 0.

When the U interface whose FREQREF is the timing master (selected on the multiplexer) is desactivated, the QUICC32 receives an interrupt indicating that the second «dea bit = 0» has been received. The QUICC32 has then the ability to select another activated U interface (if there is one), to be the clock master.The QUICC32 has 12ms (1 superframe) before receiving the next bit dea = 0, which will indicate the pending desactivation, and therefore 12ms to react to the interrupt.

If none of the U are activated, no change in the multiplex selection is required.

Below is a summary of the main features which need to be configured for each device:

S/T Interface Configuration:

- IDL2 with Time-Slot Assigner (TSA enabled in reg. OR6 bit 5 to bit 7; TSA selection in reg. OR0 to OR5)

- Slave mode (DCL & FSC are input) - (pin M/$\overline{S}$ to GND)

- TCLK enabled at 2.048MHz (reg. OR7, bit 5=1; reg. BR13, bit 5=0; reg. BR7, bit 2=1)

- «D-channel contention procedure» disabled (register BR7, bit 6=1)

U Interface Configuration:

- IDL2 with Time-Slot Assigner (TSA enabled in reg. OR6 bit 5 to bit 7; TSA selection in reg. OR0 to OR5)

- Slave mode (DCL & FSC are input) - (pin M/$\overline{S}$ to GND)

- FREQREF enabled at 2.048MHz (reg. OR8, bit 4=1)

QUICC32 Configuration:

- SCC3 using the QMC protocol for handling the different channels of the multiplexed IDL2 bus. (D-channels are HDLC encoded/decoded and B-channels can be configured for Transparent or HDLC framing)

- SCC1 can be configured for Ethernet , HDLC, Transparent or UART.

- SCC2 & SCC4 can be configured for HDLC, Transparent or UART.

- The SPI is connected to the SCP port of each S/T or U interface for handling configuration and control information.

- For the U interface the SPI/SCP connection can be replaced by a connection of the 8 bit parallel port of the U transceiver to the processor bus of the QUICC.

- One I/O pin can be dedicated for handling the SCPEN signal of each S/T or U

- One Interrupt pin can be dedicated for handling the IRQ signal of each S/T or U interface.

REFERENCES:

1. MC68360 Quad Integrated Communications Controller User's Manual, Motorola Inc. 1989.
2. MC68MH360 QUICC's Multi-channel Controller User's Manual, Motorola Inc. 1995.
3. MC145572 ISDN U-Interface Transceiver Advance Information, Motorola Inc. 1995.
4. MC145574 ISDN S/T-Interface Transceiver Advance Information, Motorola Inc. 1996.

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