IS 62C1024

128K X 8 LOW POWER CMOS STATIC RAM

PRELIMINARY
OCTOBER 1990

FEATURES

- Low active power- 75mW (Typical)
- **High speed access time-70, 85, 100ns (Max.)**
- Low standby power-10µW (Typical) CMOS standby (L-version)
- Output enable and two chip enable inputs for ease in applications
- Fully static operation-no clock or refresh required
- TTL compatible inputs and outputs
- 2V data retention for battery backup (L-version)
- Single 5V (±10%) power supply

DESCRIPTION

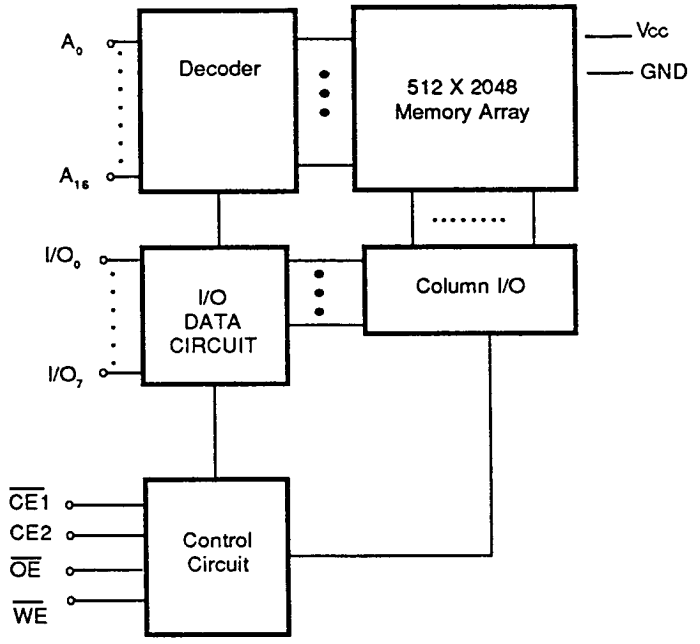
The ISSI IS62C1024 is a high speed, low power, 131,072- word by 8- bit CMOS static RAM. It is fabricated using ISSI's high performance CMOS double metal technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE1}$ is high or CE2 is low (de-select), the device assumes a standby mode at which the power dissipation can be reduced down to 10µW (typical) at CMOS input levels.

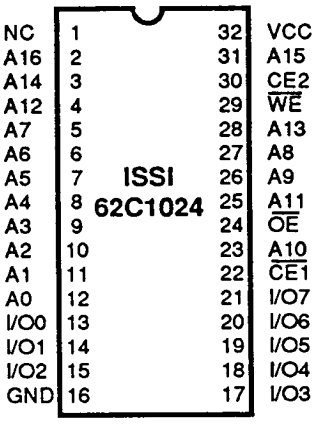
Easy memory expansion is provided by using two Chip Enable Inputs, $\overline{CE1}$ and CE2.The active low Write Enable controls both writing and reading of the memory.

The IS62C1024 is supplied in a 32 pin DIP package.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP

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ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC output Current (low)	20	mA

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to 70°C	5V ±10%
Industrial	-40°C to 85°C	5V ±10%

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics over Operating Range

Symbol	Description	Test Conditions	Standard		L-version		Units
			MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output High Voltage	V_{CC} = MIN., I_{OH} = -1.0mA	2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = MIN., I_{OL} = 2.1 mA		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	6.0	2.2	6.0	V
V_{IL}	Input Low Voltage (3)		-0.3	0.8	-0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	-2	2	-2	2	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	-2	2	-2	2	µA
I_{OS}	Output Short Circuit Current (1)	V_{CC} = MAX., V_{OUT} = GND		-100		-100	mA
I_{CC_1}	Vcc Operating Supply Current	V_{CC} = MAX., IOUT = 0mA, f = 0, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}		35		35	mA
I_{CC_2}	Vcc Dynamic Operating Supply Current	V_{CC} = MAX., IOUT = 0 mA, f = $f_{MAX.}$, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}		70		70	mA
I_{SB_1}	TTL Standby Current (TTL Inputs)	V_{CC} = MAX., V_{IN} = V_{IH} OR V_{IL}, $\overline{CE1}$ ≥ V_{IH} CE2 ≥ V_{IH}, or CE2 ≤ V_{IL}, f = 0		3		3	mA
I_{SB_2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE1}$ ≥ Vcc -0.2V CE2 ≤ 0.2V V_{IN} ≥ Vcc -0.2V, OR V_{IN} ≤ 0.2V, f = 0		2		0.1	mA

Capacitance (2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, F =1MHz Vcc = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested initially and after any design or process changes that may affect these parameters.
3. V_{IL} = -3.0V for pulse width less than 30ns.

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE_1}$	CE_2	$\overline{OE}$	I/O OPERATION	V_{CC} CURRENT
Not Selected (Power Down)	X	H	X	X	High Z	I_{SB_1}, I_{SB_2}
	X	X	L	X	High Z	I_{SB_1}, I_{SB_2}
Output Disabled	H	L	H	H	High Z	I_{CC_1},I_{CC_2}
Read	H	L	H	L	DOUT	I_{CC_1},I_{CC_2}
Write	L	L	H	X	DIN	I_{CC_1},I_{CC_2}

Switching Characteristics Over Operating Range (1)

Parameters	Description	IS62C1024-70 IS62C1024-L70		IS62C1024-85 IS62C1024-L85		IS62C1024-100 IS62C1024-L100		Units
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE								
tRC	Read Cycle Time	70		85		100		ns
tAA	Address Access Time		70		85		100	ns
tOHA	Output Hold Time	10		10		10		ns
tACE1	$\overline{CE1}$ Access Time		70		85		100	ns
tACE2	CE2 Access Time		70		85		100	ns
tDOE	$\overline{OE}$ Access Time		35		45		50	ns
tLZOE	$\overline{OE}$ to Low Z Output	5		5		5		ns
tHZOE(2)	$\overline{OE}$ to High Z Output	0	25	0	30	0	35	ns
tLZCE1	$\overline{CE1}$ to Low Z Output	10		10		10		ns
tLZCE2	CE2 to Low Z Output	10		10		10		ns
tHZCE	$\overline{CE1}$/CE2 to High Z Output	0	25	0	30	0	35	ns
tPU	$\overline{CE1}$ or CE2 to Power Up	0		0		0		ns
tPD	$\overline{CE1}$ or CE2 to Power Down		50		50		50	ns
WRITE CYCLE (3)								
tWC	Write Cycle Time	70		85		100		ns
tSCE1	$\overline{CE1}$ to Write End	60		75		90		ns
tSCE2	CE2 to Write End	60		75		90		ns
tAW	Address Set-up Time to Write End	60		75		90		ns
tHA	Address Hold to Write End	0		0		0		ns
tSA	Address Set-up Time	0		0		0		ns
tPWE (4)	$\overline{WE}$ Pulse Width	55		65		75		ns
tSD	Data Set-up to Write End	30		35		40		ns
tHD	Data hold from Write End	0		0		0		ns
tHZWE (2)	$\overline{WE}$ Low to High-Z Outputs	0	25	0	30	0	35	ns
tLZWE	$\overline{WE}$ High to Low-Z Output	5		5		5		ns

Notes:

1. Test conditions assume signal transition times of 5ns or less, timing reference levels of 1.5V, Input pulse levels of 0.8V to 2.4V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500mV from steady state voltage.
3. The internal write time is defined by the overlap of $\overline{CE1}$ low, CE2 high and $\overline{WE}$ low. All signals must be in valid states to initiate a Write, but anyone can go inactive to terminate the Write. The Data input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. Tested with $\overline{OE}$ high.
5. $\overline{WE}$ is high for a Read Cycle.
6. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$ = VIL, CE2 = VIH.
7. Address is valid prior to or coincident with $\overline{CE1}$ Low and CE2 High transitions.
8. I/O will assume the High-Z state if $\overline{OE}$≥VIH.

AC TEST CONDITIONS

Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing and Reference Level	1.5V

AC TEST LOADS AND WAVEFORMS

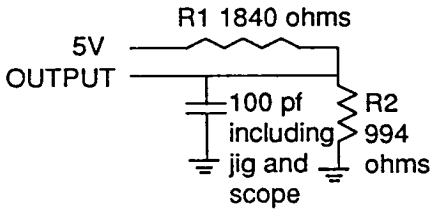


Figure 1a

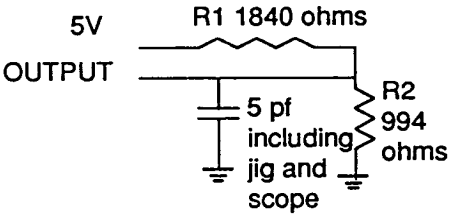
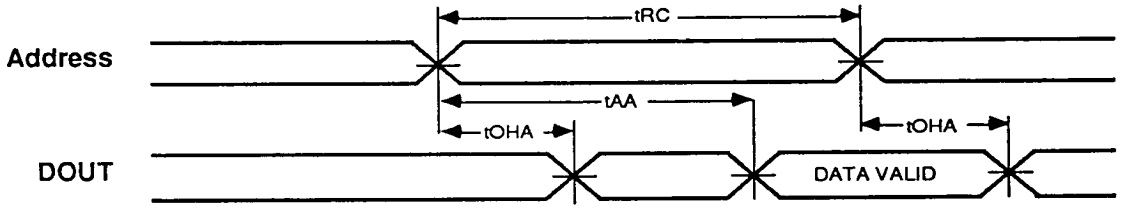
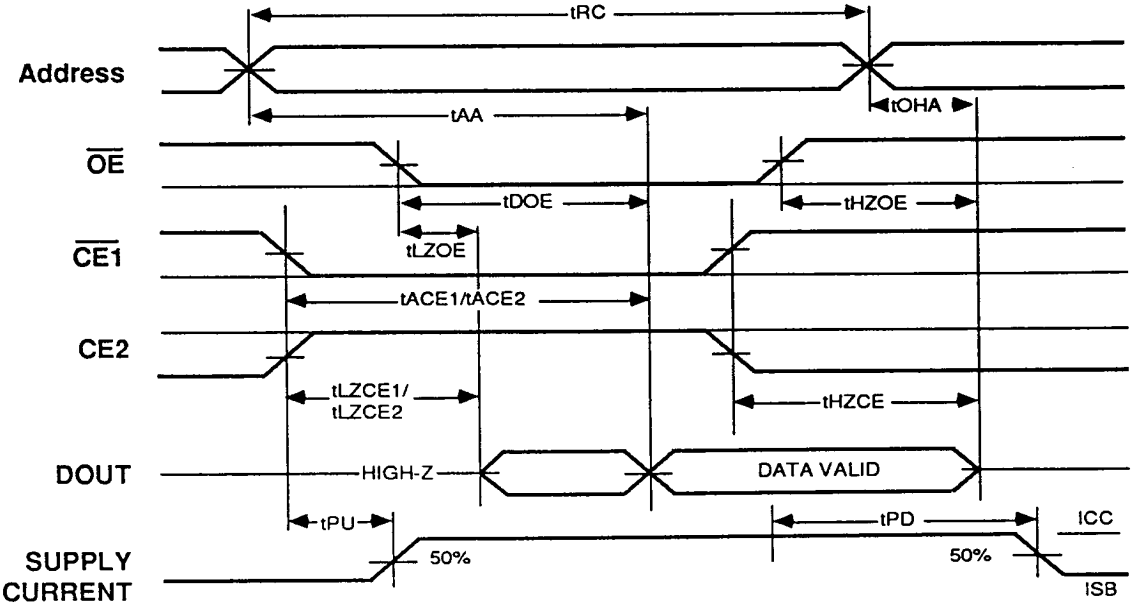


Figure 1b

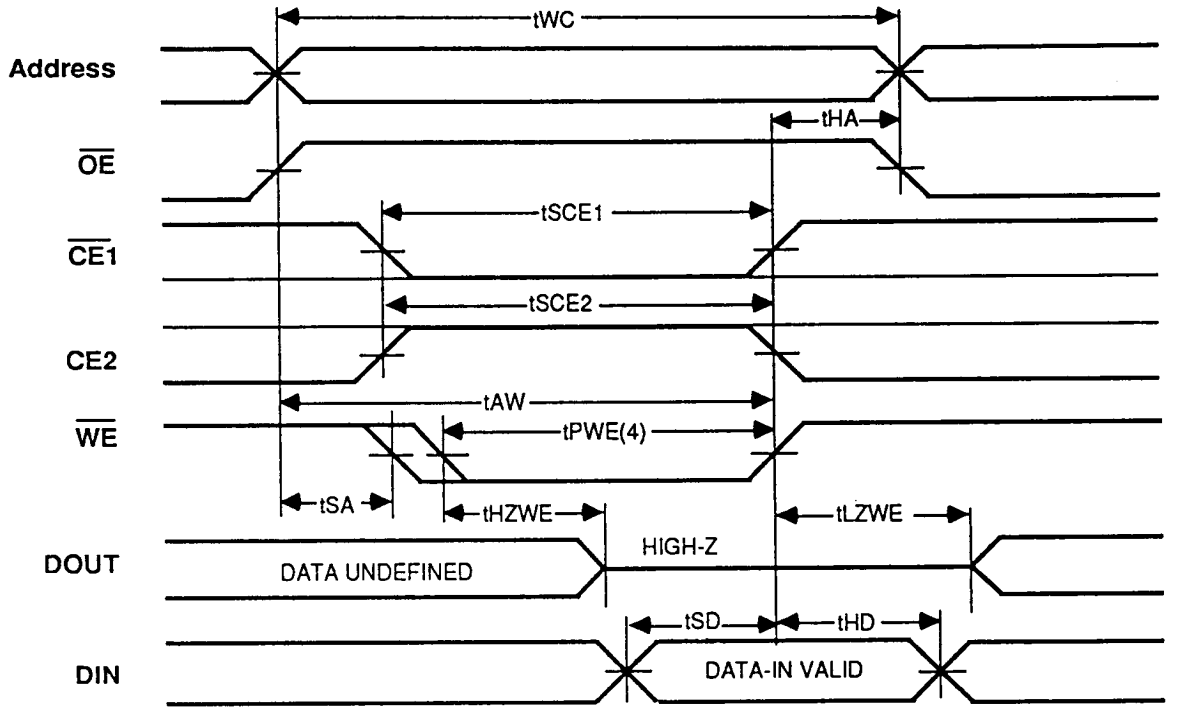
READ CYCLE NO. 1 (Note 5,6)



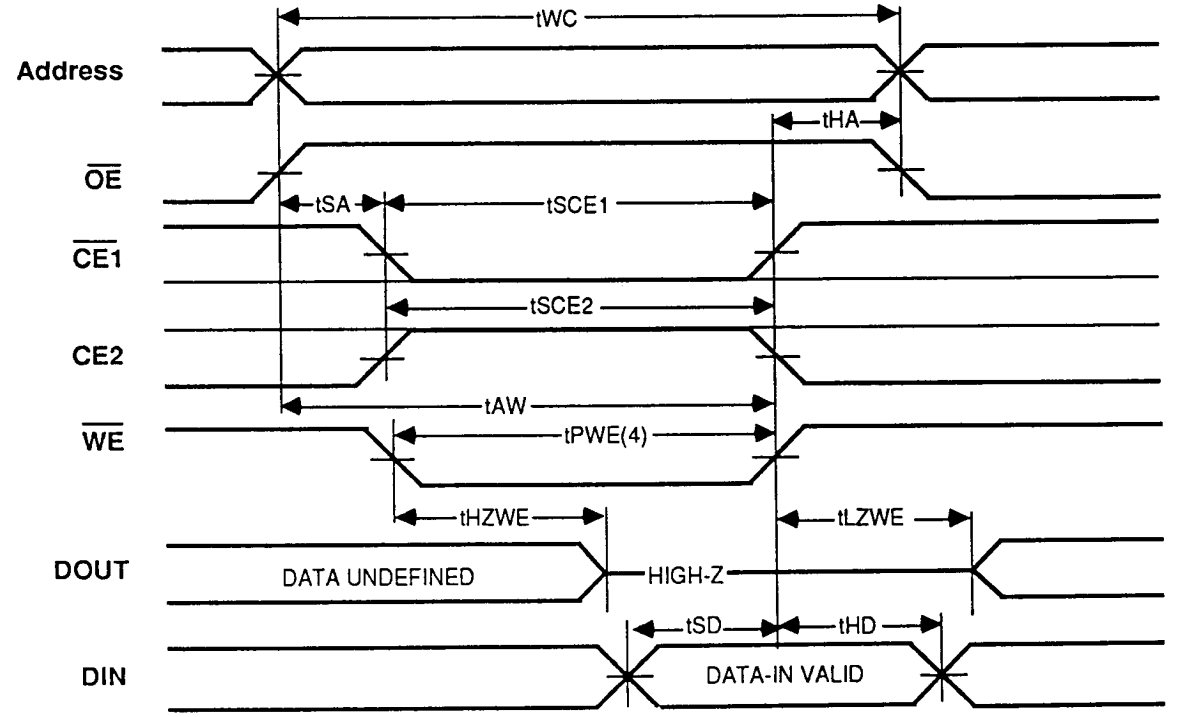
READ CYCLE NO. 2 (Note 5,7)



WRITE CYCLE NO. 1 ($\overline{WE}$ controlled) (Note 3,8)



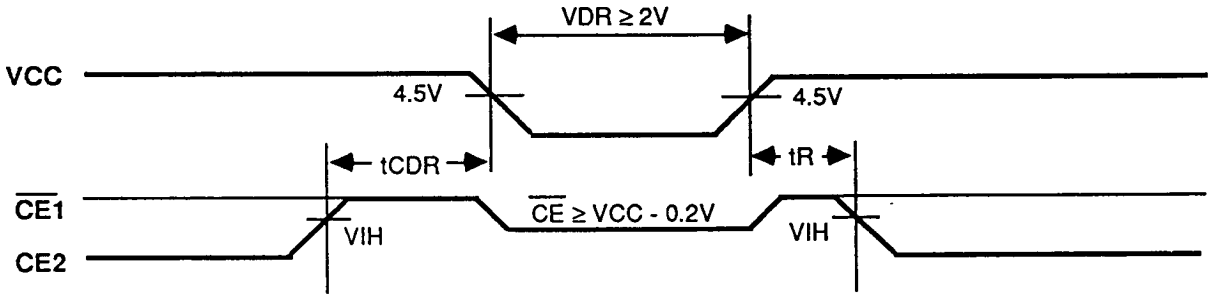
WRITE CYCLE NO. 2 ($\overline{CE1}$, CE2 controlled) (Note 3,8)



DATA RETENTION CHARACTERISTICS

Parameter	Description	Test Condition	Min.	Max.	Units
VDR	VCC for retention of data	VCC = 2.0V	2.0	---	V
ICCDR	Data retention current	$\overline{CE1}$≥VCC-0.2V,	----	50	µA
tCDR	Chip deselect to data retention time	CE2≤0.2V,	0	----	ns
tR	Operation recovery time	CMOS Inputs	5	----	ms
IL I	Input leakage current		----	2	µA

DATA RETENTION WAVEFORM



PIN DESCRIPTIONS

A_0 - A_{16} Address Inputs
These 17 address inputs select one of the 131,072 8-bit words in the RAM.

$\overline{CE1}$ Chip Enable 1 Input
CE2 Chip Enable 2 Input
$\overline{CE1}$ is active Low and CE2 is active High. The chip enable is active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

$\overline{OE}$ Output Enable Input
The ouput enable input is active Low. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the I/O pins. The I/O pins will be in the high-impedance state when $\overline{OE}$ is inactive.

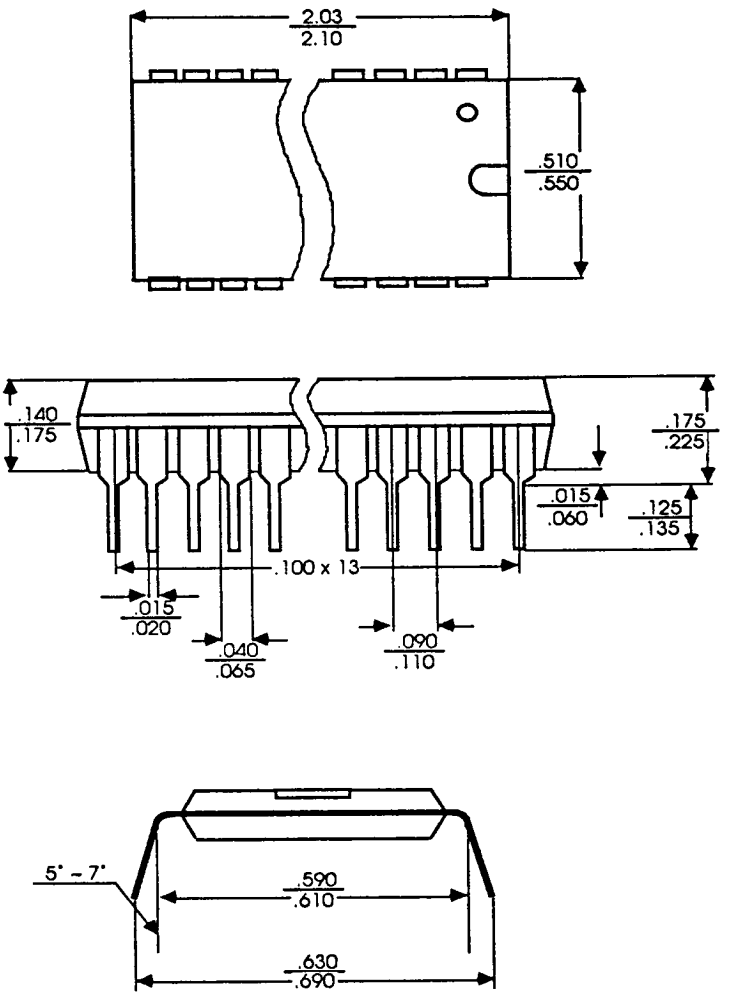
$\overline{WE}$ Write Enable Input
The write enable input is active Low and controls read and write operations. With the chip selected, when $\overline{WE}$ is Low Input data present on the I/O pins will be written into the selected memory location.

I/O_0 - I/O_7
These 8 bidirectional ports are used to read data from or write data into the RAM.

Vcc - Power

GND - Ground

32 Pin 600 MIL PLASTIC DIP Package



SPEED (ns)	ORDER PART NUMBER	PACKAGE	TEMPERATURE RANGE
70	IS62C1024-70W	Plastic DIP - 600 mil	0°C to +70°C
70 Low Power	IS62C1024-L70W	Plastic DIP - 600 mil	0°C to +70°C
85	IS62C1024-85W	Plastic DIP - 600 mil	0°C to +70°C
85 Low Power	IS62C1024-L85W	Plastic DIP - 600 mil	0°C to +70°C
100	IS62C1024-100W	Plastic DIP - 600 mil	0°C to +70°C
100 Low Power	IS62C1024-L100W	Plastic DIP - 600 mil	0°C to +70°C

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