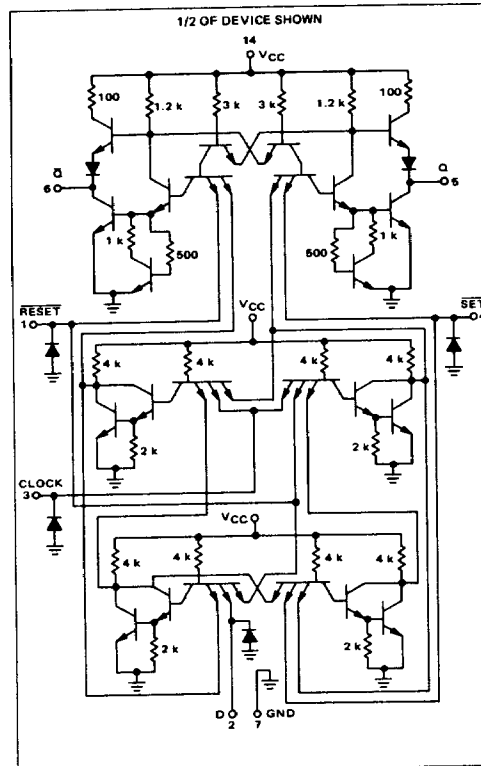


DUAL TYPE D FLIP-FLOP

MTTL III MC3100/3000 series

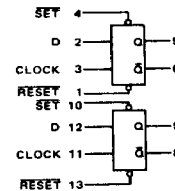
MC3160F • MC3060F
MC3160L • MC3060L,P



This dual flip-flop triggers on the positive edge of the clock and performs the Type D flip-flop logic function. This device consists of two completely independent Type D flip-flops, both having direct SET and RESET inputs for asynchronous operations such as parallel data entry in shift register applications.

Information may be applied to, or changed at, the D inputs any time during the clock cycle except during the time interval between the Setup and Hold times. The clocked inputs are inhibited when the clock is high and data may be applied to the input steering section of the flip-flop when the clock goes low. The input steering section continually reflects the input state being applied when the clock is low. The information present at the inputs during the time interval between the Setup and Hold times is transferred to the bistable section on the positive edge of the clock, and the outputs Q and $\bar{Q}$ respond accordingly.

The flip-flop can also be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct SET or RESET inputs.



TRUTH TABLE

D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$$Q^{n+1} = D^n$$

Input Loading Factors:

SET = 1.15
RESET = 1.7
CLOCK = 1.5
D = 0.75

Output Loading Factor = 10

Typical Characteristics: ($V_{CC} = 5.0$ V, $T_A = 25^\circ\text{C}$)

Total Power Dissipation = 120 mW/pkg

Toggle Frequency = 30 MHz

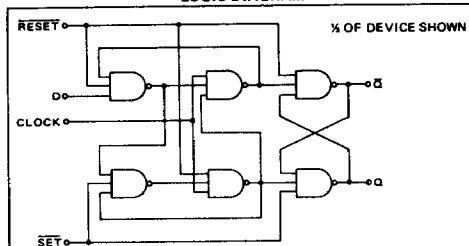
Logical "1" Setup Time = 10 ns

Logical "1" and "0" Hold Times = 5.0 ns

$t_{pd} = 17$ ns

$t_{pd+} = 15$ ns

LOGIC DIAGRAM



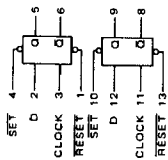
See General Information section for packaging

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ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.

[illegible]

MC3160F, MC3060F/MC3160L, MC3060L,P (continued)

OPERATING CHARACTERISTICS

Data must be present 15 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

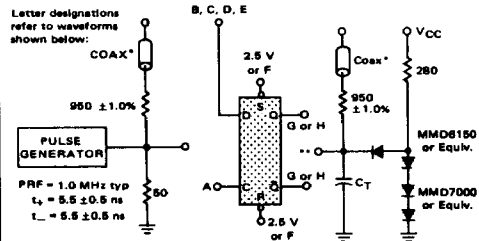
The direct **SET** and **RESET** inputs may be used at any time as they completely override the clock.

Positive edge triggering: When the clock goes from the low to the high state, the information in the input steering section is transferred to the bistable section.

Unused inputs should be tied to a voltage between 2.0 and 5.5 Vdc.

SWITCHING TIME TEST CIRCUIT

Letter designations refer to waveforms shown below:



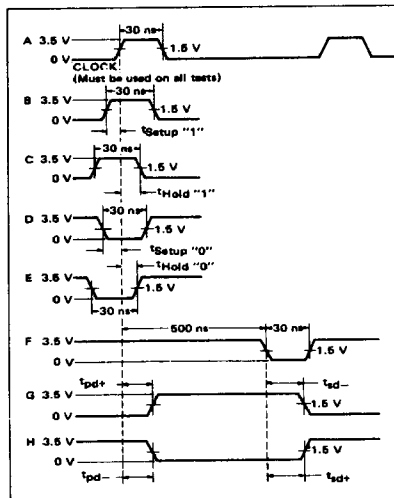
Three pulse generators are required and must be slewed together to provide the waveforms shown.

**A load is connected to each output during the test.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



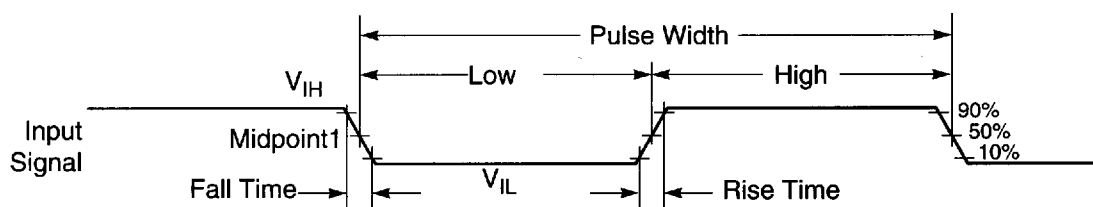
TEST PROCEDURES CHART

TEST	D*	INPUT		Q*	Q*	LIMITS (ns)	
		SET	RESET*			Min	Max
t _{setup} "1"	D	B	F	G	H	—	15
t _{hold} "1"	D	C	F	G	H	—	5.0
t _{setup} "0"	D	D	F	H	G	—	15
t _{hold} "0"	D	E	F	H	G	—	5.0
t _{pd+}		Delay from clock to Q during t _{setup} "1" D test. Delay from clock to Q-bar during t _{setup} "0" D test.				10	25
t _{pd-}		Delay from clock to Q during t _{setup} "0" D test. Delay from clock to Q-bar during t _{setup} "1" D test.				10	25
t _{sd+}		Delay from SET to Q during t _{setup} "0" D test. Delay from RESET to Q-bar during t _{setup} "1" D test.				5.0	20
t _{sd-}		Delay from SET to Q-bar during t _{setup} "0" D test. Delay from RESET to Q during t _{setup} "1" D test.				5.0	20

* Letters shown in these columns refer to waveforms at left.

AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, RESET, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

AA0179

Figure 2-1 Signal Measurement Reference