

# DATA SHEET

## **CBTD3384**

10-bit level shifting bus switch  
with 5-bit output enables

Product data  
Supersedes data of 2000 Aug 30  
File under Integrated Circuits — ICL03

2001 Dec 20

# 10-bit level shifting bus switch with 5-bit output enables

CBTD3384

## FEATURES

- 5  $\Omega$  switch connection between two ports
- TTL compatible control input and output levels
- Designed to be used in 5 V to 3.3 V level shifting applications
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, and 1000 V CDM per JESD22-C101

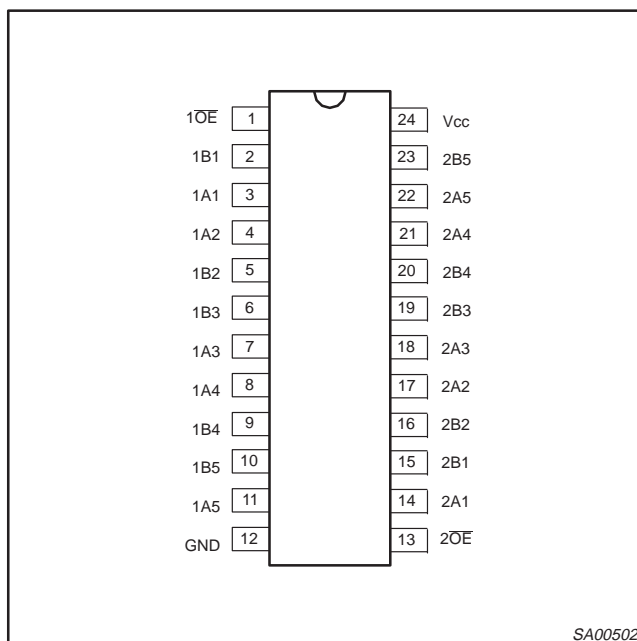
## DESCRIPTION

The CBTD3384 provides ten bits of high-speed TTL-compatible level shifting bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The gate voltage of the enabled switch is lowered by a diode to allow convenient level shifting between 5 V and 3.3 V levels on either side of the CBTD3384.

The CBTD3384 device is organized as two 5-bit bus switches with separate output-enable (OE) inputs. When OE is low, the switch is on and port A is connected to B. When OE is high, the switch is open and high-impedance state exists between the two ports.

The CBTD3384 is characterized for operation from  $-40$  to  $+85$  °C.

## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 13	1OE, 2OE	Output enables
3, 4, 7, 8, 11	1A1–1A5	Inputs
14, 17, 18, 21, 22	2A1–2A5	Inputs
2, 5, 6, 9, 10	1B1–1B5	Outputs
15, 16, 19, 20, 23	2B1–2B5	Outputs
12	GND	Ground (0V)
24	V <sub>CC</sub>	Positive supply voltage

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25$ °C; GND = 0 V	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Yn	$C_L = 50$ pF; $V_{CC} = 5$ V	250	ps
$C_{IN}$	Input capacitance	$V_I = 0$ V or $V_{CC}$	3	pF
$C_{OUT}$	Output capacitance	Outputs disabled; $V_O = 0$ V or $V_{CC}$	6	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 5.5$ V	0.2	$\mu$ A

## ORDERING INFORMATION

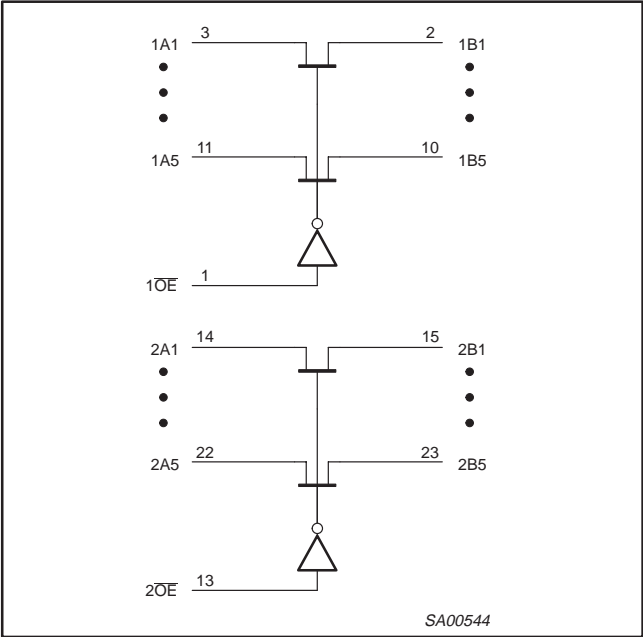
PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
24-Pin Plastic SO	$-40$ to $+85$ °C	CBTD3384D	SOT137-1
24-Pin Plastic SSOP	$-40$ to $+85$ °C	CBTD3384DB	SOT340-1
24-Pin Plastic SSOP (QSOP)	$-40$ to $+85$ °C	CBTD3384DK	SOT556-1
24-Pin Plastic TSSOP	$-40$ to $+85$ °C	CBTD3384PW	SOT355-1

Standard packing quantities and other packaging data is available at [www.philipslogic.com/packaging](http://www.philipslogic.com/packaging).

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LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS	
1OE	2OE	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

H = High voltage level  
L = Low voltage level  
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		−0.5 to +7.0	V
I <sub>IK</sub>	DC input diode current		−50	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		−1.2 to +7.0	V
I <sub>SW</sub>	DC output diode current	V <sub>O</sub> < 0	±128	mA
T <sub>stg</sub>	Storage temperature range		−65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V <sub>CC</sub>	DC supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0	—	V
V <sub>IL</sub>	Low-level Input voltage	—	0.8	V
T <sub>amb</sub>	Operating free-air temperature range	−40	+85	°C

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T <sub>amb</sub> = −40 °C to +85 °C			
			Min	Typ <sup>1</sup>	Max	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5 V; I <sub>I</sub> = −18 mA	—	—	−1.2	V
V <sub>OH</sub>	Output high pass voltage	See Figure 1	—	—	—	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V	—	—	±1	μA
I <sub>CC</sub>	Quiescent supply current <sup>2</sup>	V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND; 1OE=2OE=GND	—	—	1.5	mA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 5.5 V, one input at 3.4 V, other inputs at V <sub>CC</sub> or GND	—	—	2.5	mA
C <sub>I</sub>	Control pins	V <sub>I</sub> = 3 V or 0	—	3.2	—	pF
C <sub>I(OFF)</sub>	Port off capacitance	V <sub>O</sub> = 3 V or 0, $\overline{\text{OE}}$ = V <sub>CC</sub>	—	6	—	pF
r <sub>on</sub> <sup>3</sup>	On-resistance	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 64 mA	—	5	7	Ω
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 30 mA	—	5	7	
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 2.4 V; I <sub>I</sub> = −15 mA	—	17	50	

### NOTES:

1. All typical values are at  $V_{\text{CC}} = 5\text{ V}$ ,  $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{\text{CC}}$  or GND
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

## AC CHARACTERISTICS

GND = 0 V;  $t_{\text{R}} = t_{\text{F}} = 2.5\text{ nS}$ ;  $C_{\text{L}} = 50\text{ pF}$

SYMBOL	PARAMETER DESCRIPTION	LIMITS			UNIT
		−40 °C to +85 °C V <sub>CC</sub> = 5 V ± 0.5 V			
		Min	Mean	Max	
t <sub>pd</sub>	Propagation delay <sup>1</sup>	—	—	250	ps
t <sub>PZH</sub>	Output enable time to High level	2.3	4.3	7.0	ns
t <sub>PHZ</sub>	Output disable time from High level	1.7	2.4	5.3	ns
t <sub>PZL</sub>	Output enable time to Low level	2.3	4.9	7.5	ns
t <sub>PLZ</sub>	Output disable time from Low level	1.7	4.2	5.3	ns

### NOTE:

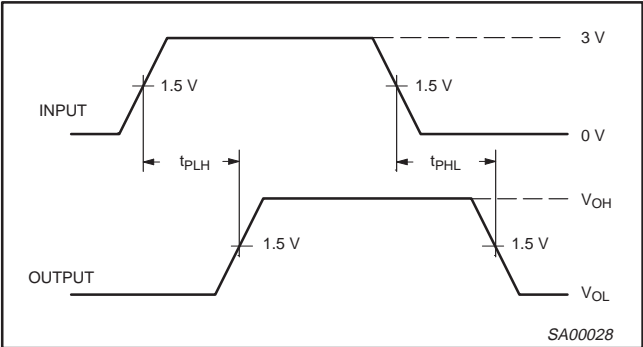
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

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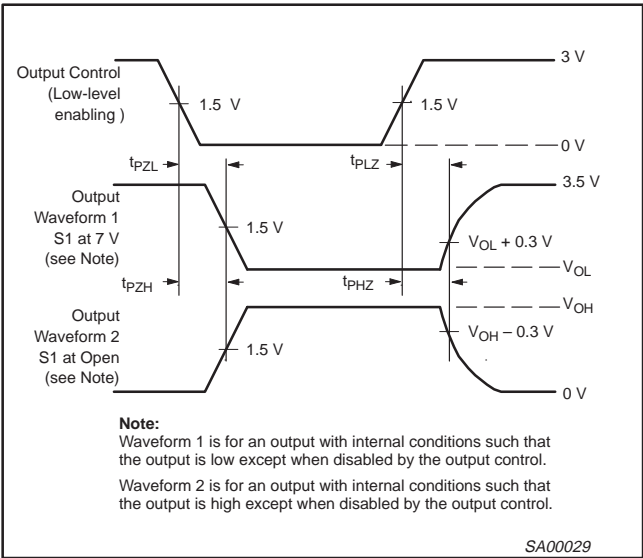
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AC WAVEFORMS

$V_M = 1.5\text{ V}$ ,  $V_{IN} = \text{GND to } 3.0\text{ V}$



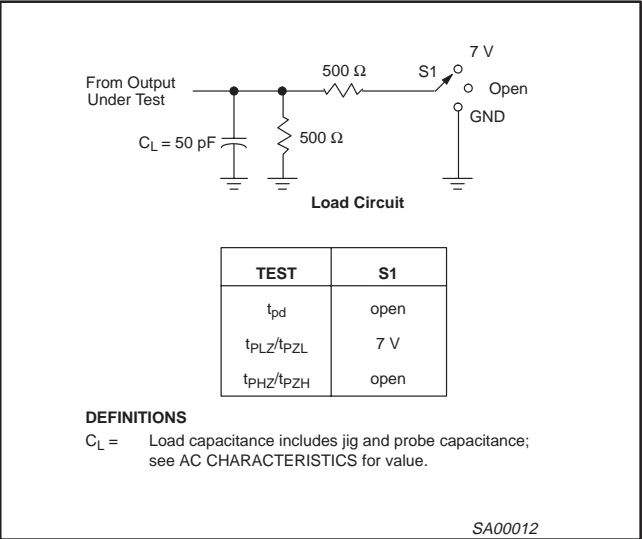
Waveform 1. Input (An) to Output (Yn) Propagation Delays



**Note:**  
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS

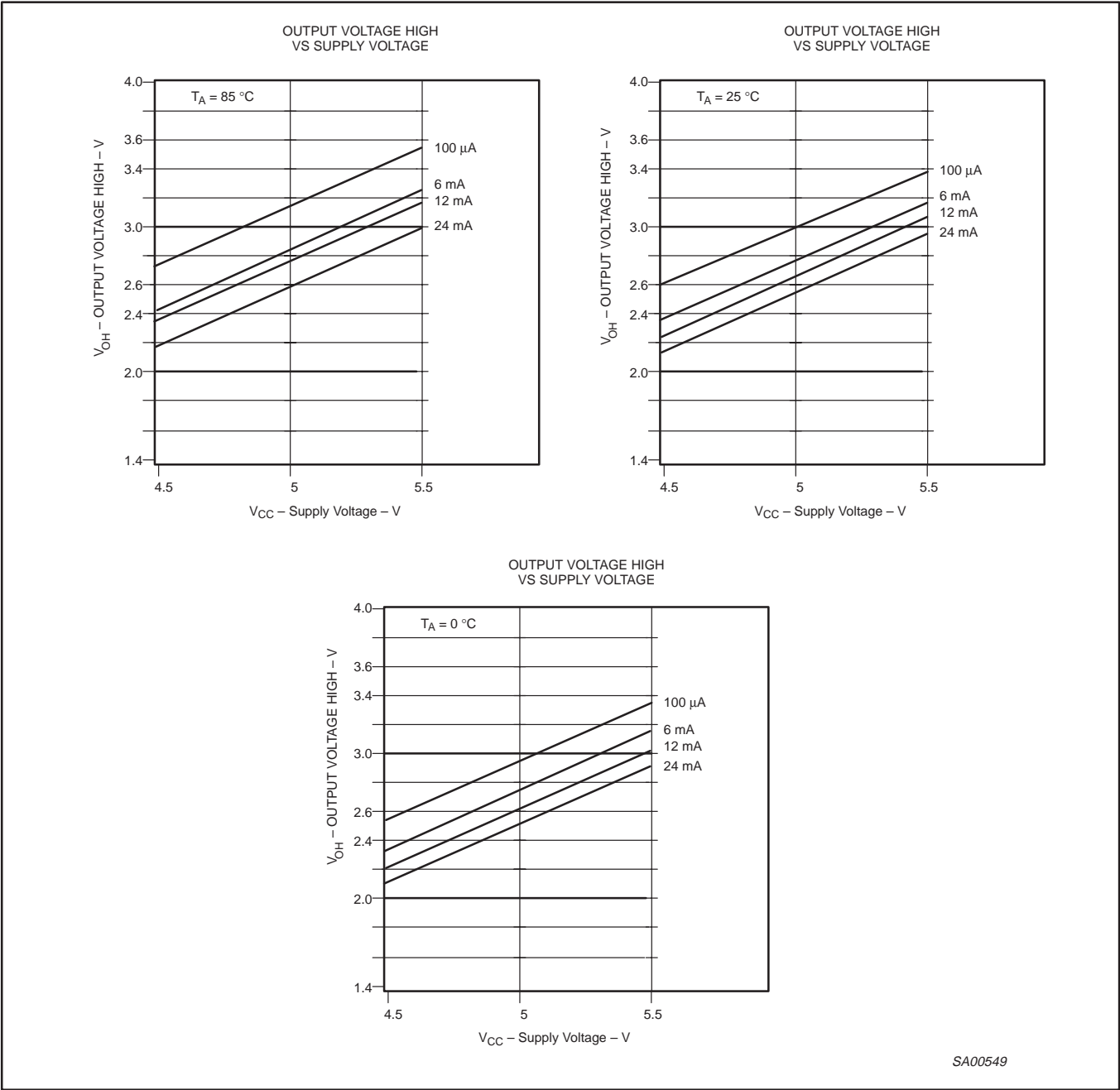


- NOTES:**
1. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  2. The outputs are measured one at a time with one transition per measurement.

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TYPICAL CHARACTERISTICS

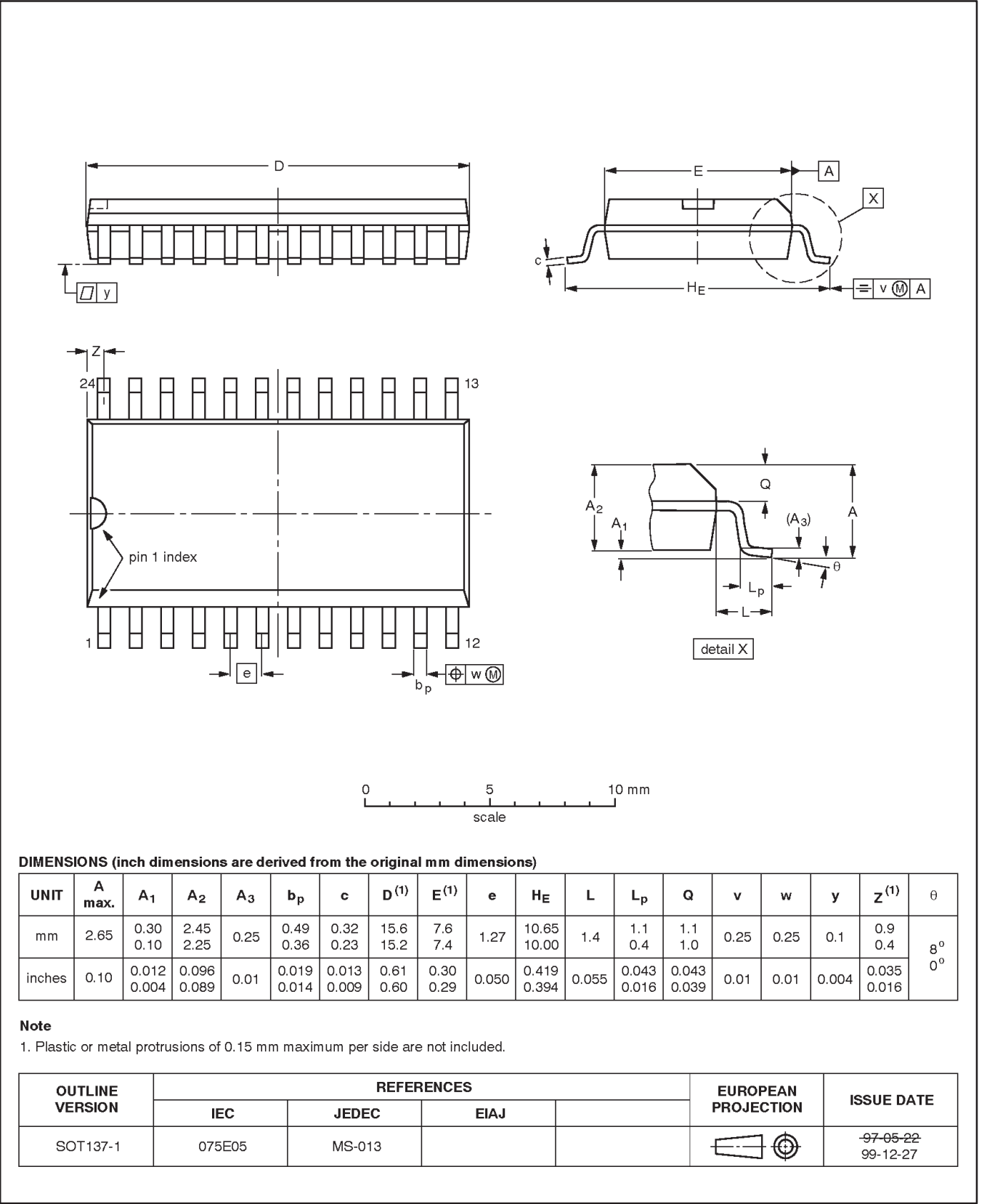


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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

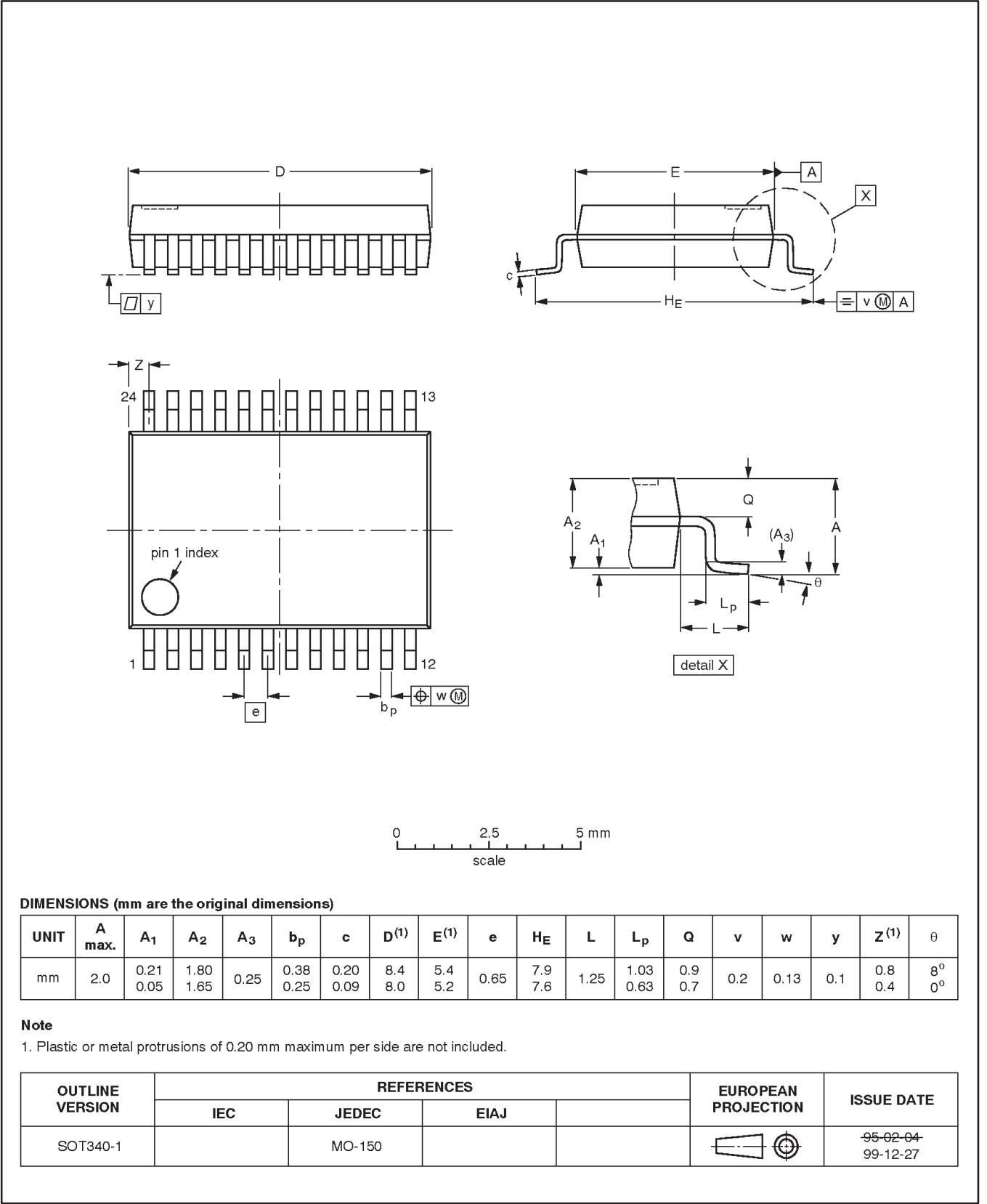


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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



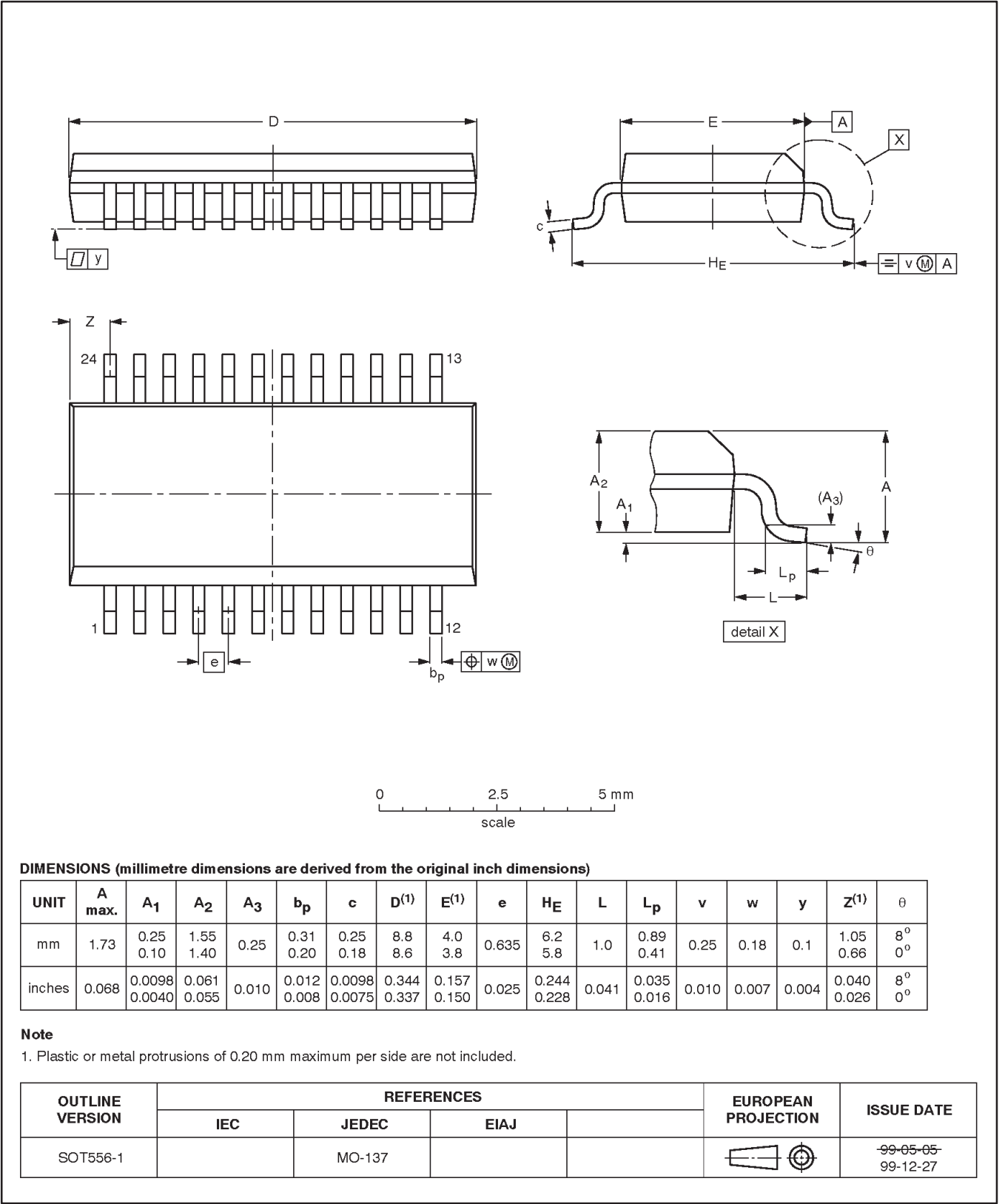


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SSOP24: plastic shrink small outline package; 24 leads;  
body width 3.9 mm; lead pitch 0.635 mm

SOT556-1

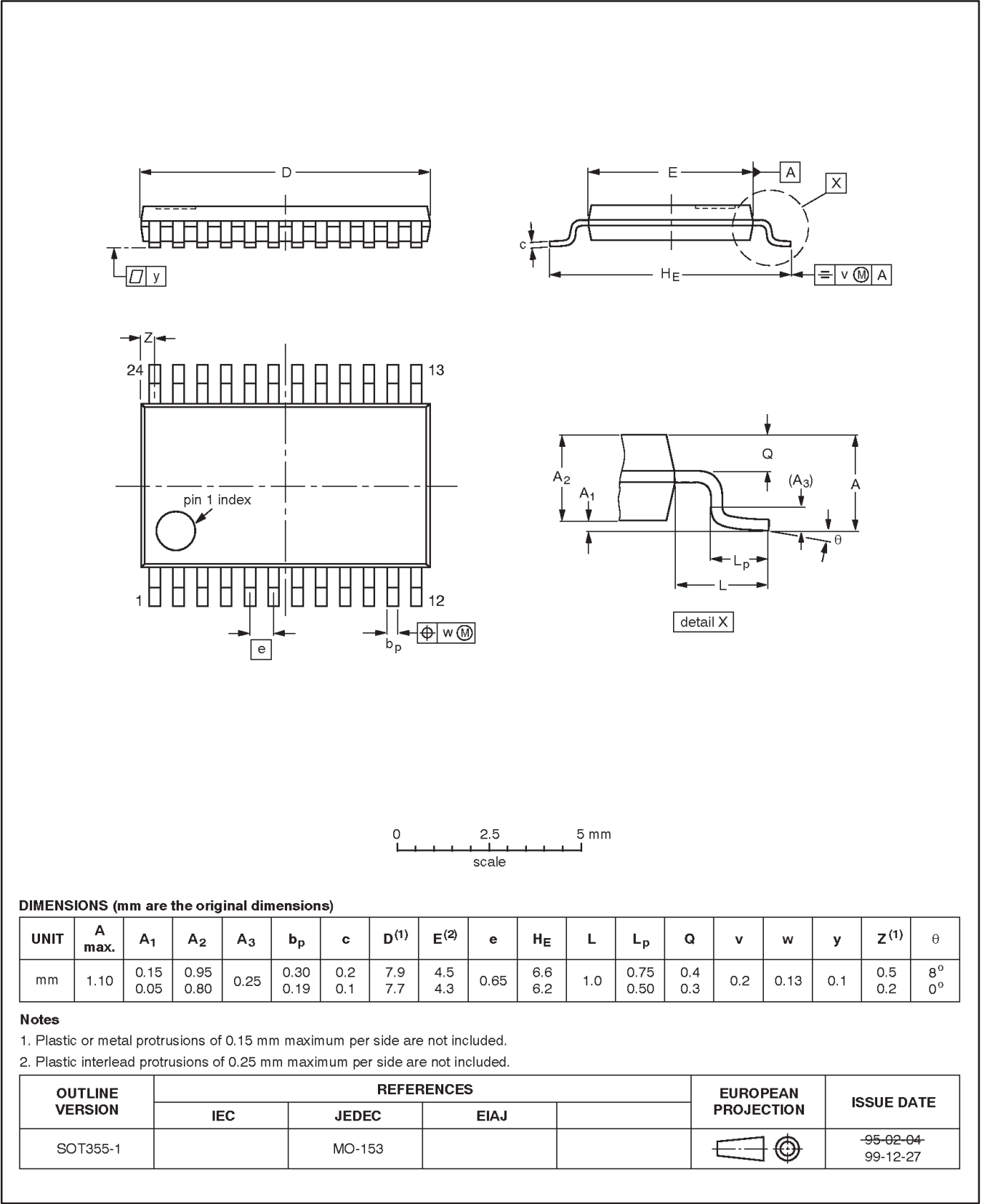


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TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



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**CBTD3384****NOTES**

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