

IRS2110(-1,-2,S)PbF IRS2113(-1,-2,S)PbF

Features

- Floating channel designed for bootstrap operation
- Fully operational to +500 V or +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V logic compatible
- Separate logic supply range from 3.3 V to 20 V
- Logic and power ground ± 5 V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Description

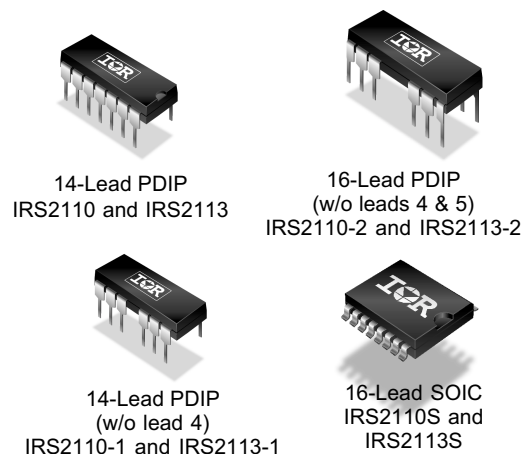
The IRS2110/IRS2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 V or 600 V.

HIGH AND LOW SIDE DRIVER

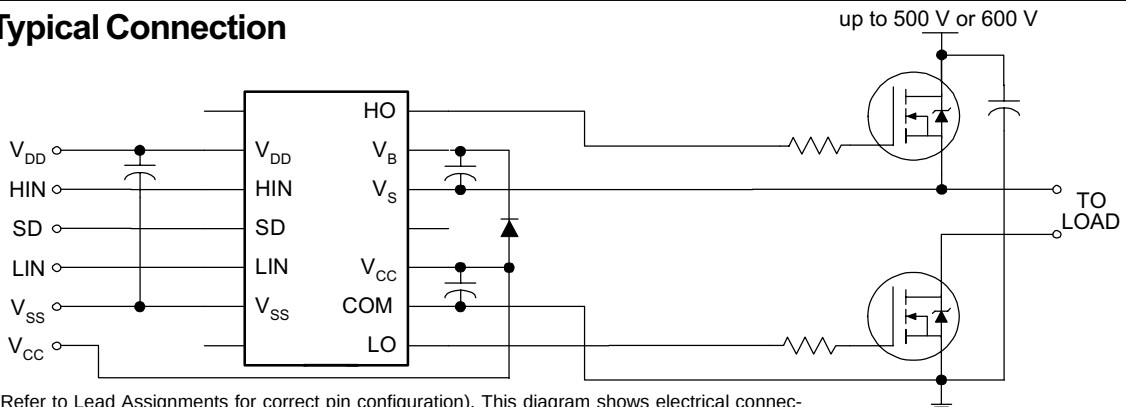
Product Summary

V _{OFFSET} (IRS2110) (IRS2113)	500 V max. 600 V max.
I _{O+/-}	2 A/2 A
V _{OUT}	10 V - 20 V
t _{on/off} (typ.)	130 ns & 120 ns
Delay Matching (IRS2110) (IRS2113)	10 ns max. 20 ns max.

Packages



Typical Connection



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figs. 28 through 35.

Symbol	Definition		Min.	Max.	Units
V _B	High side floating supply voltage	(IRS2110)	-0.3	520 (Note 1)	V
		(IRS2113)	-0.3	620 (Note 1)	
V _S	High side floating supply offset voltage		V _B - 20	V _B + 0.3	
V _{HO}	High side floating output voltage		V _S - 0.3	V _B + 0.3	
V _{CC}	Low side fixed supply voltage		-0.3	20 (Note 1)	
V _{LO}	Low side output voltage		-0.3	V _{CC} + 0.3	
V _{DD}	Logic supply voltage		-0.3	V _{SS} +20 (Note 1)	
V _{SS}	Logic supply offset voltage		V _{CC} - 20	V _{CC} + 0.3	
V _{IN}	Logic input voltage (HIN, LIN, & SD)		V _{SS} - 0.3	V _{DD} + 0.3	
dV _S /dt	Allowable offset supply voltage transient (Fig. 2)		—	50	V/ns
PD	Package power dissipation @ T _A ≤ +25 °C	(14 lead DIP)	—	1.6	W
		(16 lead SOIC)	—	1.25	
R _{THJA}	Thermal resistance, junction to ambient	(14 lead DIP)	—	75	°C/W
		(16 lead SOIC)	—	100	
T _J	Junction temperature		—	150	°C
T _S	Storage temperature		-55	150	
T _L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: All supplies are fully tested at 25 V, and an internal 20 V clamp exists for each supply.

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation, the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at a 15 V differential. Typical ratings at other bias conditions are shown in Figs. 36 and 37.

Symbol	Definition		Min.	Max.	Units
V _B	High side floating supply absolute voltage		V _S + 10	V _S + 20	V
V _S	High side floating supply offset voltage	(IRS2110)	Note 2	500	
		(IRS2113)	Note 2	600	
V _{HO}	High side floating output voltage		V _S	V _B	
V _{CC}	Low side fixed supply voltage		10	20	
V _{LO}	Low side output voltage		0	V _{CC}	
V _{DD}	Logic supply voltage		V _{SS} + 3	V _{SS} + 20	
V _{SS}	Logic supply offset voltage		-5 (Note 3)	5	
V _{IN}	Logic input voltage (HIN, LIN & SD)		V _{SS}	V _{DD}	°C
T _A	Ambient temperature		-40	125	

Note 2: Logic operational for V_S of -4 V to +500 V. Logic state held for V_S of -4 V to -V_{BS}. (Refer to the Design Tip DT97-3)

Note 3: When V_{DD} < 5 V, the minimum V_{SS} offset is limited to -V_{DD}.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15 V, C_L = 1000 pF, T_A = 25 °C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Fig. 3.

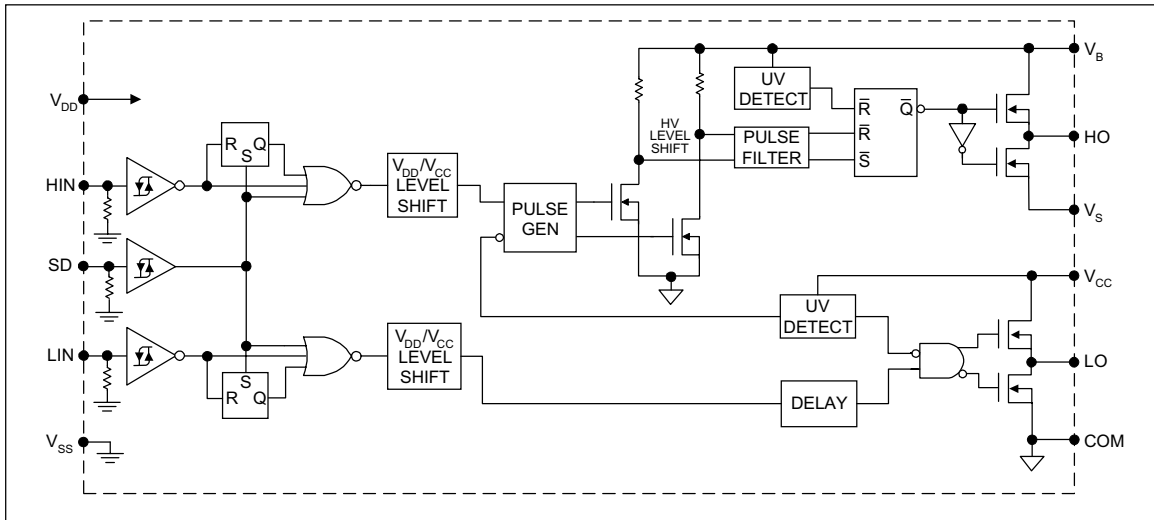
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	7	—	130	160	ns	$V_S = 0$ V
t_{off}	Turn-off propagation delay	8	—	120	150		$V_S = 500$ V/600 V
t_{sd}	Shutdown propagation delay	9	—	130	160		
t_r	Turn-on rise time	10	—	25	35		
t_f	Turn-off fall time	11	—	17	25		
MT	Delay matching, HS & LS turn-on/off	(IRS2110)	—	—	—	10	
		(IRS2113)	—	—	—	20	

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15 V, T_A = 25 °C and V_{SS} = COM unless otherwise specified. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN, and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	12	9.5	—	—	V	
V_{IL}	Logic "0" input voltage	13	—	—	6.0		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	14	—	—	1.2		$I_O = 0$ A
V_{OL}	Low level output voltage, V_O	15	—	—	0.15		$I_O = 20$ mA
I_{LK}	Offset supply leakage current	16	—	—	50	μ A	$V_B = V_S = 500$ V/600 V
I_{QBS}	Quiescent V_{BS} supply current	17	—	125	230		$V_{IN} = 0$ V or V_{DD}
I_{QCC}	Quiescent V_{CC} supply current	18	—	180	340		
I_{QDD}	Quiescent V_{DD} supply current	19	—	15	30		
I_{IN+}	Logic "1" input bias current	20	—	20	40		$V_{IN} = V_{DD}$
I_{IN-}	Logic "0" input bias current	21	—	—	1.0		$V_{IN} = 0$ V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	22	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	24	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	25	7.0	8.2	9.4		
I_{O+}	Output high short circuit pulsed current	26	2.0	2.5	—	A	$V_O = 0$ V, $V_{IN} = V_{DD}$ $PW \leq 10$ μ s
I_{O-}	Output low short circuit pulsed current	27	2.0	2.5	—		$V_O = 15$ V, $V_{IN} = 0$ V $PW \leq 10$ μ s

Functional Block Diagram



Lead Definitions

Symbol	Description
V _{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V _{SS}	Logic ground
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
V _{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

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Lead Assignments

<table><tr><td>8</td><td></td><td>HO</td><td>7</td></tr><tr><td>9</td><td>VDD</td><td>VB</td><td>6</td></tr><tr><td>10</td><td>HIN</td><td>VS</td><td>5</td></tr><tr><td>11</td><td>SD</td><td></td><td>4</td></tr><tr><td>12</td><td>LIN</td><td>VCC</td><td>3</td></tr><tr><td>13</td><td>VSS</td><td>COM</td><td>2</td></tr><tr><td>14</td><td></td><td>LO</td><td>1</td></tr></table> 14 Lead PDIP IRS2110/IRS2113	8		HO	7	9	VDD	VB	6	10	HIN	VS	5	11	SD		4	12	LIN	VCC	3	13	VSS	COM	2	14		LO	1	<table><tr><td>9</td><td></td><td>HO</td><td>8</td></tr><tr><td>10</td><td></td><td>VB</td><td>7</td></tr><tr><td>11</td><td>VDD</td><td>VS</td><td>6</td></tr><tr><td>12</td><td>HIN</td><td></td><td></td></tr><tr><td>13</td><td>SD</td><td></td><td></td></tr><tr><td>14</td><td>LIN</td><td>VCC</td><td>3</td></tr><tr><td>15</td><td>VSS</td><td>COM</td><td>2</td></tr><tr><td>16</td><td></td><td>LO</td><td>1</td></tr></table> 16 Lead SOIC (Wide Body) IRS2110S/IRS2113S	9		HO	8	10		VB	7	11	VDD	VS	6	12	HIN			13	SD			14	LIN	VCC	3	15	VSS	COM	2	16		LO	1
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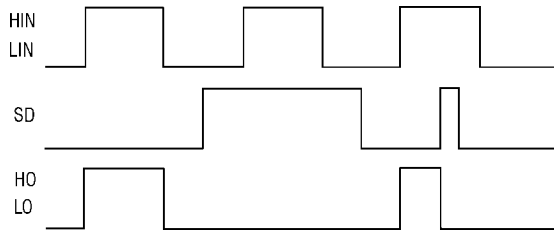


Figure 1. Input/Output Timing Diagram

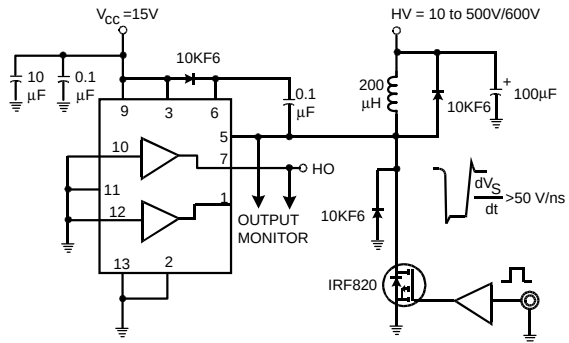


Figure 2. Floating Supply Voltage Transient Test Circuit

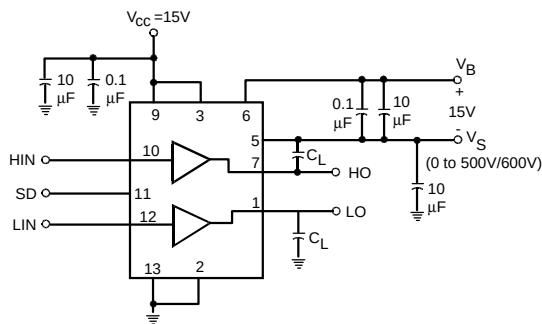


Figure 3. Switching Time Test Circuit

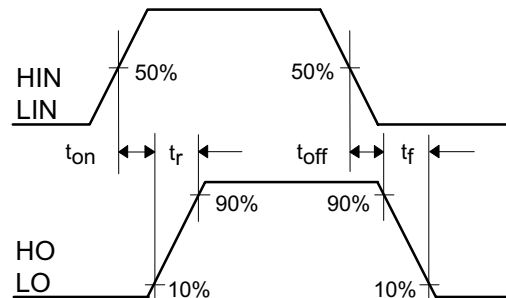


Figure 4. Switching Time Waveform Definition

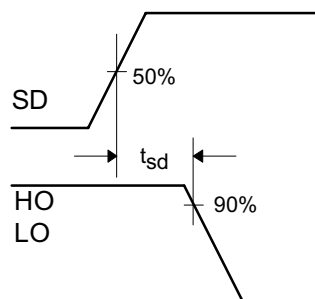


Figure 5. Shutdown Waveform Definitions

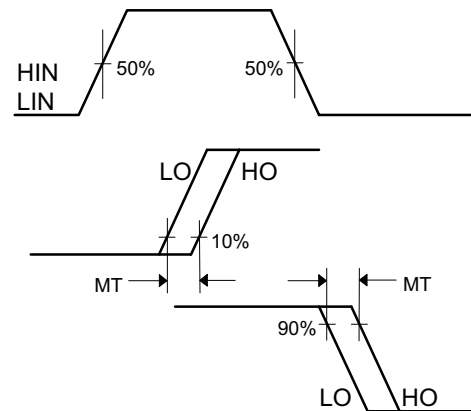


Figure 6. Delay Matching Waveform Definitions

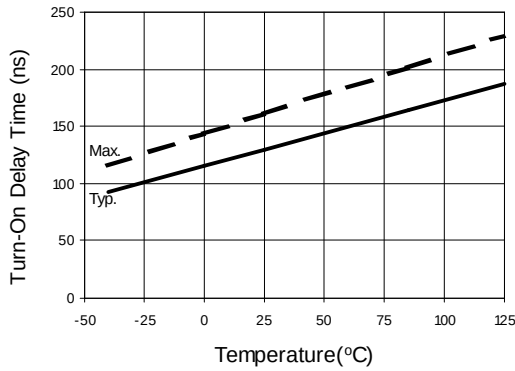


Figure 7A. Turn-On Time vs. Temperature

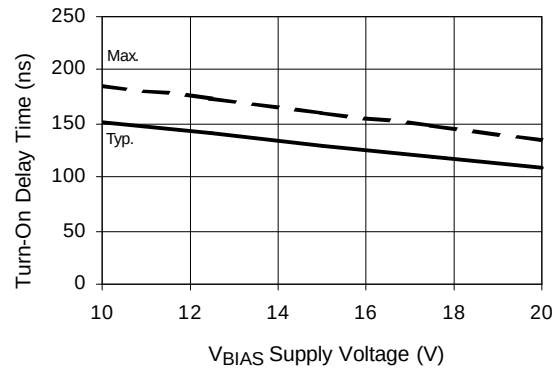


Figure 7B. Turn-On Time vs. Supply Voltage

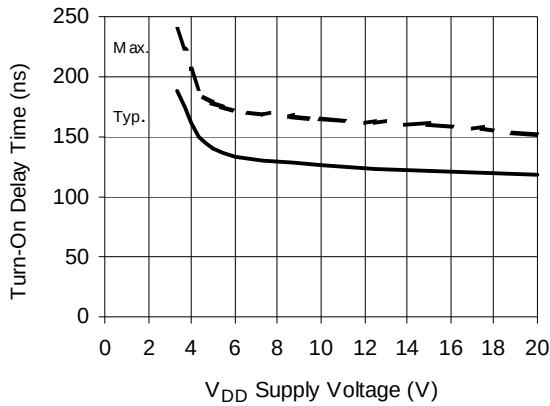


Figure 7C. Turn-On Time vs. V_{DD} Supply Voltage

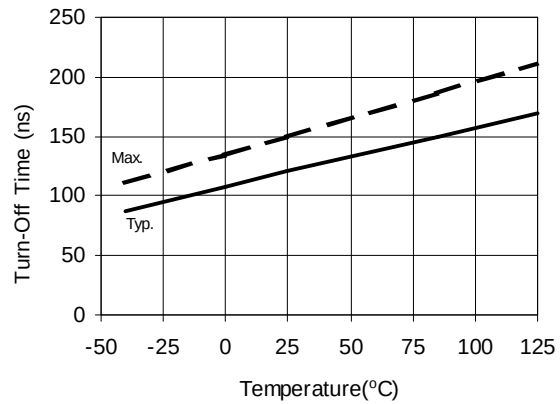


Figure 8A. Turn-Off Time vs. Temperature

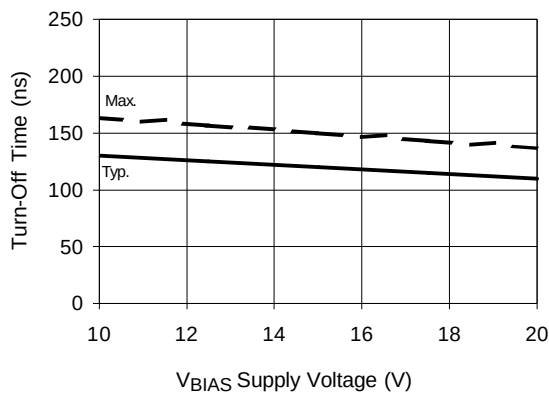


Figure 8B. Turn-Off Time vs. Supply Voltage

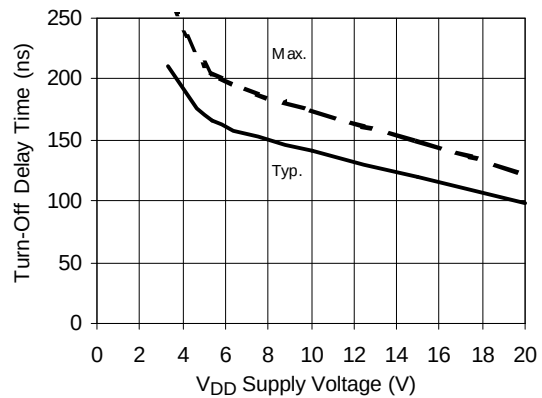


Figure 8C. Turn-Off Time vs. V_{DD} Supply Voltage

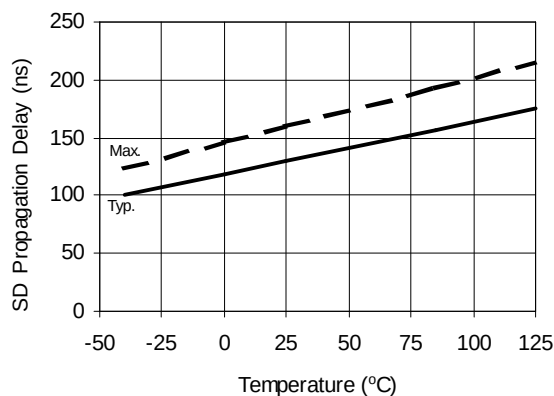


Figure 9A. Shutdown Time vs. Temperature

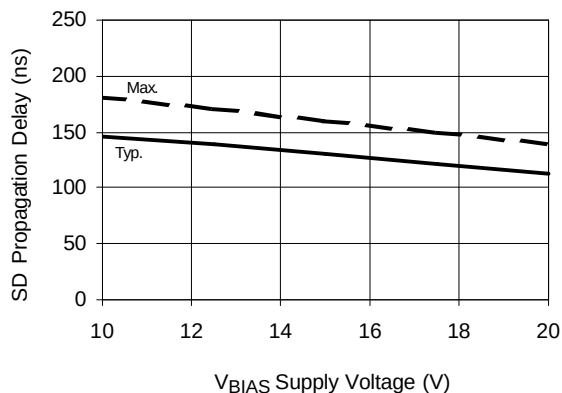


Figure 9B. Shutdown Time vs. Supply Voltage

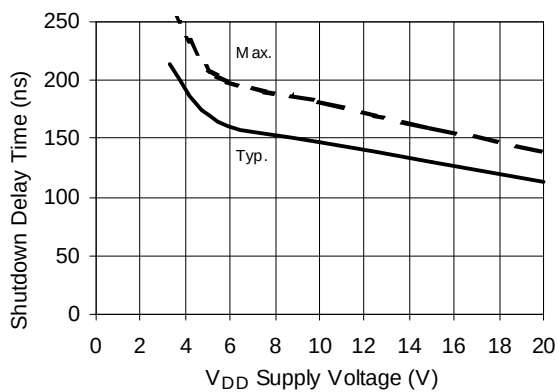


Figure 9C. Shutdown Time vs. VDD Supply Voltage

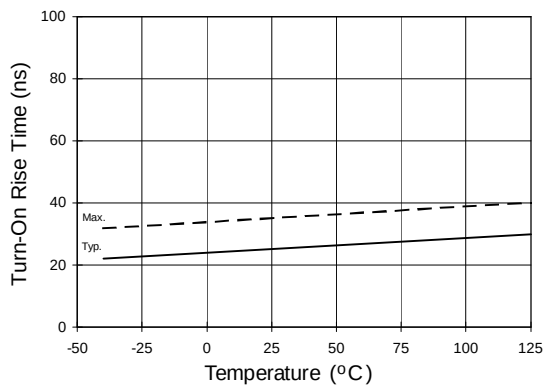


Figure 10A. Turn-On Rise Time vs. Temperature

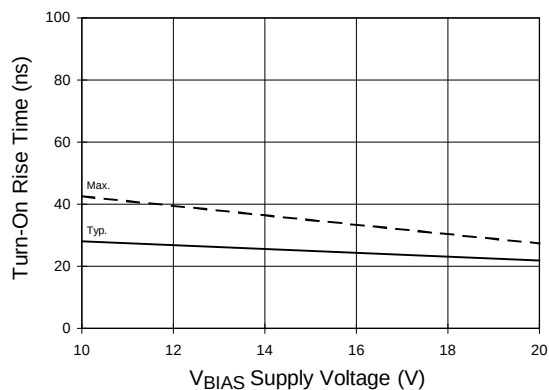


Figure 10B. Turn-On Rise Time vs. Voltage

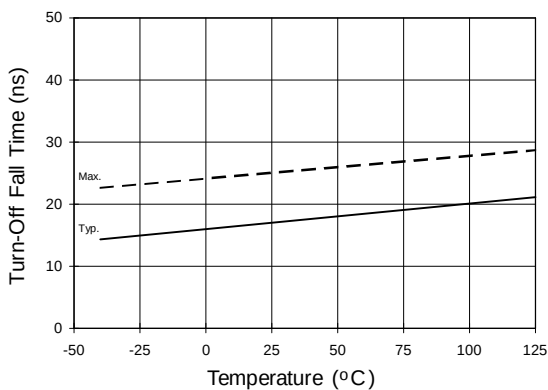


Figure 11A. Turn-Off Fall Time vs. Temperature

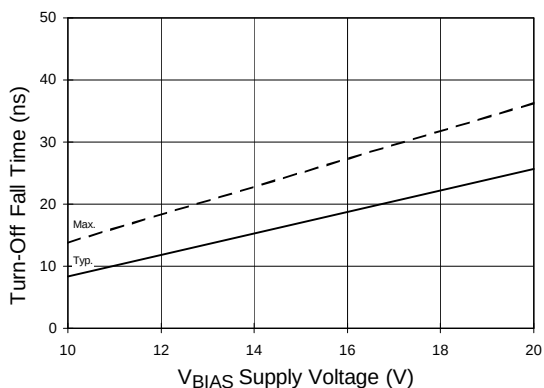


Figure 11B. Turn-Off Fall Time vs. Voltage

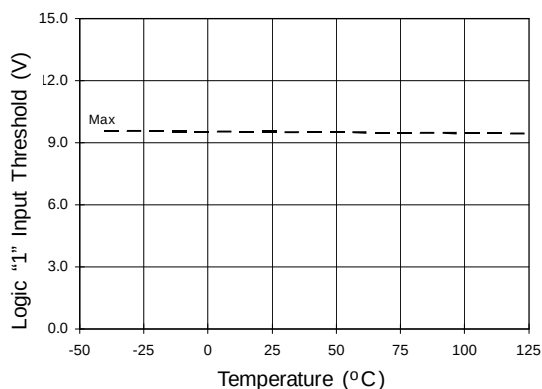


Figure 12A. Logic "1" Input Threshold vs. Temperature

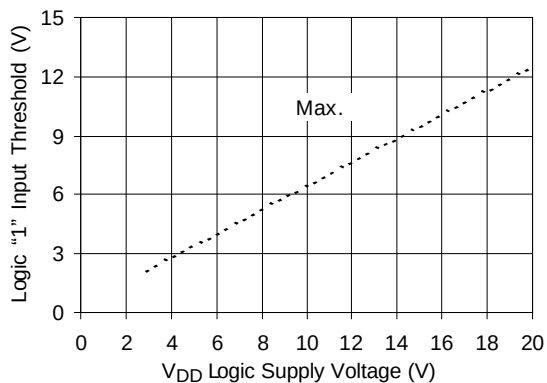


Figure 12B. Logic "1" Input Threshold vs. Voltage

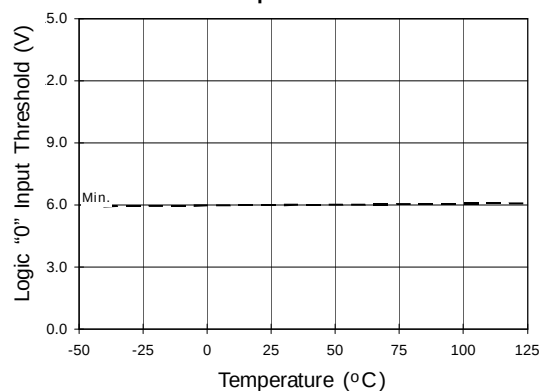


Figure 13A. Logic "0" Input Threshold vs. Temperature

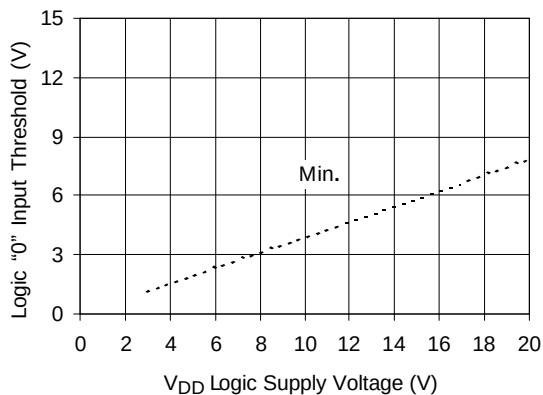


Figure 13B. Logic "0" Input Threshold vs. Voltage

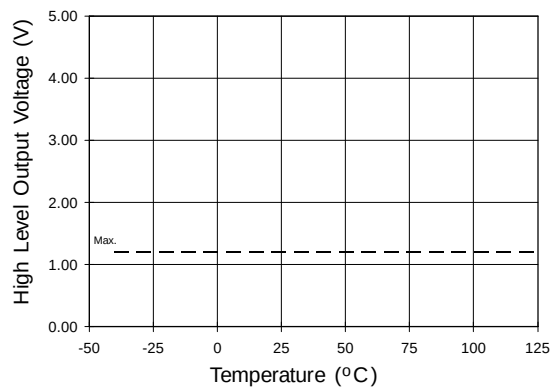


Figure 14A. High Level Output vs. Temperature

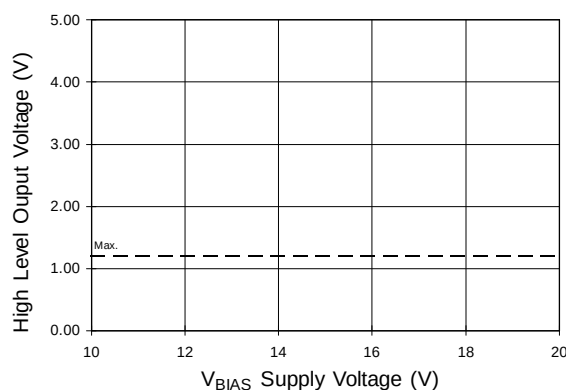


Figure 14B. High Level Output vs. Voltage

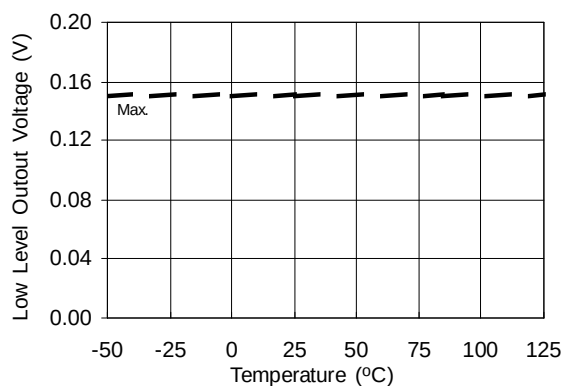


Figure 15A. Low Level Output vs. Temperature

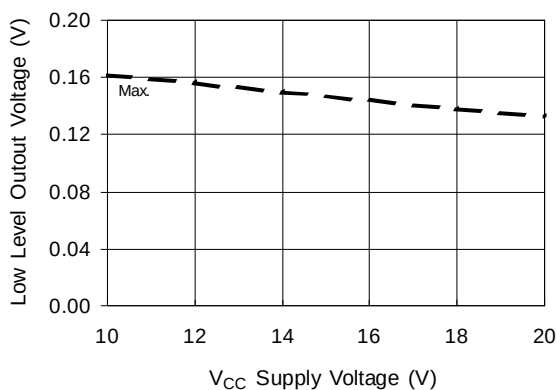


Figure 15B. Low Level Output vs. Supply Voltage

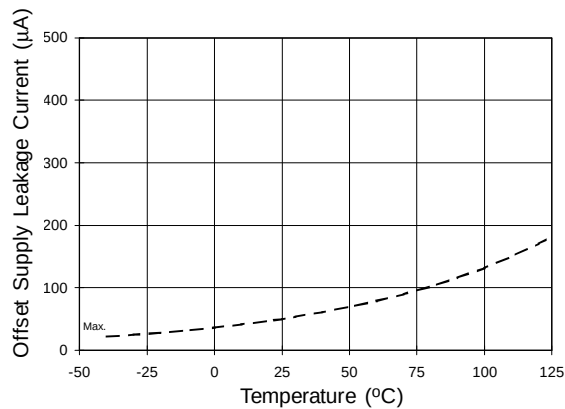


Figure 16A. Offset Supply Current vs. Temperature

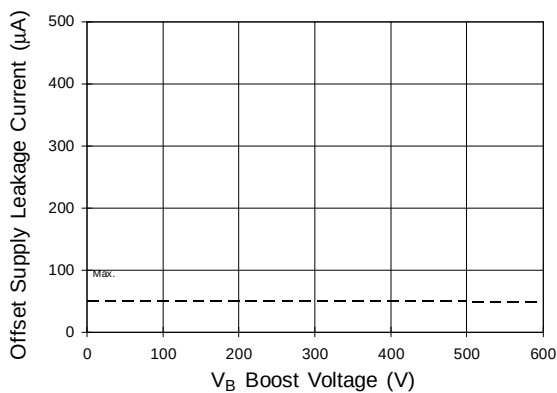


Figure 16B. Offset Supply Current vs. Voltage

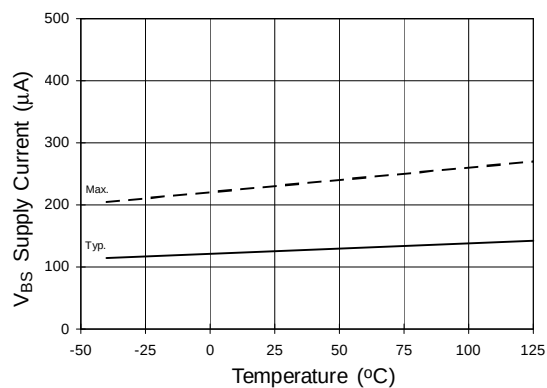


Figure 17A. V_{BS} Supply Current vs. Temperature

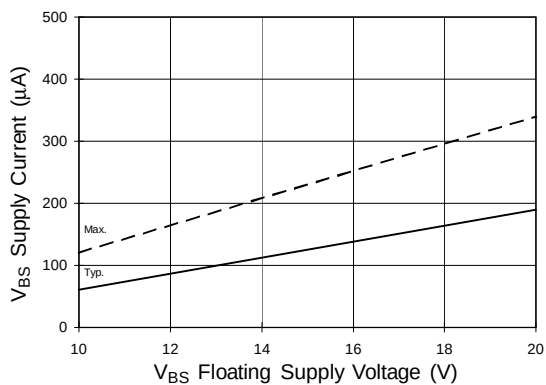


Figure 17B. V_{BS} Supply Current vs. Voltage

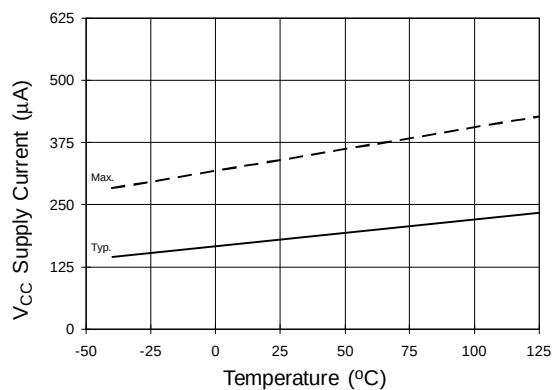


Figure 18A. V_{CC} Supply Current vs. Temperature

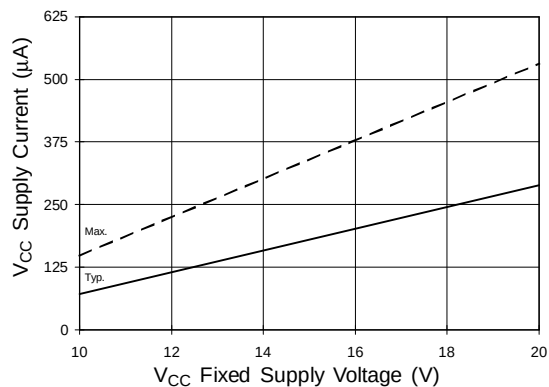


Figure 18B. V_{CC} Supply Current vs. Voltage

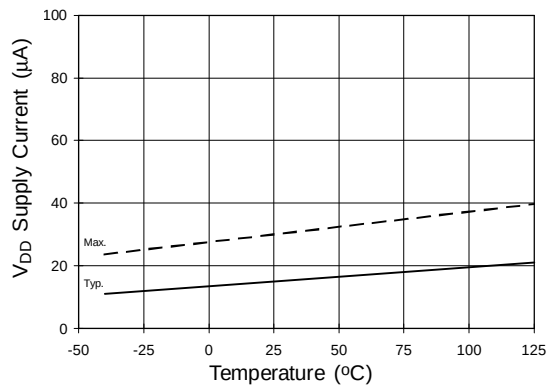


Figure 19A. V_{DD} Supply Current vs. Temperature

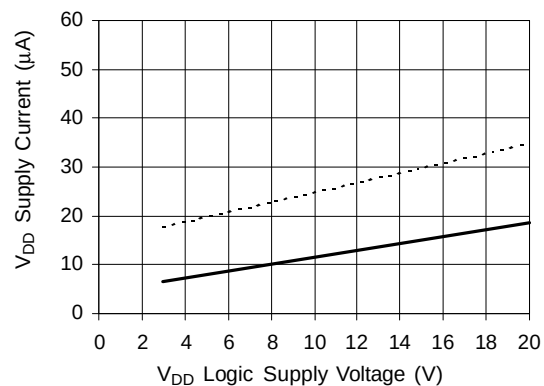


Figure 19B. V_{DD} Supply Current vs. V_{DD} Voltage

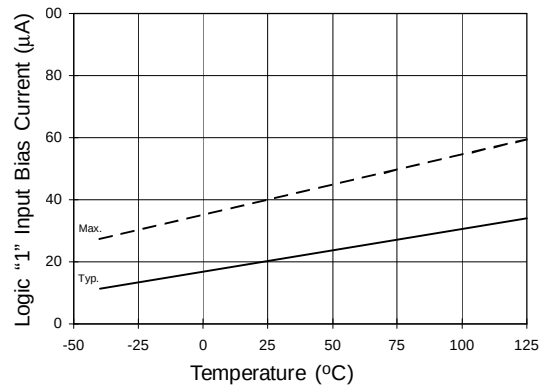


Figure 20A. Logic "1" Input Current vs. Temperature

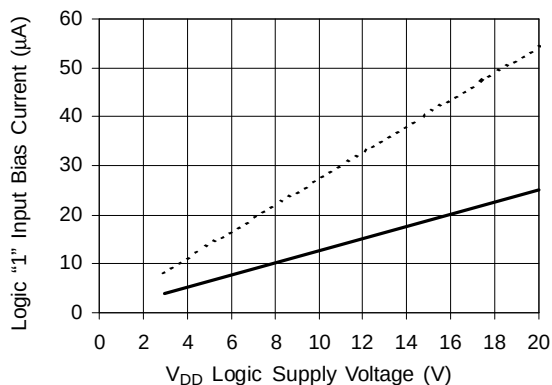


Figure 20B. Logic "1" Input Current vs. V_{DD} Voltage

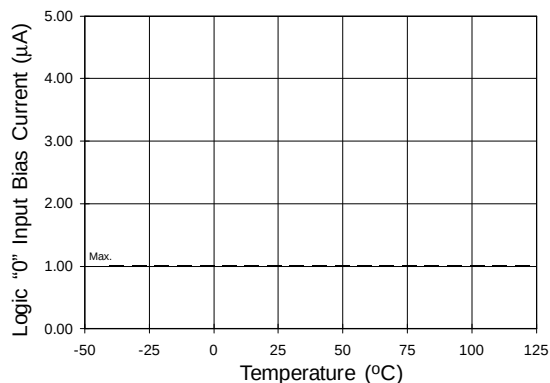


Figure 21A. Logic "0" Input Current vs. Temperature

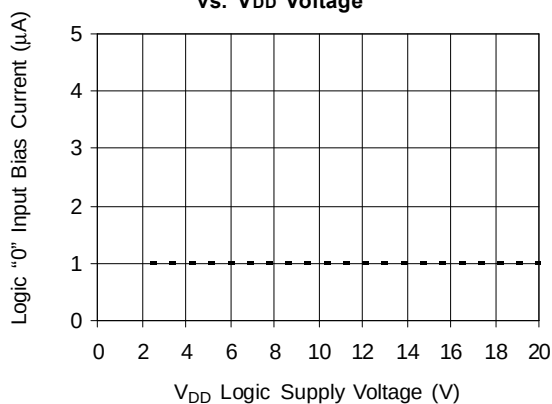


Figure 21B. Logic "0" Input Current vs. V_{DD} Voltage

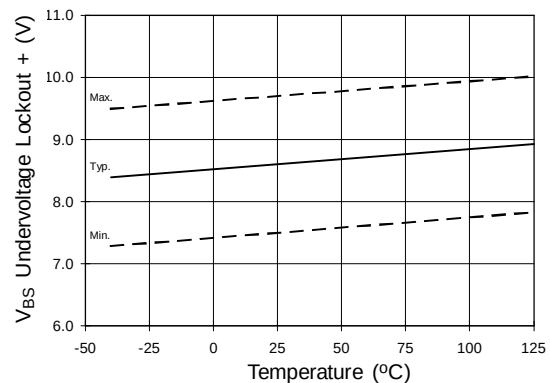


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

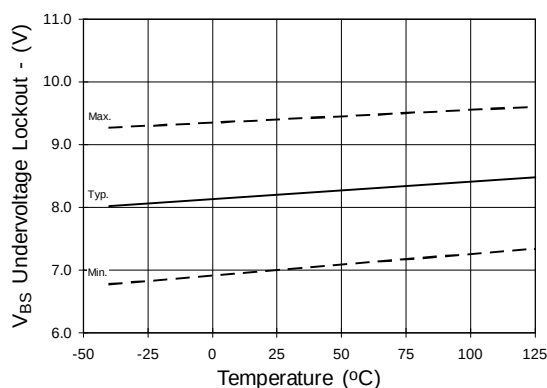


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

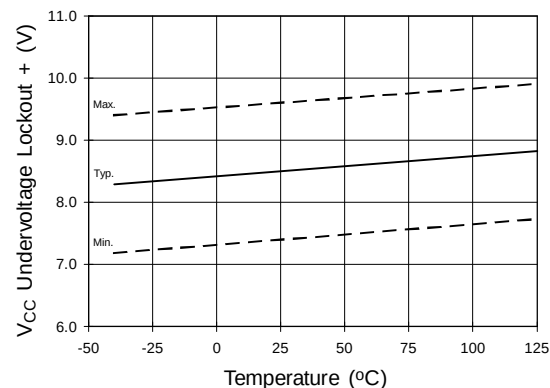


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

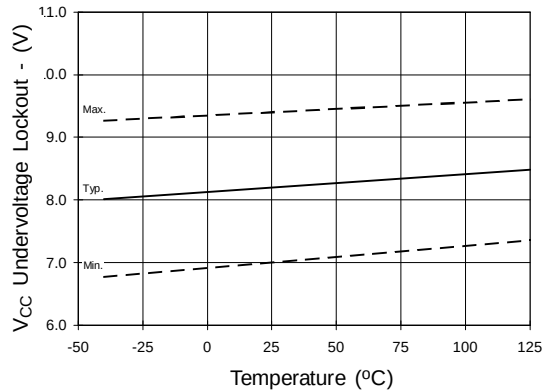


Figure 25. V_{CC} Undervoltage Lockout (-) vs. Temperature

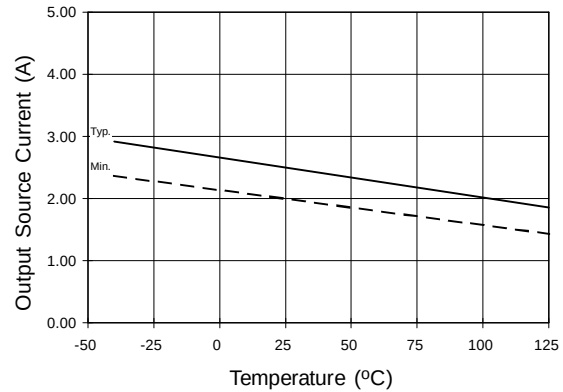


Figure 26A. Output Source Current vs. Temperature

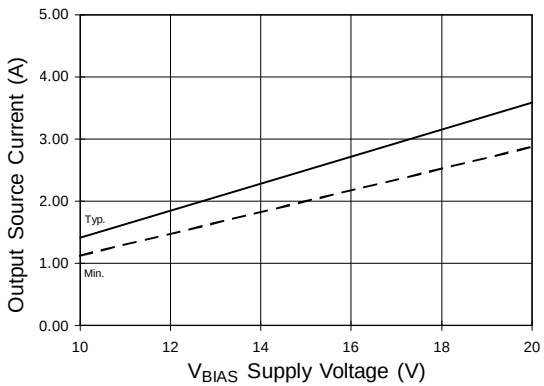


Figure 26B. Output Source Current vs. Voltage

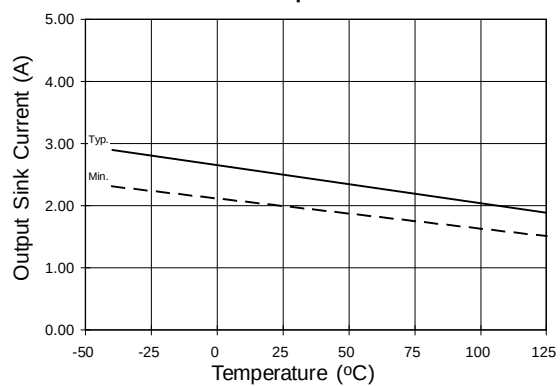


Figure 27A. Output Sink Current vs. Temperature

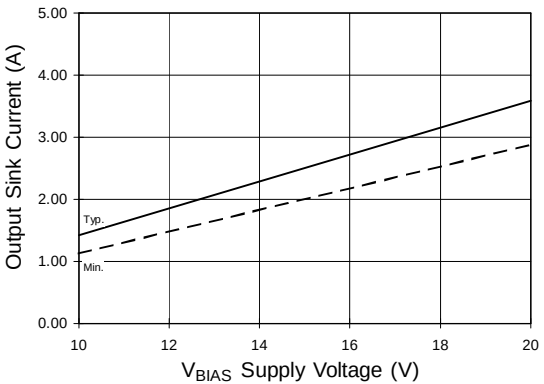


Figure 27B. Output Sink Current vs. Voltage

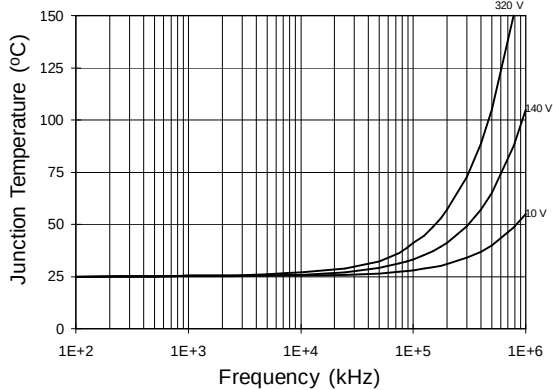


Figure 28. IRS2110/IRS2113 T_J vs. Frequency (IRFBC20) $R_{GATE} = 33 \Omega$, $V_{CC} = 15 \text{ V}$

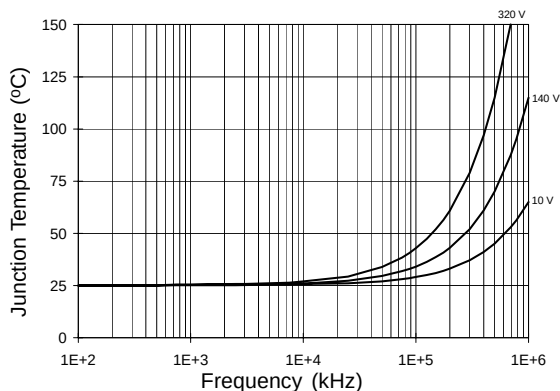


Figure 29. IRS2110/IRS2113 T_j vs. Frequency (IRFBC30) $R_{GATE} = 22 \Omega$, $V_{CC} = 15 V$

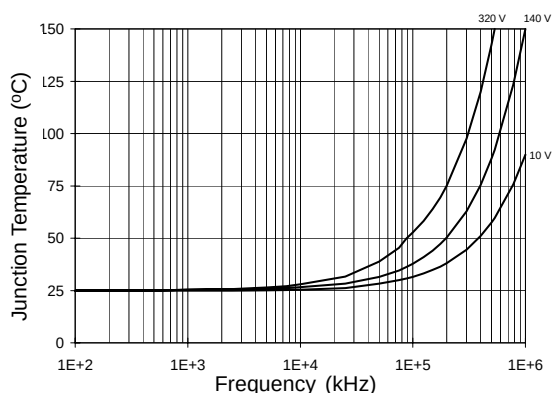


Figure 30. IRS2110/IRS2113 T_j vs. Frequency (IRFBC40) $R_{GATE} = 15 \Omega$, $V_{CC} = 15 V$

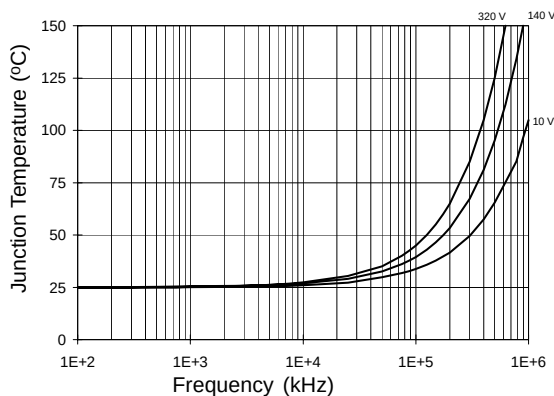


Figure 31. IRS2110/IRS2113 T_j vs. Frequency (IRFPE50) $R_{GATE} = 10 \Omega$, $V_{CC} = 15 V$

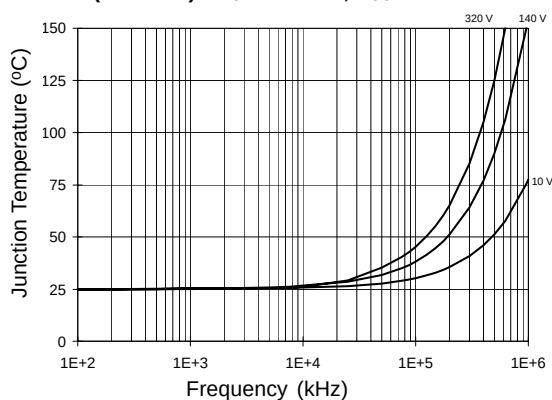


Figure 32. IRS2110S/IRS2113S T_j vs. Frequency (IRFBC20) $R_{GATE} = 33 \Omega$, $V_{CC} = 15 V$

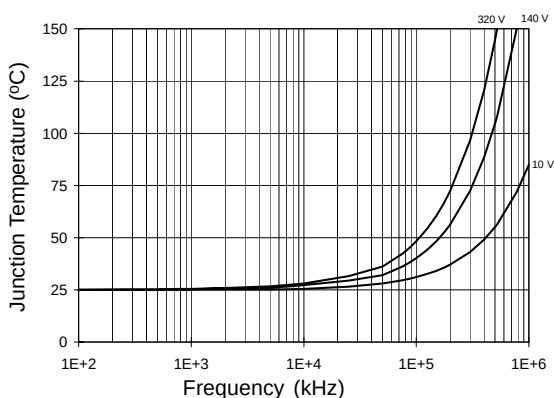


Figure 33. IRS2110S/IRS2113S T_j vs. Frequency (IRFBC30) $R_{GATE} = 22 \Omega$, $V_{CC} = 15 V$

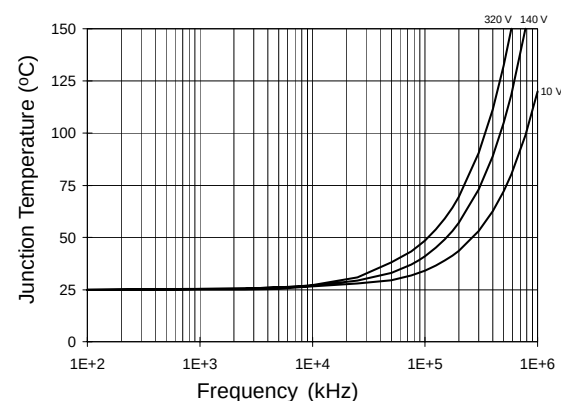


Figure 34. IRS2110S/IRS2113S T_j vs. Frequency (IRFBC40) $R_{GATE} = 15 \Omega$, $V_{CC} = 15 V$

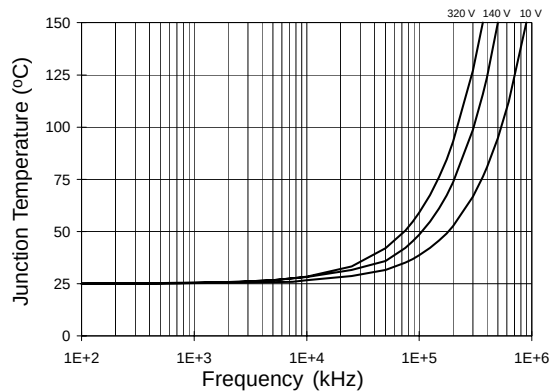


Figure 35. IRS2110S/IRS2113S T_J vs. Frequency (IRFPE50) $R_{GATE} = 10 \Omega$, $V_{CC} = 15 V$

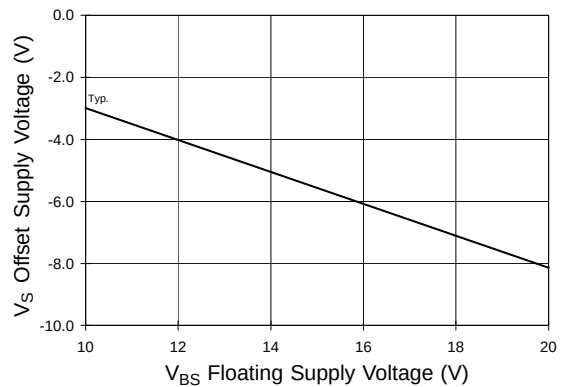


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

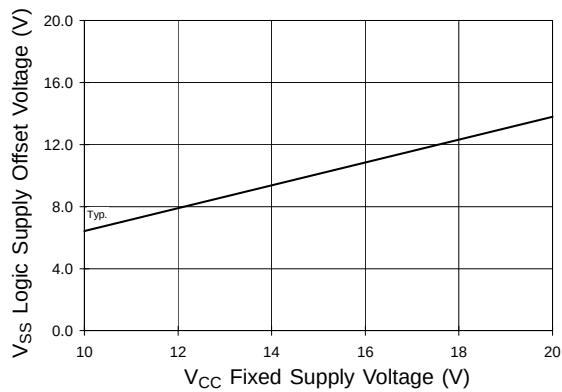
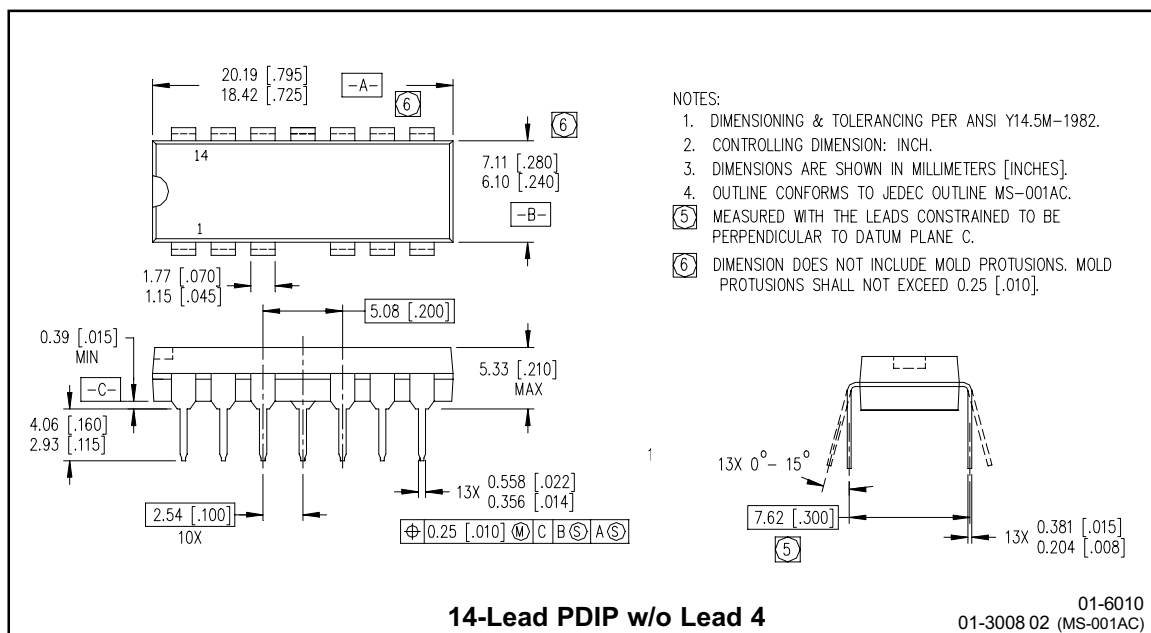
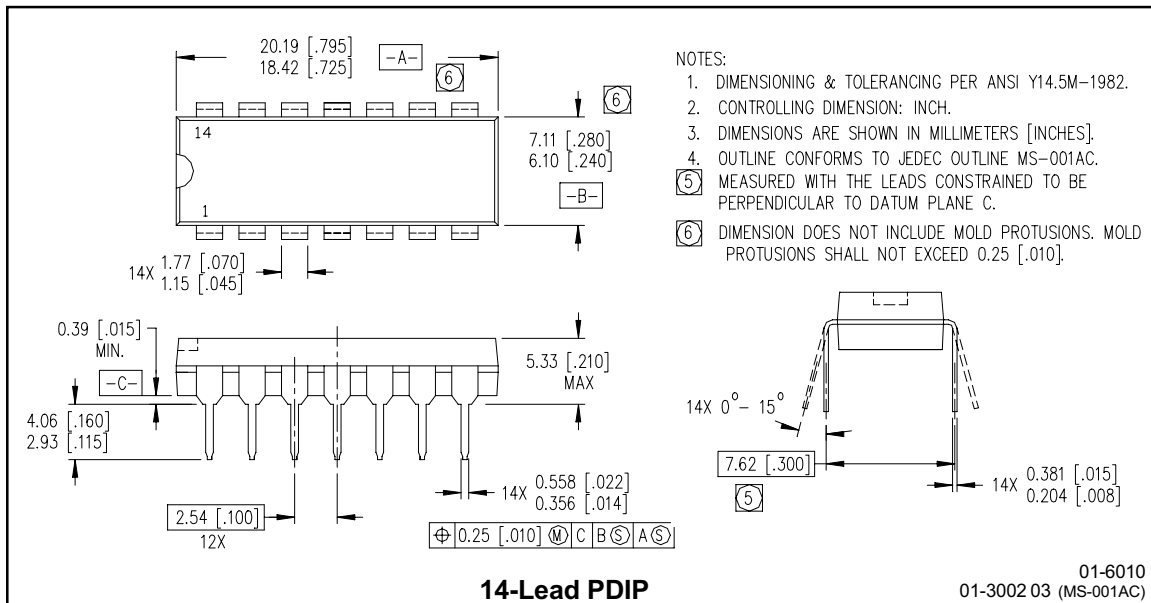
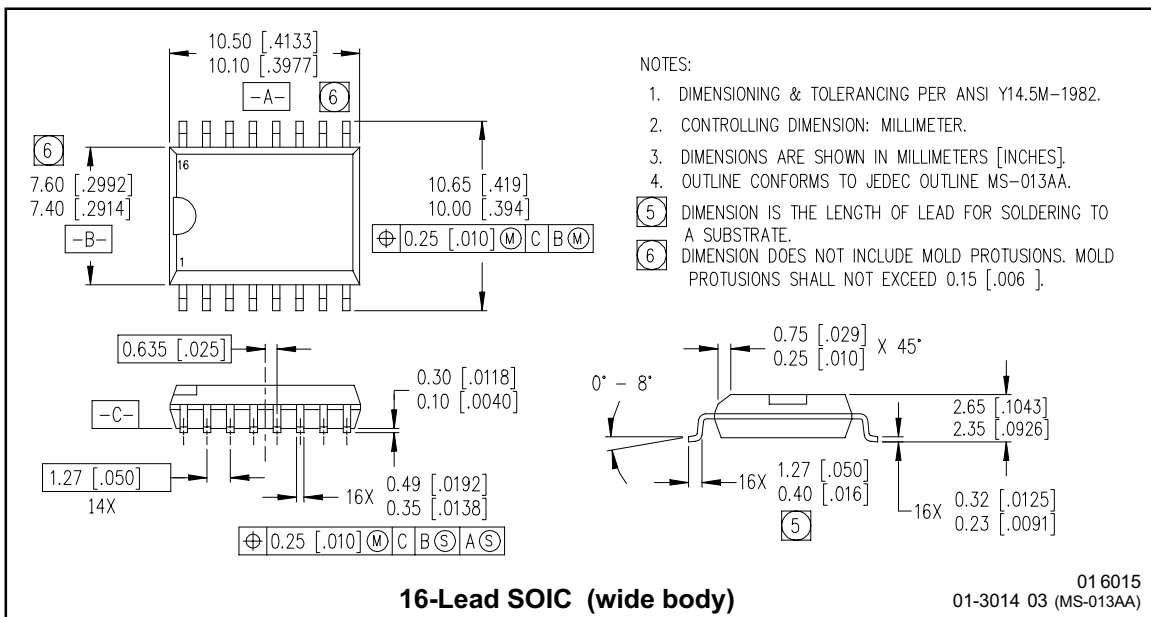
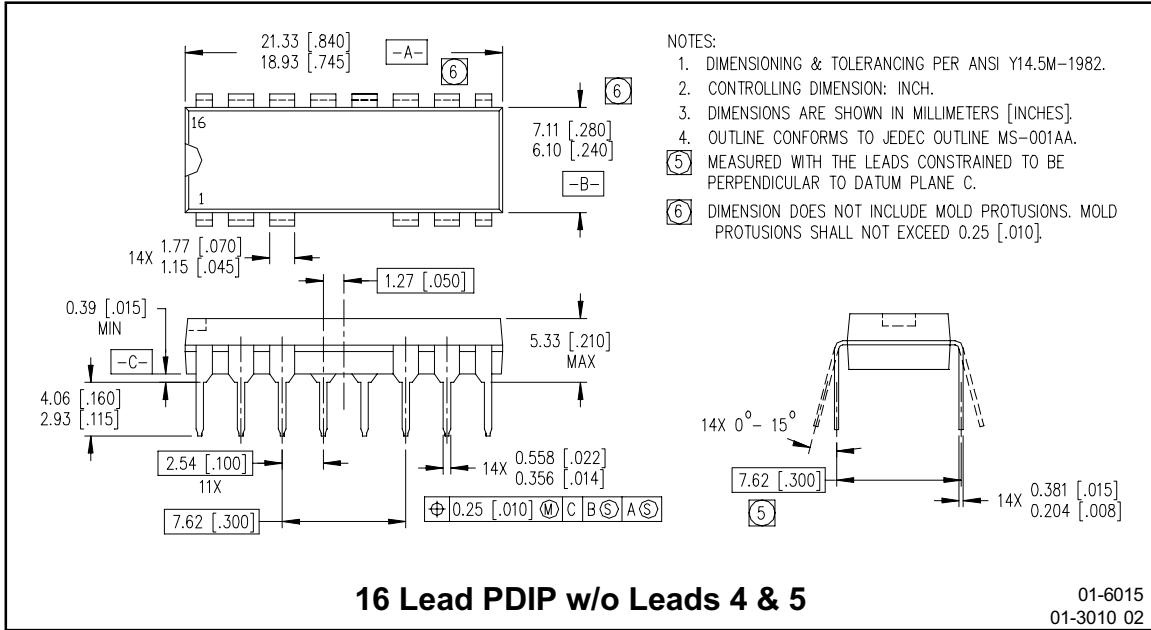


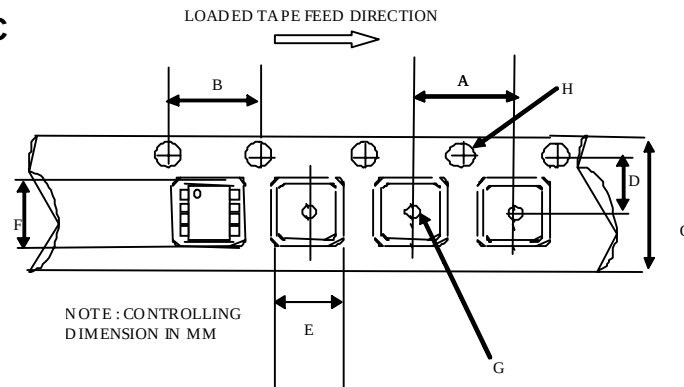
Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

Case Outlines



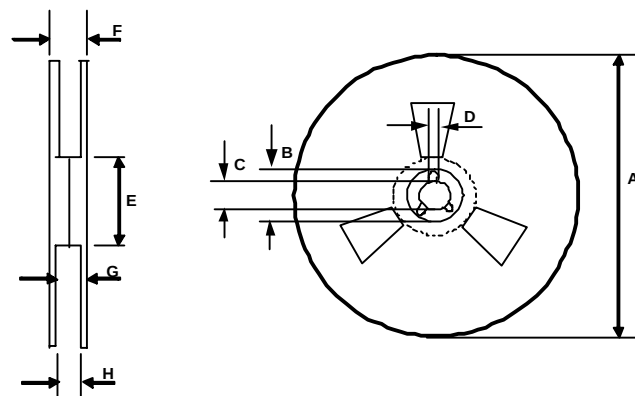


Tape & Reel
16-Lead SOIC



CARRIER TAPE DIMENSION FOR 16SOICW

Code	Metric		Imperial	
	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	10.80	11.00	0.425	0.433
F	10.60	10.80	0.417	0.425
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

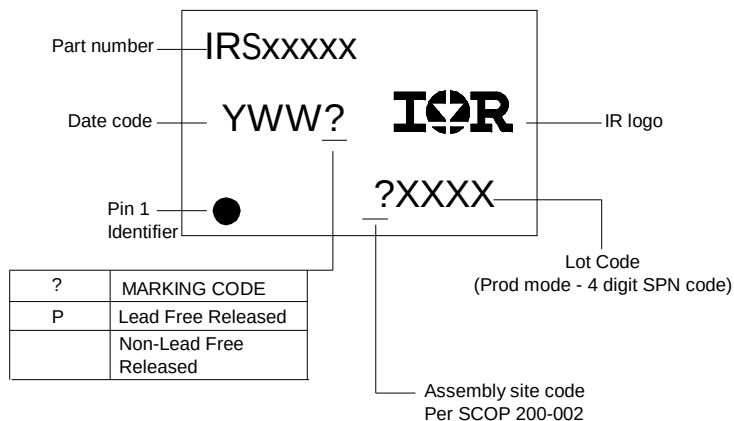


REEL DIMENSIONS FOR 16SOICW

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

IRS2110(-1,-2,S)PbF/IRS2113(-1,-2,S)PbF

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

14-Lead PDIP IRS2110PbF
 14-Lead PDIP IRS2110-1PbF
 14-Lead PDIP IRS2113PbF
 14-Lead PDIP IRS2113-1PbF
 16-Lead PDIP IRS2110-2PbF
 16-Lead PDIP IRS2113-2PbF
 16-Lead SOIC IRS2110SPbF
 16-Lead SOIC IRS2113SPbF
 16-Lead SOIC Tape & Reel IRS2110STRPbF
 16-Lead SOIC Tape & Reel IRS2113STRPbF