

74HC595; 74HCT595

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

Rev. 7 — 26 January 2015

Product data sheet

1. General description

The 74HC595; 74HCT595 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74HC595; 74HCT595 are 8-stage serial shift registers with a storage register and 3-state outputs. The registers have separate clocks.

Data is shifted on the positive-going transitions of the shift register clock input (SHCP). The data in each register is transferred to the storage register on a positive-going transition of the storage register clock input (STCP). If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (DS) and a serial standard output (Q7S) for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW.

2. Features and benefits

- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typical) shift out frequency
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Applications

- Serial-to-parallel data conversion
- Remote control holding register



4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC595N	−40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT595N				
74HC595D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT595D				
74HC595DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT595DB				
74HC595PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT595PW				
74HC595BQ	−40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT595BQ				

5. Functional diagram

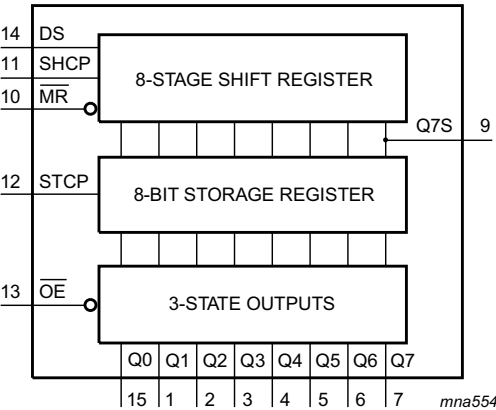


Fig 1. Functional diagram

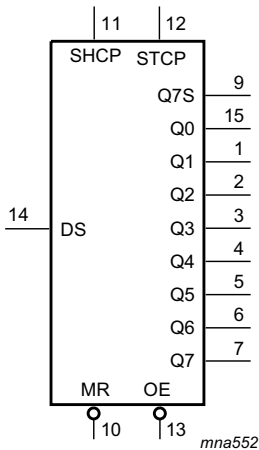


Fig 2. Logic symbol

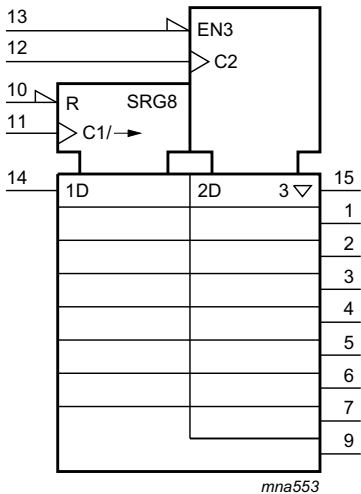


Fig 3. IEC logic symbol

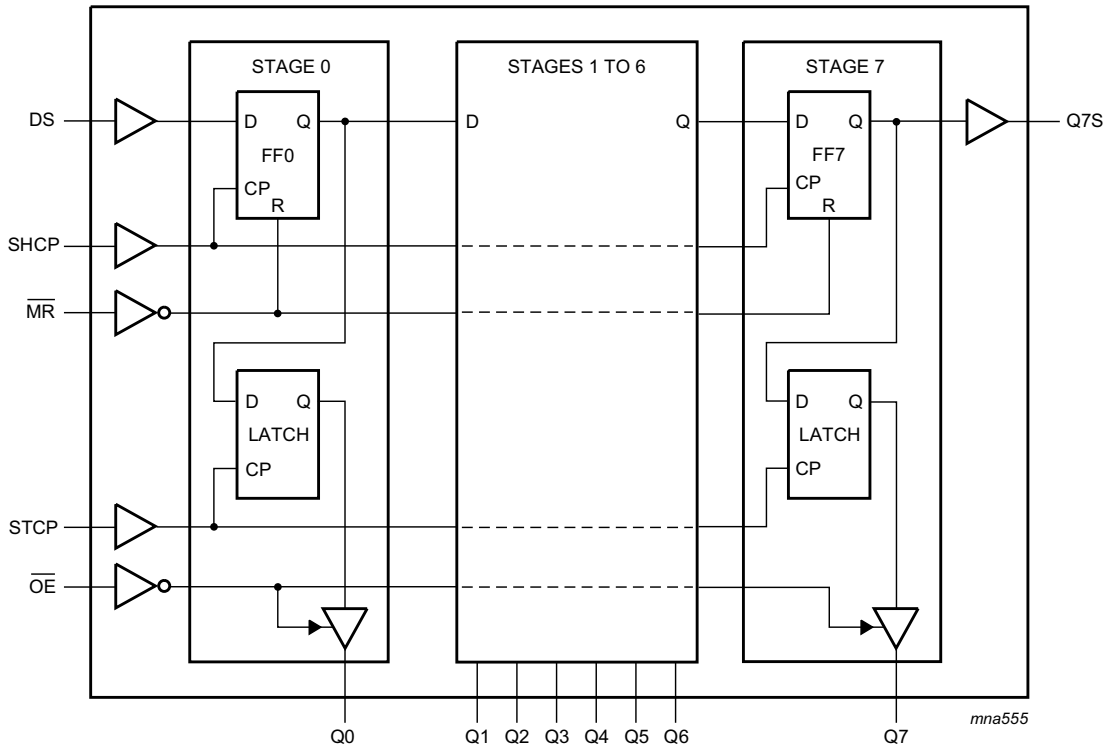
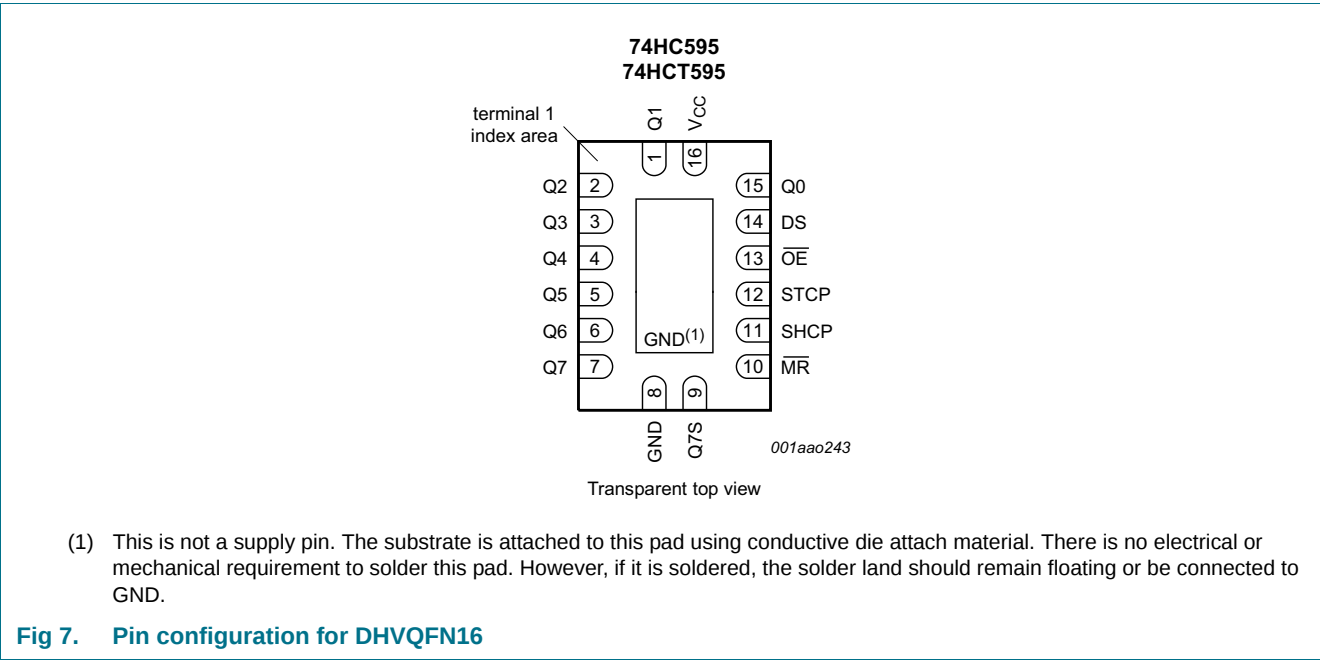
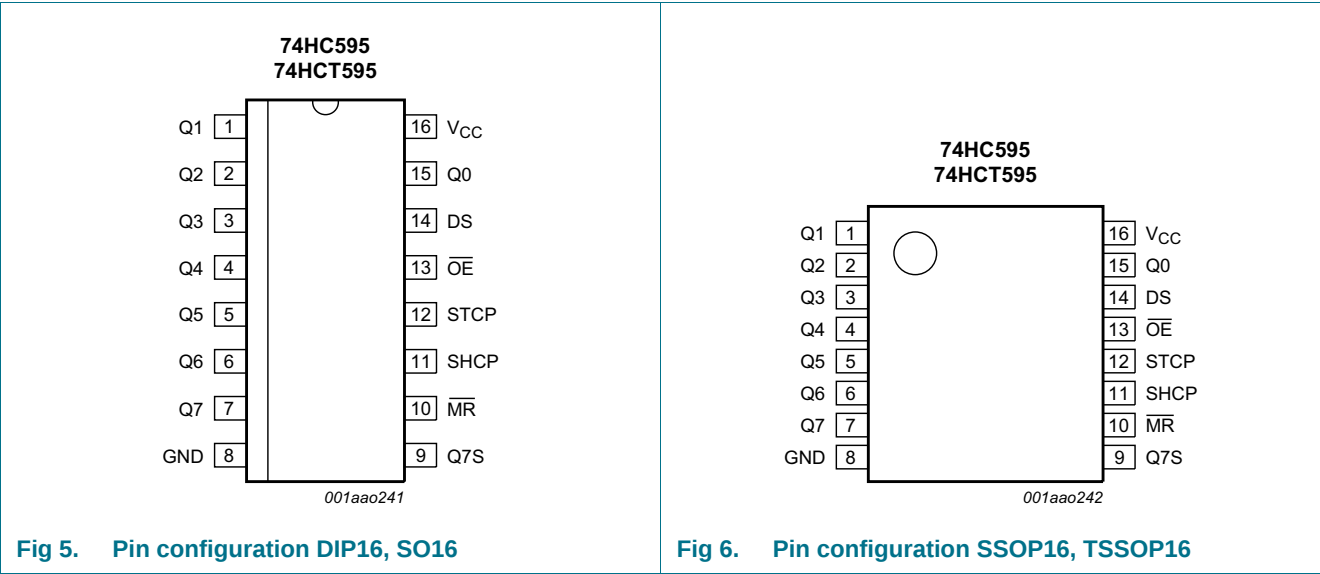


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q1	1	parallel data output 1
Q2	2	parallel data output 2
Q3	3	parallel data output 3
Q4	4	parallel data output 4
Q5	5	parallel data output 5
Q6	6	parallel data output 6
Q7	7	parallel data output 7
GND	8	ground (0 V)
Q7S	9	serial data output
$\overline{\text{MR}}$	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
$\overline{\text{OE}}$	13	output enable input (active LOW)
DS	14	serial data input
Q0	15	parallel data output 0
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table^[1]

Control				Input	Output		Function
SHCP	STCP	$\overline{\text{OE}}$	$\overline{\text{MR}}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on $\overline{\text{MR}}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

- [1] H = HIGH voltage state;
 L = LOW voltage state;
 ↑ = LOW-to-HIGH transition;
 X = don't care;
 NC = no change;
 Z = high-impedance OFF-state.

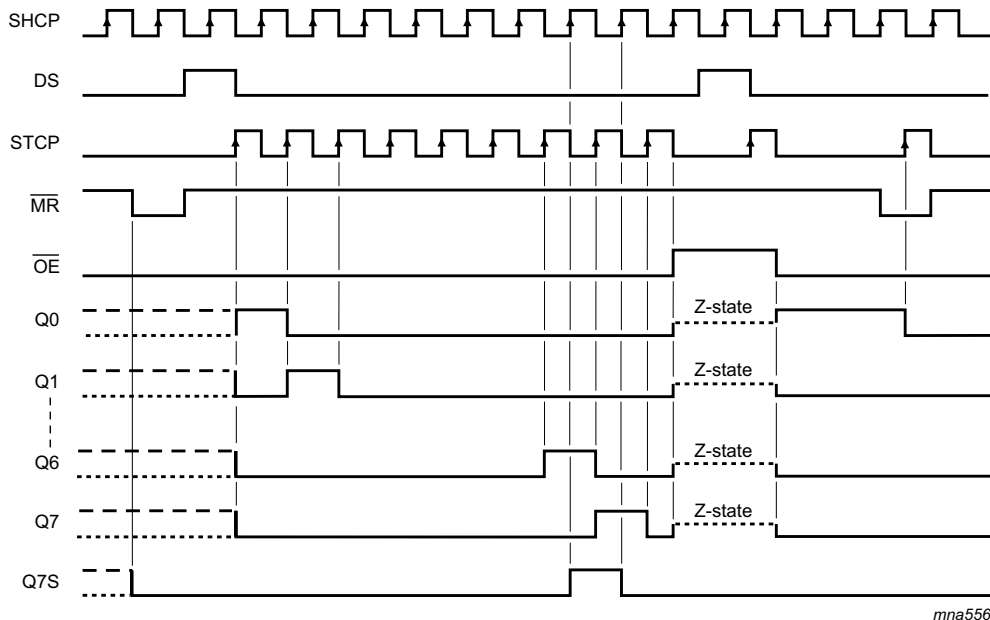


Fig 8. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$	-	± 20	mA
I_O	output current	$V_O = -0.5 \text{ V}$ to $(V_{CC} + 0.5 \text{ V})$			
		pin Q7S	-	± 25	mA
		pins Qn	-	± 35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	DIP16 package [1]	-	750	mW
		SO16 package [2]	-	500	mW
		SSOP16 package [3]	-	500	mW
		TSSOP16 package [3]	-	500	mW
		DHVQFN16 package [4]	-	500	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN16 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC595			74HCT595			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC595								
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		all outputs						
		I _O = −20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I _O = −20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = −20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		Q7S output						
		I _O = −4 mA; V _{CC} = 4.5 V	3.84	4.32	-	3.7	-	V
		I _O = −5.2 mA; V _{CC} = 6.0 V	5.34	5.81	-	5.2	-	V
		Qn bus driver outputs						
		I _O = −6 mA; V _{CC} = 4.5 V	3.84	4.32	-	3.7	-	V
I _O = −7.8 mA; V _{CC} = 6.0 V	5.34	5.81	-	5.2	-	V		

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		all outputs						
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	V
		Q7S output						
		I _O = 4 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
		Qn bus driver outputs						
		I _O = 6 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I _O = 7.8 mA; V _{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	-	±1.0	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 6.0 V; V _O = V _{CC} or GND	-	-	±5.0	-	±10	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	80	-	160	µA
C _I	input capacitance		-	3.5	-	-	-	pF
74HCT595								
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V						
		all outputs						
		I _O = -20 µA	4.4	4.5	-	4.4	-	V
		Q7S output						
		I _O = -4 mA	3.84	4.32	-	3.7	-	V
		Qn bus driver outputs						
		I _O = -6 mA	3.7	4.32	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V						
		all outputs						
		I _O = 20 µA	-	0	0.1	-	0.1	V
		Q7S output						
		I _O = 4.0 mA	-	0.15	0.33	-	0.4	V
		Qn bus driver outputs						
		I _O = 6.0 mA	-	0.16	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±1.0	-	±1.0	µA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND	-	-	±5.0	-	±10	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	80	-	160	μA
ΔI_{CC}	additional supply current	per input pin; $I_O = 0$ A; $V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V						
		pins $\overline{MR}$, SHCP, STCP, $\overline{OE}$	-	150	675	-	735	μA
		pin DS	-	25	113	-	123	μA
C_I	input capacitance		-	3.5	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 14](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
74HC595										
t _{pd}	propagation delay	SHCP to Q7S; see Figure 9 ^[2]								
		V _{CC} = 2 V	-	52	160	-	200	-	240	ns
		V _{CC} = 4.5 V	-	19	32	-	40	-	48	ns
		V _{CC} = 6 V	-	15	27	-	34	-	41	ns
		STCP to Qn; see Figure 10 ^[2]								
		V _{CC} = 2 V	-	55	175	-	220	-	265	ns
		V _{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V _{CC} = 6 V	-	16	30	-	37	-	45	ns
		$\overline{MR}$ to Q7S; see Figure 12 ^[3]								
		V _{CC} = 2 V	-	47	175	-	220	-	265	ns
		V _{CC} = 4.5 V	-	17	35	-	44	-	53	ns
		V _{CC} = 6 V	-	14	30	-	37	-	45	ns
t _{en}	enable time	$\overline{OE}$ to Qn; see Figure 13 ^[4]								
		V _{CC} = 2 V	-	47	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	17	30	-	38	-	45	ns
		V _{CC} = 6 V	-	14	26	-	33	-	38	ns
t _{dis}	disable time	$\overline{OE}$ to Qn; see Figure 13 ^[5]								
		V _{CC} = 2 V	-	41	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	15	30	-	38	-	45	ns
		V _{CC} = 6 V	-	12	27	-	33	-	38	ns

Table 7. Dynamic characteristics ...continuedVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 14](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
t _w	pulse width	SHCP HIGH or LOW; see Figure 9								
		V _{CC} = 2 V	75	17	-	95	-	110	-	ns
		V _{CC} = 4.5 V	15	6	-	19	-	22	-	ns
		V _{CC} = 6 V	13	5	-	16	-	19	-	ns
		STCP HIGH or LOW; see Figure 10								
		V _{CC} = 2 V	75	11	-	95	-	110	-	ns
		V _{CC} = 4.5 V	15	4	-	19	-	22	-	ns
		V _{CC} = 6 V	13	3	-	16	-	19	-	ns
		MR LOW; see Figure 12								
		V _{CC} = 2 V	75	17	-	95	-	110	-	ns
		V _{CC} = 4.5 V	15	6	-	19	-	22	-	ns
		V _{CC} = 6 V	13	5	-	16	-	19	-	ns
t _{su}	set-up time	DS to SHCP; see Figure 10								
		V _{CC} = 2 V	50	11	-	65	-	75	-	ns
		V _{CC} = 4.5 V	10	4	-	13	-	15	-	ns
		V _{CC} = 6 V	9	3	-	11	-	13	-	ns
		SHCP to STCP; see Figure 11								
		V _{CC} = 2 V	75	22	-	95	-	110	-	ns
		V _{CC} = 4.5 V	15	8	-	19	-	22	-	ns
		V _{CC} = 6 V	13	7	-	16	-	19	-	ns
t _h	hold time	DS to SHCP; see Figure 11								
		V _{CC} = 2 V	3	–6	-	3	-	3	-	ns
		V _{CC} = 4.5 V	3	–2	-	3	-	3	-	ns
		V _{CC} = 6 V	3	–2	-	3	-	3	-	ns
t _{rec}	recovery time	MR to SHCP; see Figure 12								
		V _{CC} = 2 V	50	–19	-	65	-	75	-	ns
		V _{CC} = 4.5 V	10	–7	-	13	-	15	-	ns
		V _{CC} = 6 V	9	–6	-	11	-	13	-	ns
f _{max}	maximum frequency	SHCP or STCP; see Figure 9 and 10								
		V _{CC} = 2 V	9	30	-	4.8	-	4	-	MHz
		V _{CC} = 4.5 V	30	91	-	24	-	20	-	MHz
		V _{CC} = 6 V	35	108	-	28	-	24	-	MHz
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} [6][7]	-	115	-	-	-	-	-	pF

Table 7. Dynamic characteristics ...continuedVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 14](#).

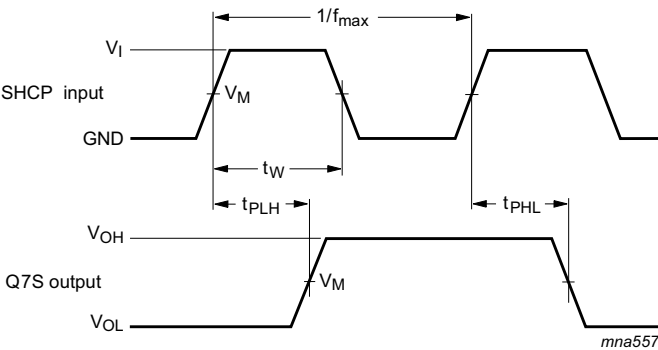
Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
74HCT595; V _{CC} = 4.5 V to 5.5 V										
t _{pd}	propagation delay	SHCP to Q7S; see Figure 9 ^[2]	-	25	42	-	53	-	63	ns
		STCP to Qn; see Figure 10 ^[2]	-	24	40	-	50	-	60	ns
		MR to Q7S; see Figure 12 ^[3]	-	23	40	-	50	-	60	ns
t _{en}	enable time	OE to Qn; see Figure 13 ^[4]	-	21	35	-	44	-	53	ns
t _{dis}	disable time	OE to Qn; see Figure 13 ^[5]	-	18	30	-	38	-	45	ns
t _w	pulse width	SHCP HIGH or LOW; see Figure 9	16	6	-	20	-	24	-	ns
		STCP HIGH or LOW; see Figure 10	16	5	-	20	-	24	-	ns
		MR LOW; see Figure 12	20	8	-	25	-	30	-	ns
t _{su}	set-up time	DS to SHCP; see Figure 10	16	5	-	20	-	24	-	ns
		SHCP to STCP; see Figure 11	16	8	-	20	-	24	-	ns
t _h	hold time	DS to SHCP; see Figure 11	3	–2	-	3	-	3	-	ns
t _{rec}	recovery time	MR to SHCP; see Figure 12	10	–7	-	13	-	15	-	ns
f _{max}	maximum frequency	SHCP and STCP; see Figure 9 and 10	30	52	-	24	-	20	-	MHz
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} – 1.5 V ^[6] ^[7]	-	130	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.[3] t_{pd} is the same as t_{PHL} only.[4] t_{en} is the same as t_{PZL} and t_{PZH}.[5] t_{dis} is the same as t_{PLZ} and t_{PHZ}.[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).P_D = C_{PD} × V_{CC}² × f_i + Σ(C_L × V_{CC}² × f_o) where:f_i = input frequency in MHz;f_o = output frequency in MHz;Σ(C_L × V_{CC}² × f_o) = sum of outputs;C_L = output load capacitance in pF;V_{CC} = supply voltage in V.

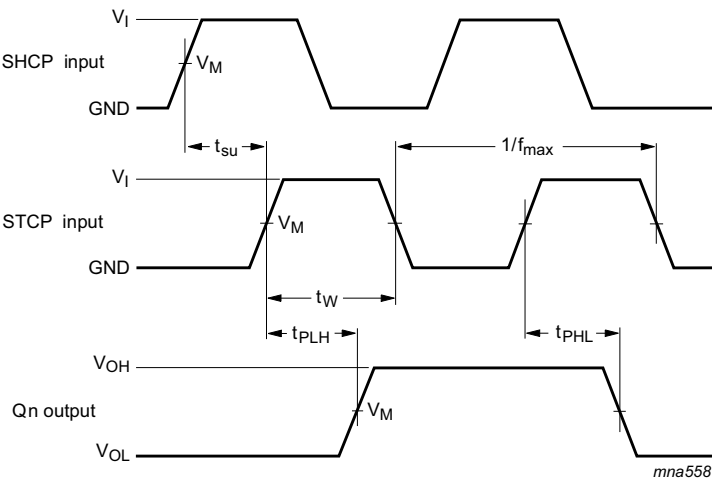
[7] All 9 outputs switching.

12. Waveforms



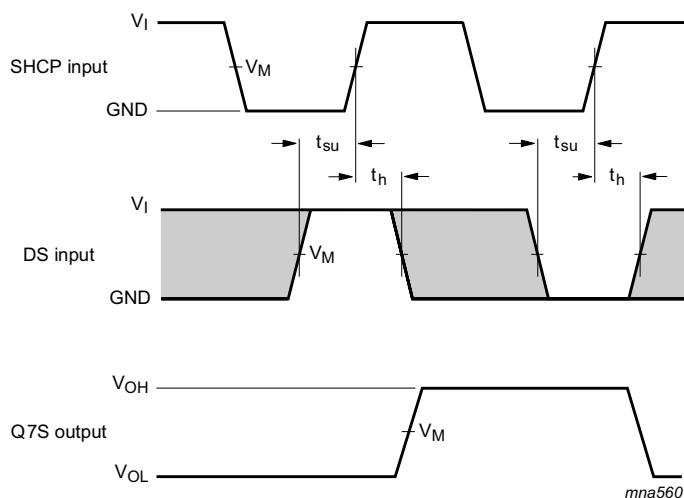
Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. Shift clock pulse, maximum frequency and input to output propagation delays



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 10. Storage clock to output propagation delays

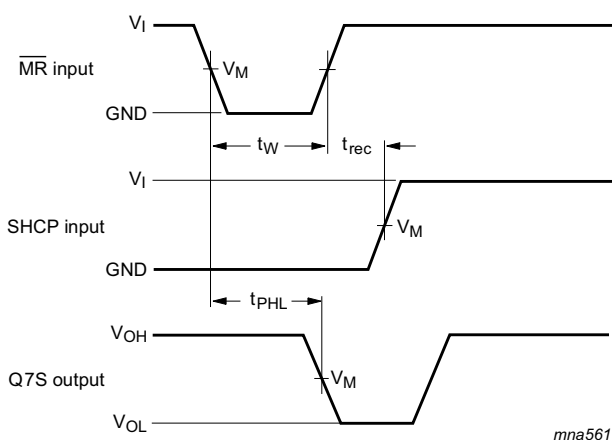


Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

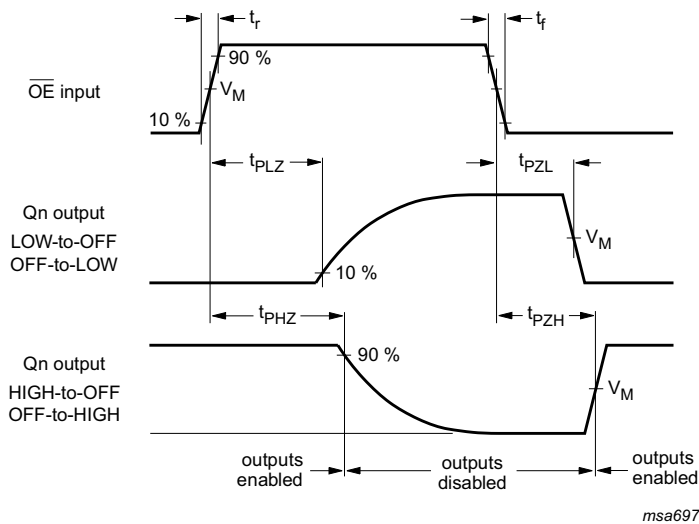
Fig 11. Data set-up and hold times



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 12. Master reset to output propagation delays



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 13. Enable and disable times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC595	$0.5V_{CC}$	$0.5V_{CC}$
74HCT595	1.3 V	1.3 V

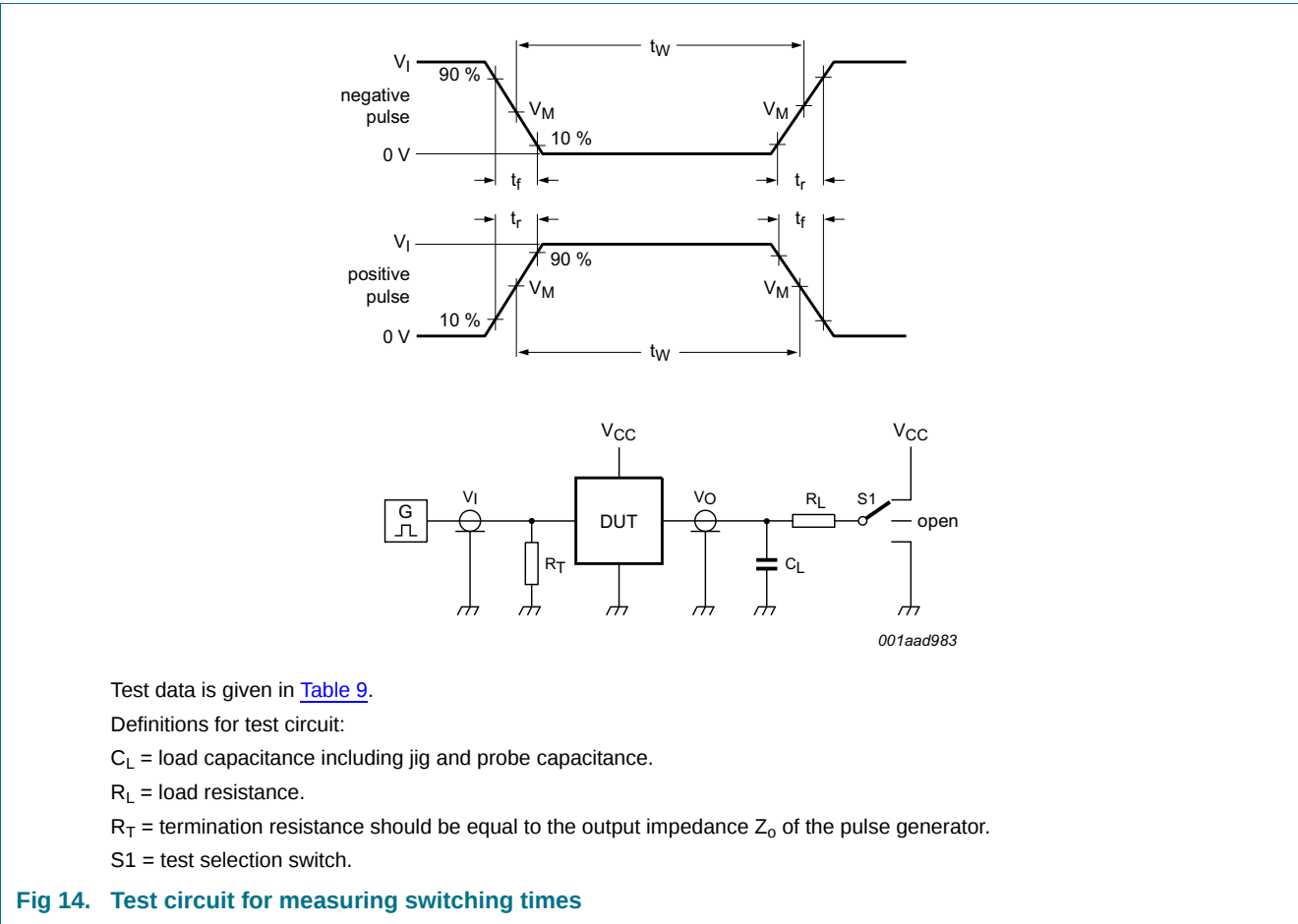


Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC595	V_{CC}	6 ns	50 pF	1 k Ω	open	GND	V_{CC}
74HCT595	3 V	6 ns	50 pF	1 k Ω	open	GND	V_{CC}

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

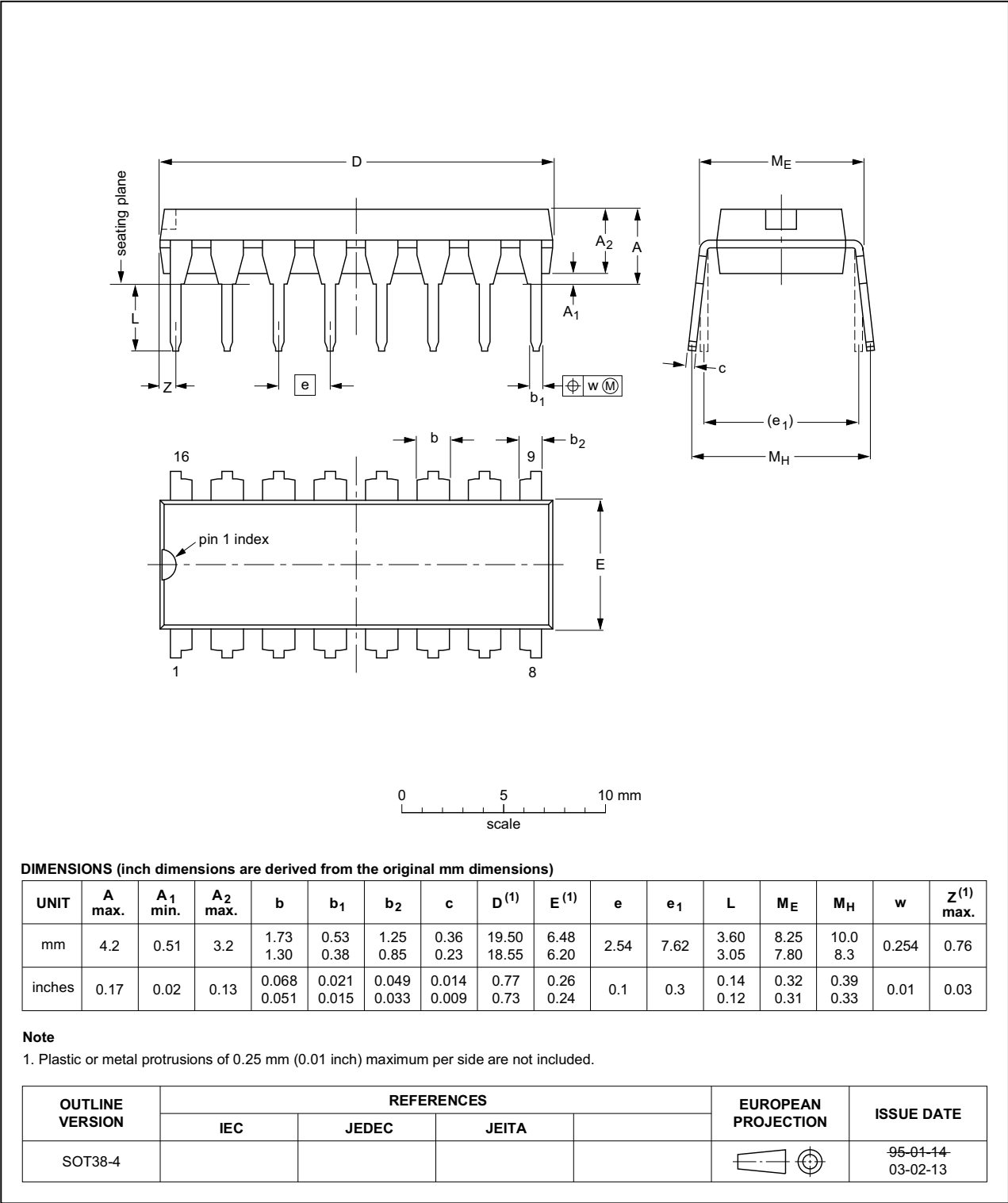


Fig 15. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

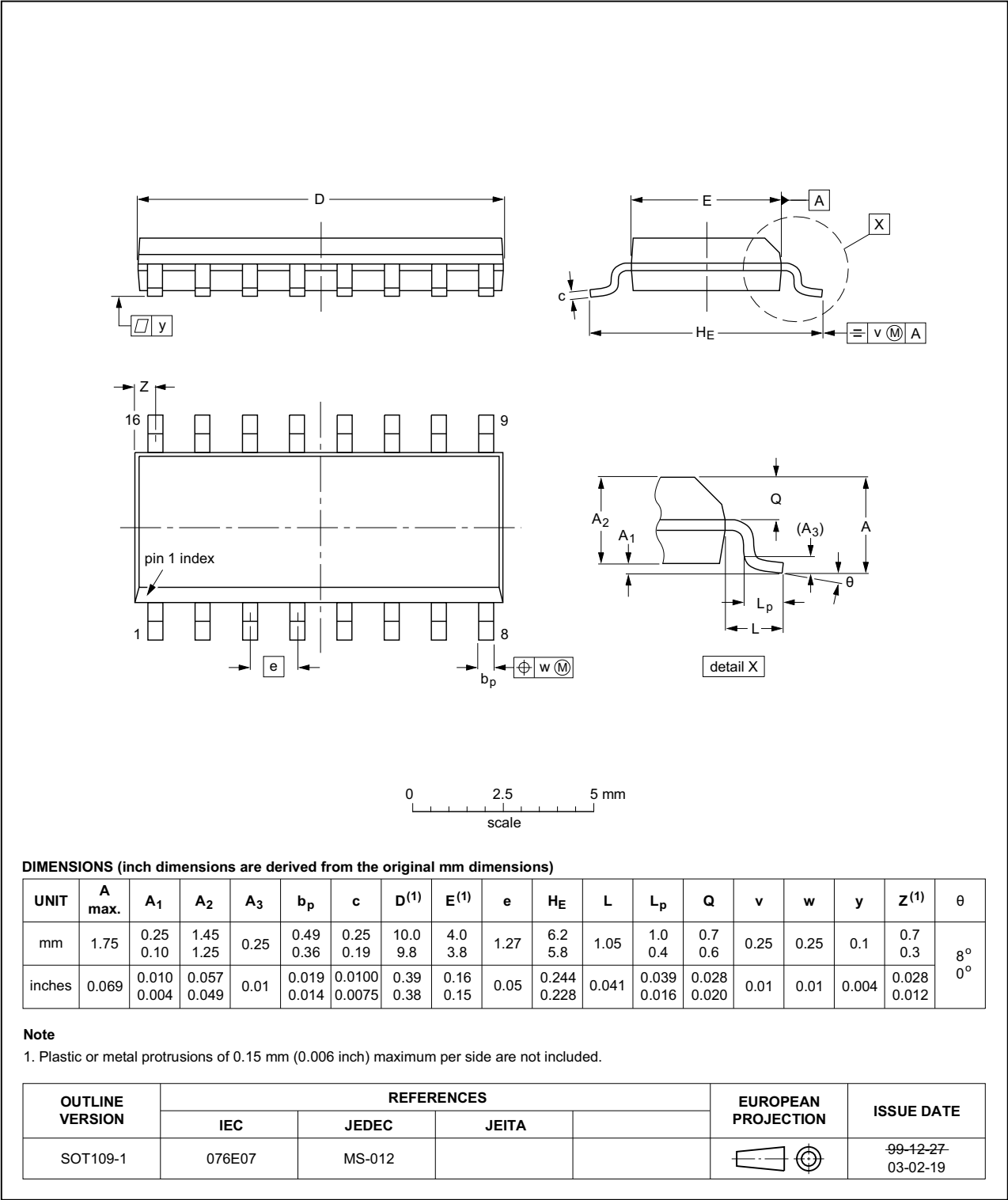


Fig 16. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

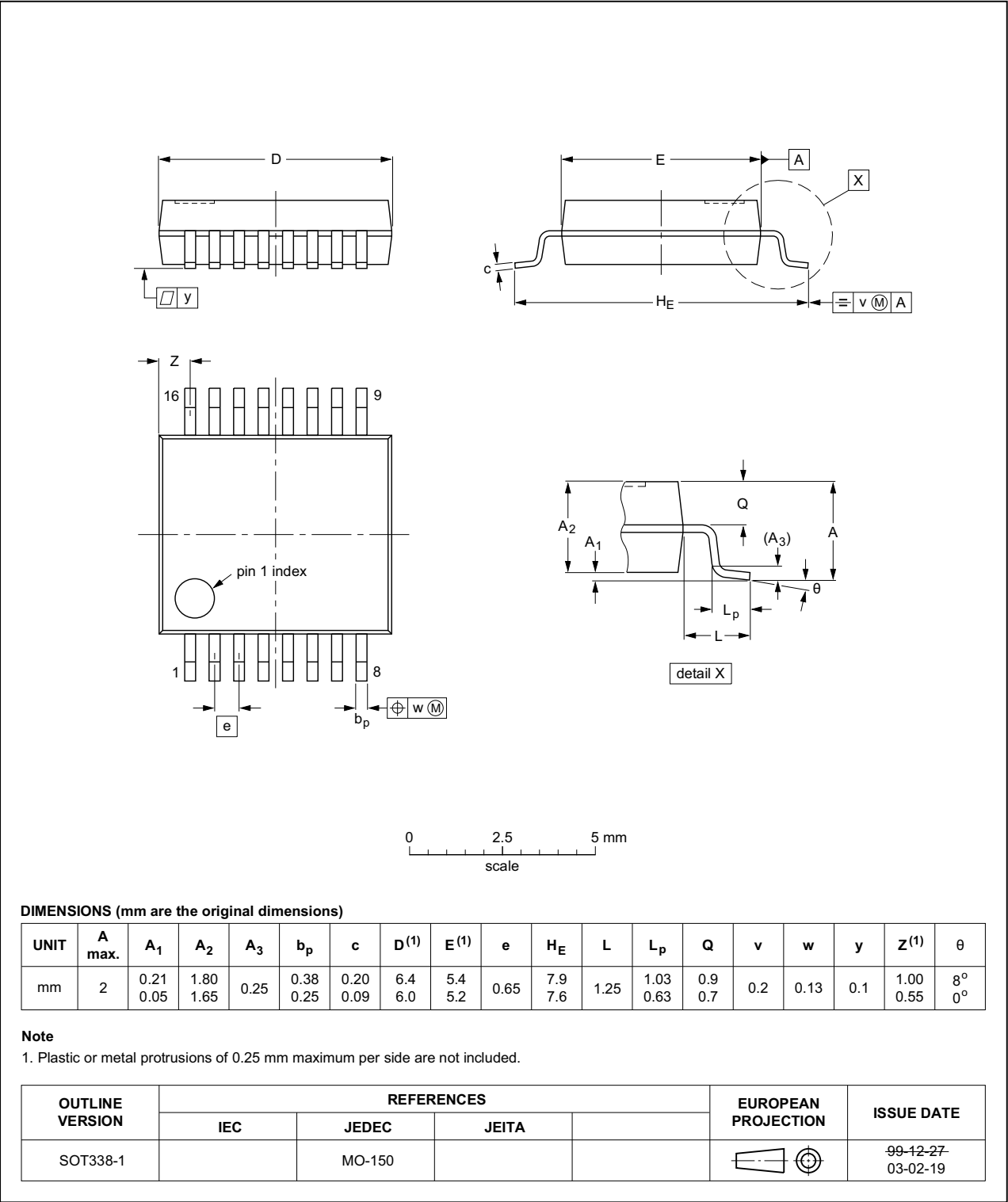


Fig 17. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

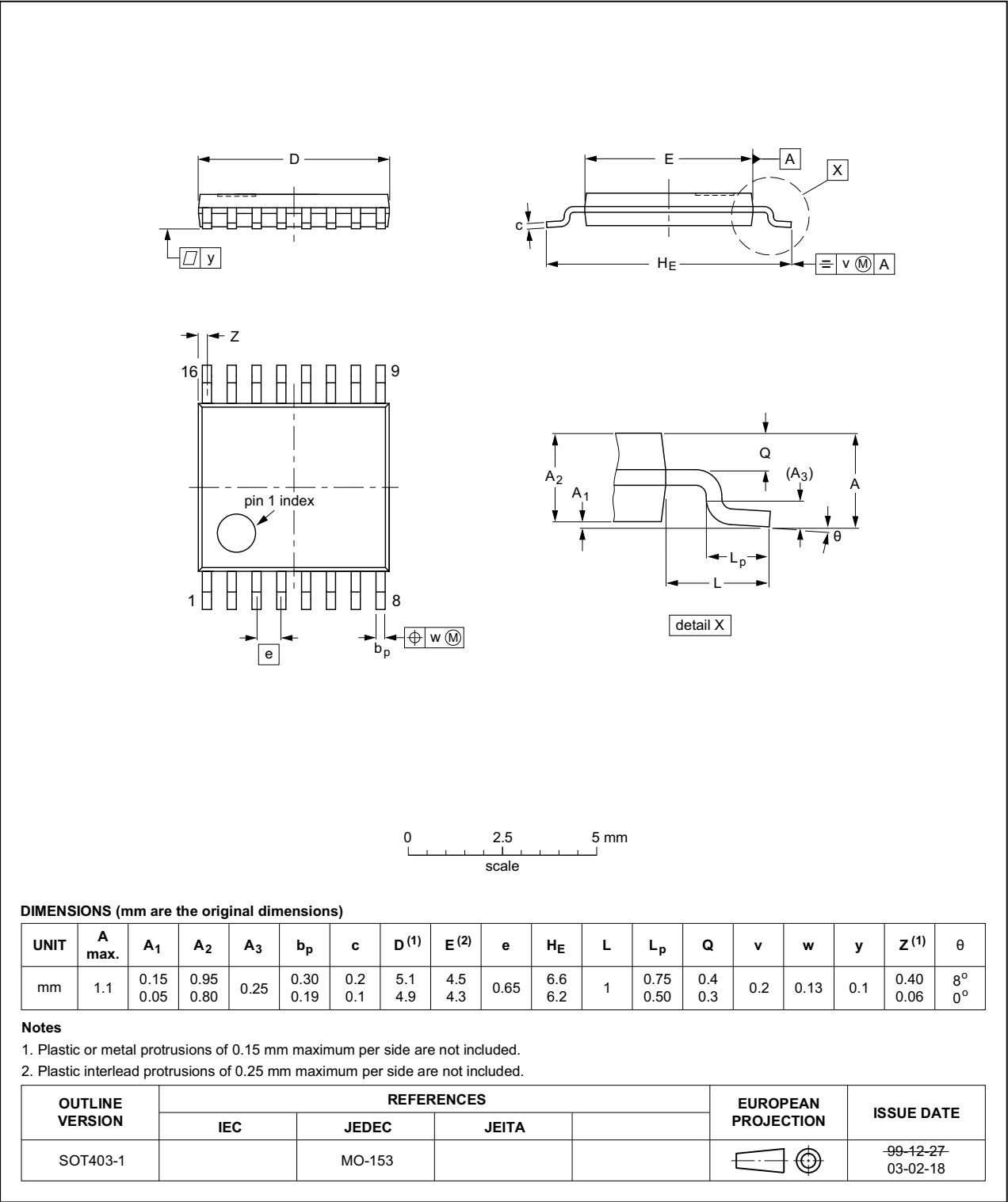


Fig 18. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

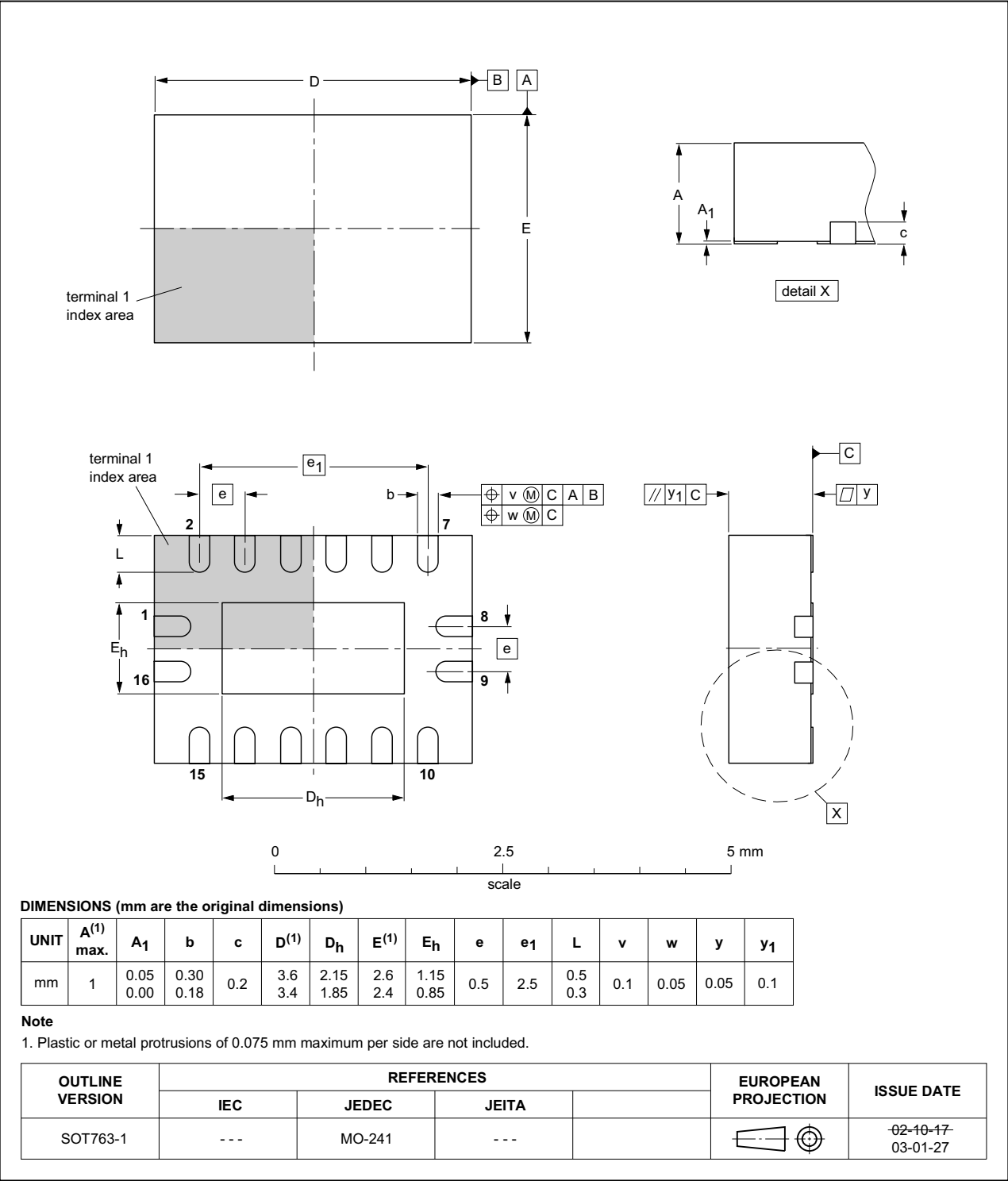


Fig 19. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Abbreviation
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT595 v.7	20150126	Product data sheet	-	74HC_HCT595 v.6
Modifications:	• Table 7 : Power dissipation capacitance condition for 74HCT595 is corrected.			
74HC_HCT595 v.6	20111212	Product data sheet	-	74HC_HCT595 v.5
Modifications:	• Legal pages updated.			
74HC_HCT595 v.5	20110628	Product data sheet	-	74HC_HCT595 v.4
74HC_HCT595 v.4	20030604	Product specification	-	74HC_HCT595_CNV v.3
74HC_HCT595_CNV v.3	19980604	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Date of release: 26 January 2015

Document identifier: 74HC_HCT595