

General Description

The MIC5012 is the dual member of the Micrel MIC501X driver family. These ICs are designed to drive the gate of an N-channel power MOSFET above the supply rail in high-side power switch applications. The 14-pin MIC5012 is extremely easy to use, requiring only a power FET and nominal supply decoupling to implement either a high- or low-side switch.

The MIC5012 charges a 1nF load in 60μs typical. Operation down to 4.75V allows the MIC5012 to drive standard MOSFETs in 5V low-side applications by boosting the gate voltage above the logic supply. In addition, multiple, paralleled MOSFETs can be driven by a single MIC5012 for ultra-high current applications.

Other members of the Micrel driver family include the MIC5010 full-featured driver, MIC5011 minimum parts count driver, and MIC5013 protected 8-pin driver.

For new designs, Micrel recommends the pin-compatible MIC5016 dual MOSFET driver.

Features

- 4.75V to 32V operation
- 2 independent drivers; implements high and low side drivers
- Less than 1μA standby current in the "off" state per channel
- Available in small outline SOIC packages
- Internal charge pump to drive the gate of an N-channel power FET above supply
- Internal zener clamp for gate protection
- Minimum external parts count
- Can be used to boost drive to low-side power FETs operating on logic supplies
- Independent supply pins for half-bridge applications

Applications

- Lamp drivers
- Motion Control
- Heater switching
- Power bus switching
- Half or full H-bridge drivers

Typical Applications

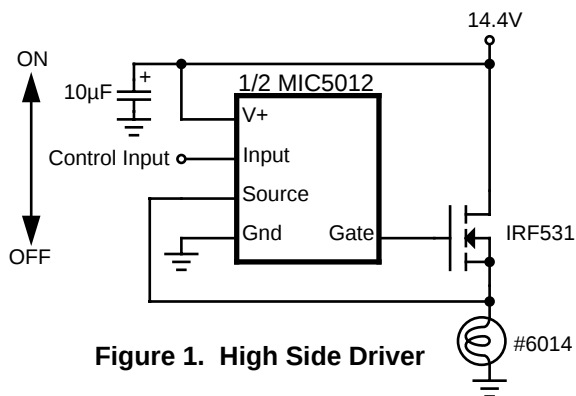


Figure 1. High Side Driver

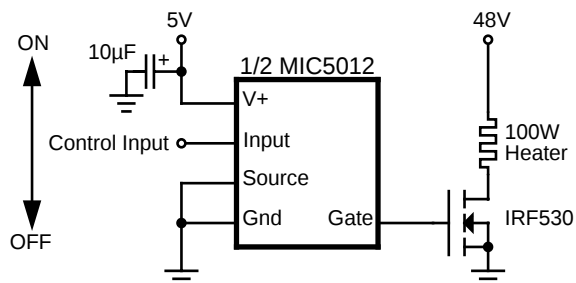


Figure 2. Low Side Driver

Ordering Information

Part Number	Temp. Range	Package
MIC5012BN	-40°C to +85°C	14-pin Plastic DIP
MIC5012BWM	-40°C to +85°C	16-pin Wide SOIC

Note: The MIC5012 is ESD sensitive.

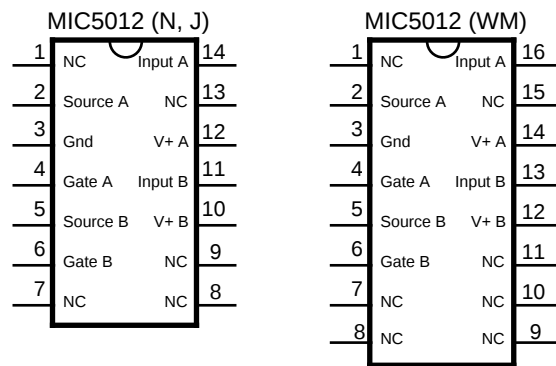
Protected under one or more of the following Micrel patents:
patent #4,951,101; patent #4,914,546

Absolute Maximum Ratings (Note 1, 2)			Operating Ratings (Notes 1, 2)	
Supply Voltage (V ⁺), Pins 10, 12	−0.5V to 36V		Power Dissipation	1.56W
Input Voltage, Pins 11, 14	−10V to V ⁺		θ _{JA} (Plastic DIP)	80 °C/W
Source Voltage, Pins 2, 5	−10V to V ⁺		θ _{JA} (SOIC)	105°C/W
Current into Pins 2, 5	50mA		Ambient Temperature: B version	−40°C to +85°C
Gate Voltage, Pins 4, 6	−1V to 50V		Storage Temperature	−65°C to +150°C
Junction Temperature	150°C		Lead Temperature	260°C
			(Soldering, 10 seconds)	
			Supply Voltage (V ⁺), Pin 1	4.75V to 32V high side 4.75V to 15V low side

Pin Description (Refer to Typical Applications)

DIP Pin Number	Pin Name	Pin Function
12, 10	V ⁺	Supply; must be decoupled to isolate from large transients caused by the power FET drain. 10μF is recommended close to pins 1 and 4.
14, 11	Input	Turns on power MOSFET when taken above threshold (3.5V typical). Requires <1 μA to switch.
2, 5	Source	Connects to source lead of power FET and is the return for the gate clamp zener. Can safely swing to −10V when turning off inductive loads.
3	Ground	
4, 6	Gate	Drives and clamps the gate of the power FET. Clamped to approximately −0.7V by an internal diode when turning off inductive loads.

Pin Configuration



Electrical Characteristics (Note 3) Test circuit. $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V^+ = 15\text{V}$, all switches open, unless otherwise specified.

Parameter	Conditions		Min	Typical	Max	Units
Supply Current (per section)	$V^+ = 32\text{V}$	$V_{IN} = 0\text{V}$, S2 closed		0.1	10	μA
		$V_{IN} = V_S = 32\text{V}$		8	20	mA
	$V^+ = 5\text{V}$	$V_{IN} = 5\text{V}$, S2 closed		1.6	4	mA
Logic Input Voltage	$V^+ = 4.75\text{V}$	Adjust V_{IN} for V_{GATE} low			2	V
		Adjust V_{IN} for V_{GATE} high	4.5			V
	$V^+ = 15\text{V}$	Adjust V_{IN} for V_{GATE} high	5.0			V
Logic Input Current, I_2	$V^+ = 32\text{V}$	$V_{IN} = 0\text{V}$	-1			μA
		$V_{IN} = 32\text{V}$			1	μA
Input Capacitance	Pins 11, 14			5		pF
Gate Drive, V_{GATE}	S1, S2 closed, $V_S = V^+$, $V_{IN} = 5\text{V}$	$V^+ = 4.75\text{V}$, $I_{GATE} = 0$, $V_{IN} = 4.5\text{V}$	7	10		V
		$V^+ = 15\text{V}$, $I_{GATE} = 100\mu\text{A}$, $V_{IN} = 5\text{V}$	24	27		V
Zener Clamp, $V_{GATE} - V_{SOURCE}$	S2 closed, $V_{IN} = 5\text{V}$	$V^+ = 15\text{V}$, $V_S = 15\text{V}$	11	12.5	15	V
		$V^+ = 32\text{V}$, $V_S = 32\text{V}$	11	13	16	V
Gate Turn-on Time, t_{ON} (Note 4)	V_{IN} switched from 0 to 5V; measure time for V_{GATE} to reach 20V			60	200	μs
Gate Turn-off Time, t_{OFF}	V_{IN} switched from 5 to 0V; measure time for V_{GATE} to reach 1V			4	10	μs

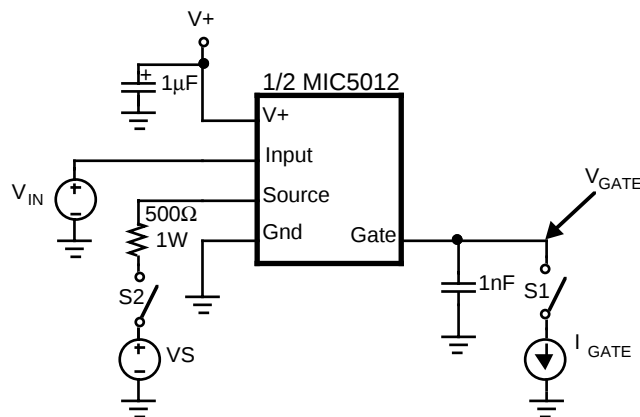
Note 1 **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2 The MIC5012 is ESD sensitive.

Note 3 Minimum and maximum **Electrical Characteristics** are 100% tested at $T_A = 25^\circ\text{C}$ and $T_A = 85^\circ\text{C}$, and 100% guaranteed over the entire range. Typicals are characterized at 25°C and represent the most likely parametric norm.

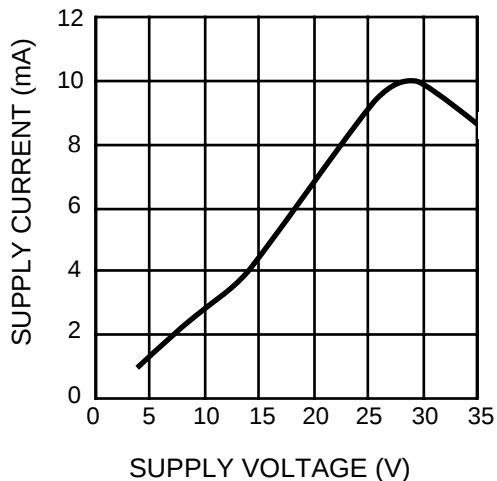
Note 4 Test conditions reflect worst case high-side driver performance. Low-side and bootstrapped topologies are significantly faster—see **Applications Information**. Maximum value of switching speed seen at 125°C , units operated at room temperature will reflect the typical values shown.

Test Circuit

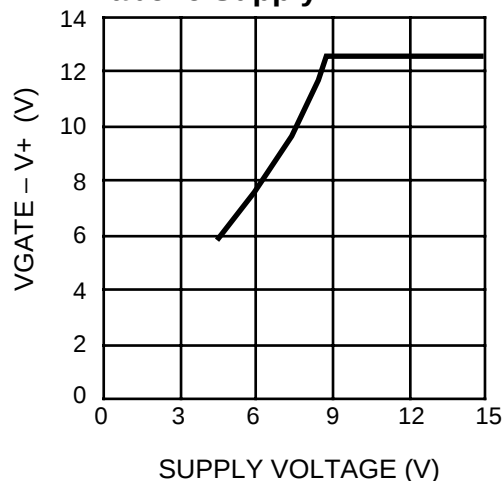


Typical Characteristics (Continued)

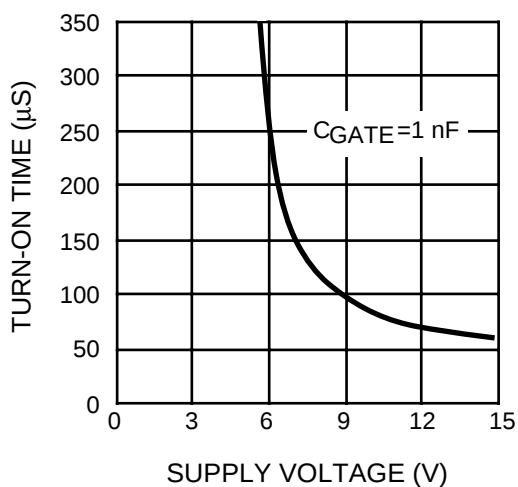
Supply Current



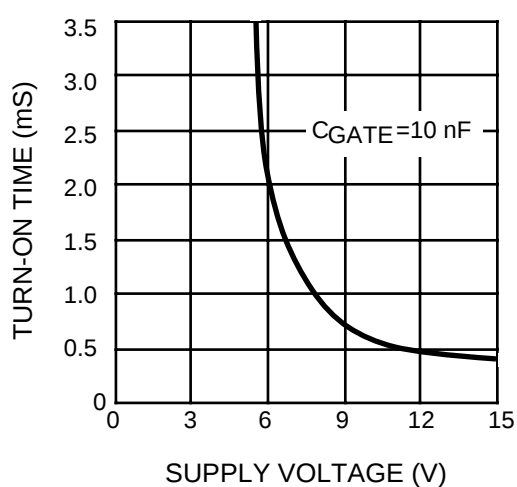
DC Gate Voltage above Supply



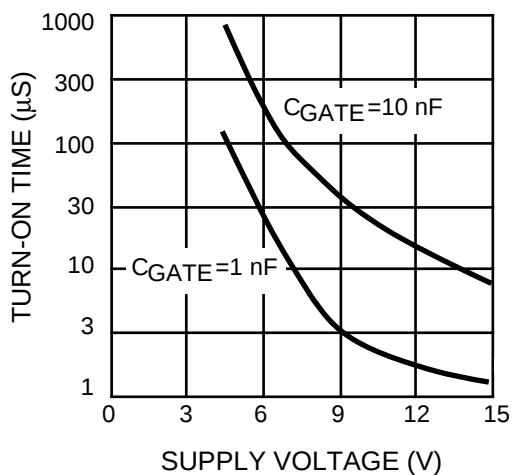
High-side Turn-on Time*



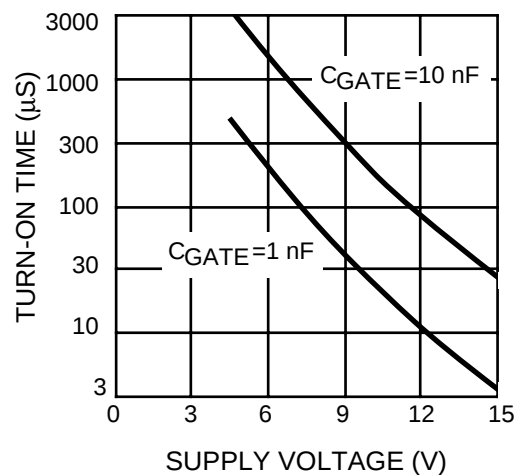
High-side Turn-on Time*



Low-side Turn-on Time for Gate = 5V



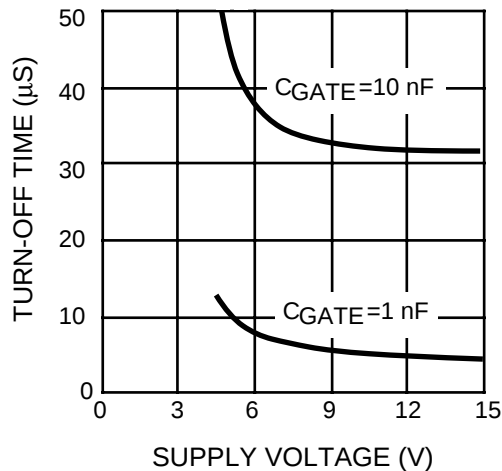
Low-side Turn-on Time for Gate = 10V



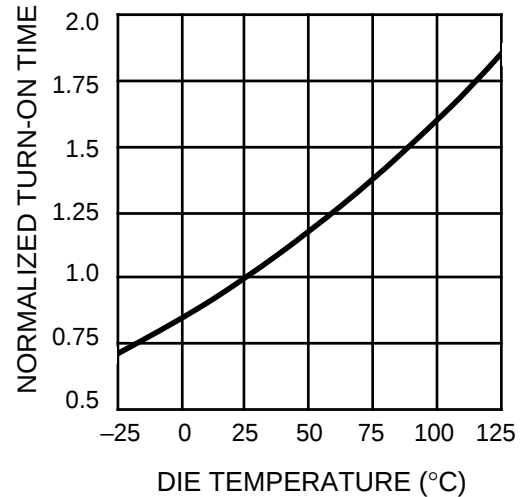
* Time for gate to reach $V^+ + 5V$ in test circuit with $V_S = V^+ - 5V$.

Typical Characteristics (Continued)

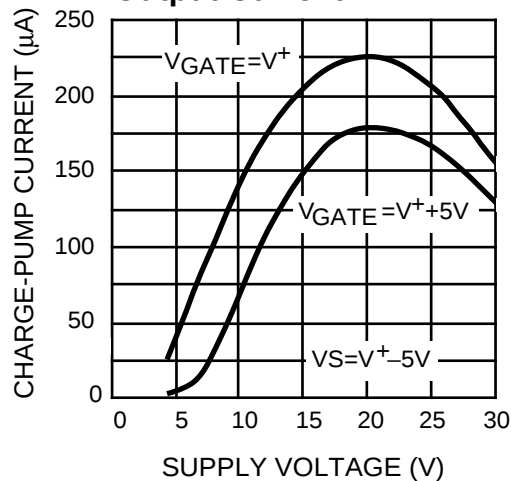
Turn-off Time



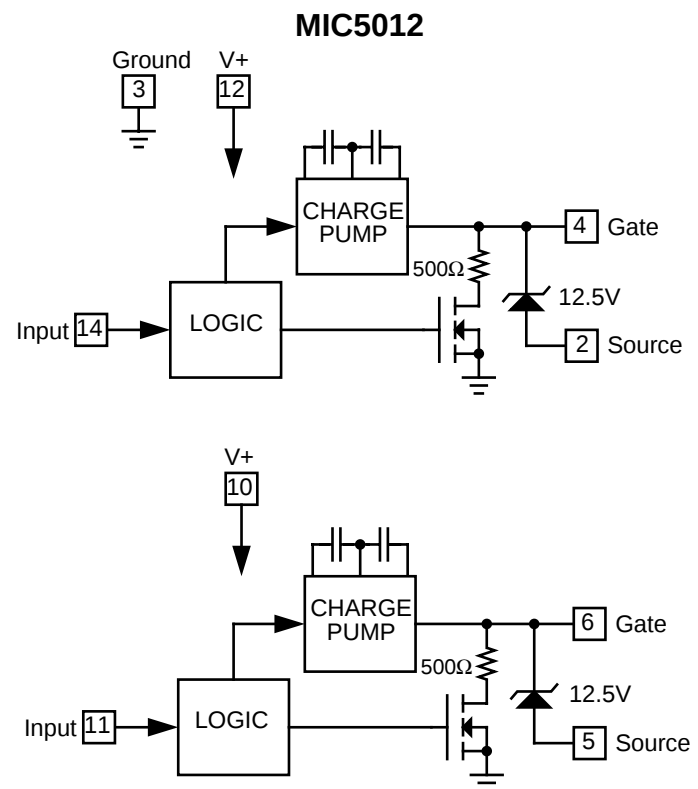
Turn-on Time



Charge Pump Output Current



Block Diagram



Applications Information

Functional Description (Refer to Block Diagram)

The MIC5012 consists of two independent drivers sharing a common ground. The functions are controlled via a logic block connected to the logic input. When the input is low, all functions are turned off for low standby current and the gate of the power MOSFET is also held low through 500Ω to an N-channel switch. When the input is taken above the turn-on threshold (3.5V typical), the N-channel switch turns off and the charge pump is turned on to charge the gate of the power FET.

The charge pump incorporates a 100kHz oscillator and on-chip pump capacitors capable of charging 1nF to 5V above supply in 60μs typical. The charge pump is capable of pumping the gate up to over twice the supply voltage. For this reason, a zener clamp (12.5V typical) is provided between the gate pin and source pin to prevent exceeding

the V_{GS} rating of the MOSFET at high supplies.

Since the supply pins are independent, the two drivers contained in the MIC5012 can be operated from separate supplies of different values (see Figure 6).

Construction Hints

High current pulse circuits demand equipment and assembly techniques that are more stringent than normal, low current lab practices. The following are the sources of

Applications Information (Continued)

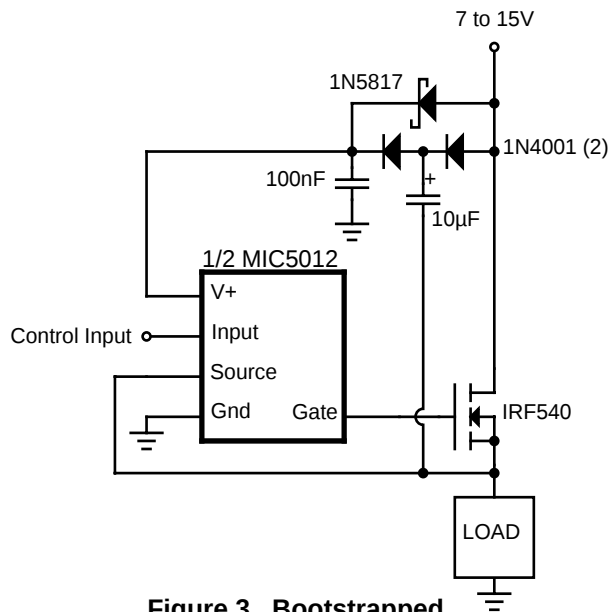


Figure 3. Bootstrapped High-Side Driver

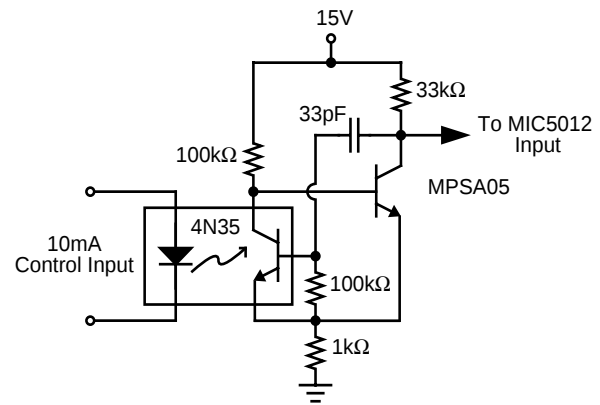


Figure 4. Improved Opto-Isolator Performance

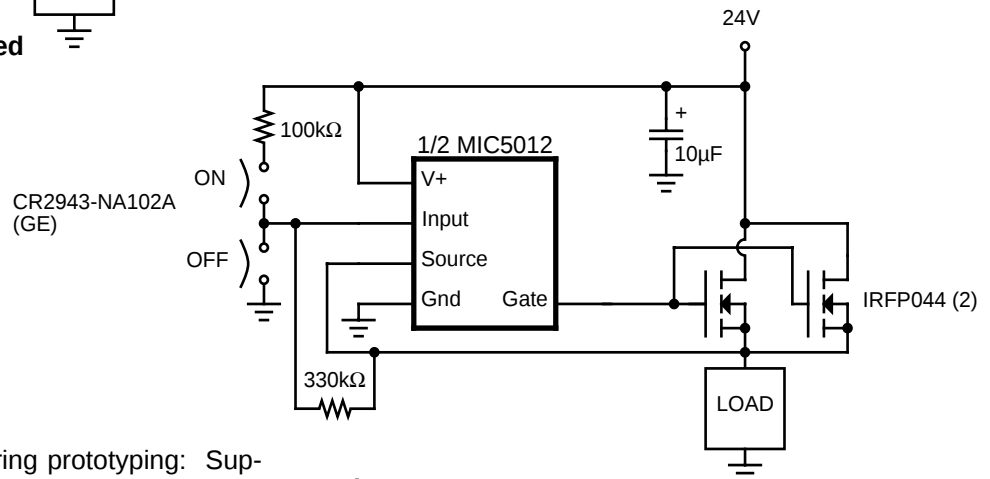


Figure 5. 50-Ampere Industrial Switch

pitfalls most often encountered during prototyping: Supplies: many bench power supplies have poor transient response. Circuits that are being pulse tested, or those that operate by pulse-width modulation will produce strange results when used with a supply that has poor ripple rejection, or a peaked transient response. Always monitor the power supply voltage that appears at the drain of a high-side driver (or the supply side of the load in a low-side driver) with an oscilloscope. It is not uncommon to find bench power supplies in the 1kW class that overshoot or undershoot by as much as 50% when pulse loaded. Not only will the load current and voltage measurements be affected, but it is possible to over-stress various components—especially electrolytic capacitors—with possibly catastrophic results. A 10µF supply bypass capacitor at the chip is recommended.

Residual Resistances: Resistances in circuit connections may also cause confusing results. For example, a circuit may employ a 50mΩ power MOSFET for low drop, but careless construction techniques could easily add 50 to 100mΩ resistance. Do not use a socket for the MOSFET. If the MOSFET is a TO-220 type package, make high-current drain connections to the tab. Wiring losses have a profound effect on high-current circuits. A floating millivoltmeter can identify connections that are contributing excess drop under load.

Circuit Topologies

The MIC5012 is suited for use with standard MOSFETs in high- or low-side driver applications. In addition, the MIC5012 works well in applications where, for faster switching times, the supply is bootstrapped from the MOSFET source output. Low voltage, high-side drivers (such as shown in Figure 1) are the slowest; their speed is reflected in the gate turn-on time specifications. The fastest drivers are the low-side and bootstrapped high-side types (Figures 2 and 4). Load current switching times are often much faster than the time to full gate enhancement, depending on the circuit type, the MOSFET, and the load. Turn-off times are essentially the same for all circuits (less than 10µs to $V_{GS} = 1V$). The choice of one topology over another is based on a combination of considerations including speed, voltage, and desired system characteristics.

High-Side Driver (Figure 1). The high-side topology works well down to $V^+ = 7V$ with standard MOSFETs. From 4.75 to 7V supply, a logic-level MOSFET can be substituted since the MIC5012 will not reach 10V gate enhancement (10V is the maximum rating for logic-compatible MOSFETs).

Applications Information (Continued)

High-side drivers implemented with MIC501X drivers are self-protected against inductive switching transients. During turn-off an inductive load will force the MOSFET source 5V or more below ground, while the MIC5012 holds the gate at ground potential. The MOSFET is forced into conduction, and it dissipates the energy stored in the load inductance. The MIC5012 source pin is designed to withstand this negative excursion without damage. External clamp diodes are unnecessary.

Low-Side Driver (Figure 2). A key advantage of the low-side topology is that the load supply is limited only by the MOSFET BV_{DSS} rating. Clamping may be required to protect the MOSFET drain terminal from inductive switching transients. The MIC5012 supply should be limited to 15V in low-side topologies; otherwise, a large current will be forced through the gate clamp zener. The switching speed to 10V enhancement is 300 μ s driving 1nF on a 5V supply. On a 15V supply the turn-on time is less than 2 μ s to 10V

Low-side drivers constructed with the MIC501X family are also fast; the MOSFET gate is driven to near supply immediately when commanded ON. Typical circuits achieve 10V enhancement in 10 μ s or less on a 12 to 15V supply.

Modifying Switching Times. Do not add external capacitors to the MOSFET gate. Add a resistor (1k Ω to 51k Ω) in series with the gate to slow down the switching time.

Bootstrapped High-Side Driver (Figure 3). The speed of a high-side driver can be increased to better than 10 μ s by bootstrapping the supply off of the MOSFET source. This topology can be used where the load is pulse-width modulated (100Hz to 20kHz), or where it is energized continu-

ously. The Schottky barrier diode prevents the MIC5012 supply pin from dropping more than 200mV below the drain supply, and it also improves turn-on time on supplies of less than 10V. Since the supply current in the "off" state is only a small leakage, the 100nF bypass capacitor tends to remain charged for several seconds after the MIC5012 is turned off. In a PWM application the chip supply is sustained at a higher potential than the system supply, which improves switching time.

Opto-Isolated Interface (Figure 4). Although the MIC5012 has no special input slew rate requirement, the lethargic transitions provided by an opto-isolator may cause oscillations on the rise and fall of the output. The circuit shown accelerates the input transitions from a 4N35 opto-isolator by adding hysteresis. Opto-isolators are used where the control circuitry cannot share a common ground with the MIC5012 and high-current power supply, or where the control circuitry is located remotely. This implementation is intrinsically safe; if the control line is severed the MIC5012 will turn OFF.

Industrial Switch (Figure 5). The most common manual control for industrial loads is a push button on/off switch. The "on" button is physically arranged in a recess so that in a panic situation the "off" button, which extends out from the control box, is more easily pressed. This circuit is compatible with control boxes such as the CR2943 series (GE). The circuit is configured so that if both switches close simultaneously, the "off" button has precedence.

This application also illustrates how two (or more) MOSFETs

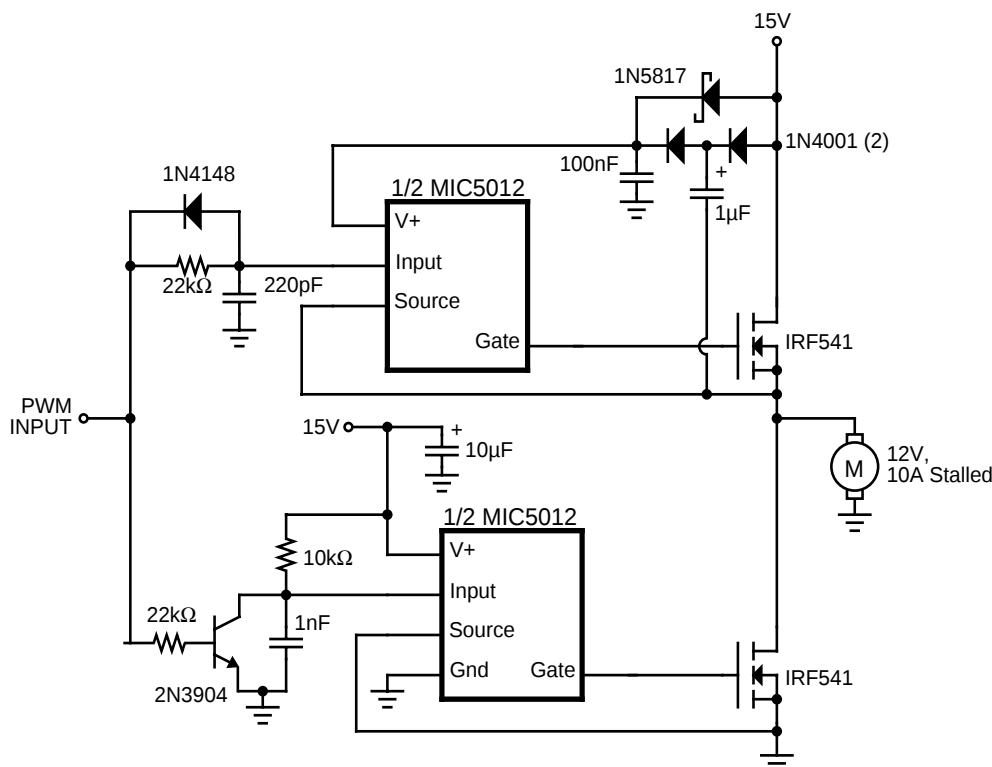


Figure 6. Half-Bridge Motor Driver

Applications Information (Continued)

can be paralleled. This reduces the switch drop, and distributes the switch dissipation into multiple packages.

Half-Bridge Motor Driver (Figure 6). Closed loop control of motor speed requires a half-bridge driver. This topology presents an extra challenge since the two output devices should not cross conduct (shoot-through) when switching. Cross conduction increases output device power dissipation. Speed is also important, since PWM control requires the outputs to switch in the 2 to 20kHz range.

The circuit of Figure 6 utilizes fast configurations for both the top- and bottom-side drivers. Delay networks at each input provide a 2 to 3 μ s dead time effectively eliminating cross conduction. Two of these circuits can be connected together to form an H-bridge for locked antiphase or sign/magnitude control.

Time-Delay Relay (Figure 7). The MIC5012 forms the basis of a simple time-delay relay. As shown, the delay commences when power is applied, but the 100k Ω /1N4148 could be independently driven from an external source such as a switch or another high-side driver to give a delay relative to some other event in the system. Hysteresis has been added to guarantee clean switching at turn-on.

Motor Driver with Stall Shutdown (Figure 8). Tachometer feedback can be used to shut down a motor driver circuit when a stall condition occurs. The control switch is a 3-way type; the "START" position is momentary and forces the driver ON. When released, the switch returns to the "RUN" position, and the tachometer's output is used to hold the MIC5012 input ON. If the motor slows down, the tach output is reduced, and the MIC5012 switches OFF. Resistor "R" sets the shutdown threshold.

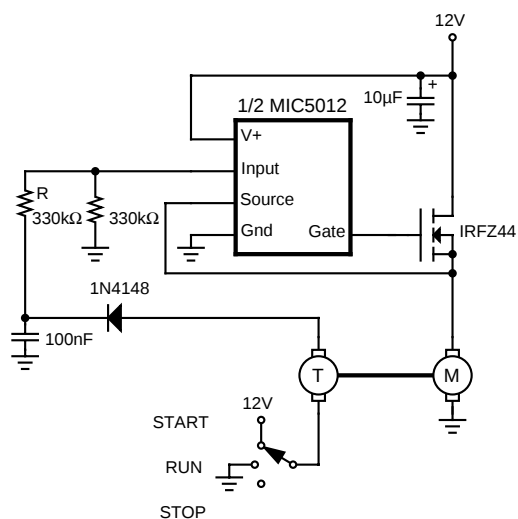


Figure 8. Motor Stall Shutdown

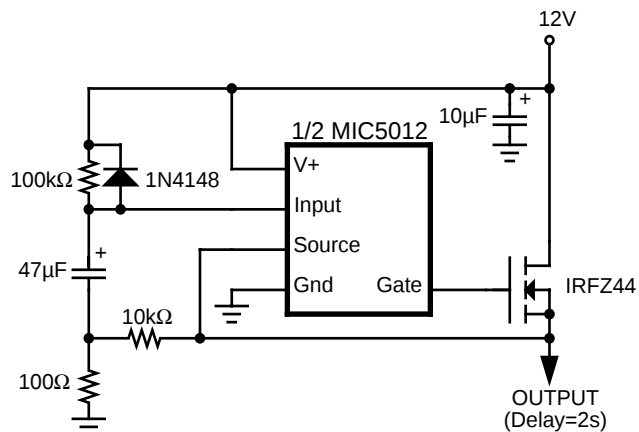


Figure 7. 30 Ampere Time-Delay Relay

Electronic Governor (Figure 9). The output of an ac tachometer can be used to form a PWM loop to maintain the speed of a motor. The tachometer output is rectified, partially filtered, and fed back to the input of the MIC5012. When the motor is stalled there is no tachometer output, and MIC5012 input is pulled high delivering full power to the motor. If the motor spins fast enough, the tachometer output is sufficient to pull the MIC5012 input low, shutting the output off. Since the rectified waveform is only partially filtered, the input oscillates around its threshold causing the MIC5012 to switch on and off at the frequency of the tachometer signal. A PWM action results since the average dc voltage at the input decreases as the motor spins faster. The 1k Ω potentiometer is used to set the running speed of the motor. Loop gain (and speed regulation) is increased by increasing the value of the 100nF filter capacitor.

The performance of such a loop is imprecise, but stable and inexpensive. A more elaborate loop would consist of a PWM controller and a half-bridge.

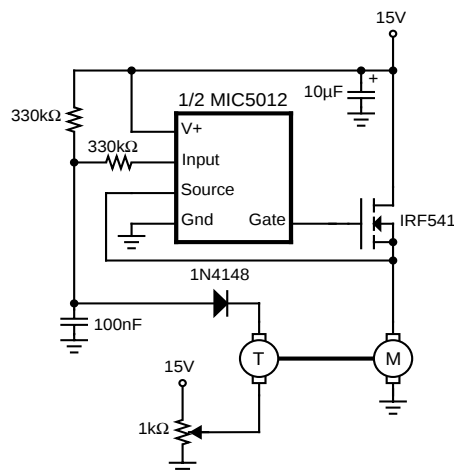


Figure 9. Electronic Governor

Applications Information (Continued)

Gate Control Circuit

When applying the MIC5012, it is helpful to understand the operation of the gate control circuitry (see Figure 12). The gate circuitry can be divided into two sections: 1) charge pump (oscillator, Q1-Q5, and the capacitors) and 2) gate turn-off switch (Q6).

When the MIC5012 is in the OFF state, the oscillator is turned off, thereby disabling the charge pump. Q5 is also turned off, and Q6 is turned on. Q6 holds the gate pin (G) at ground potential which effectively turns the external MOSFET off.

Q6 is turned off when the MIC5012 is commanded on, and Q5 pulls the gate up to supply (through 2 diodes). Next, the charge pump begins supplying current to the gate. The gate accepts charge until the gate-source voltage reaches 12.5V and is clamped by the zener diode.

A 2-output, three-phase clock switches Q1-Q4, providing a quasi-tripling action. During the initial phase Q4 and Q2 are ON. C1 is discharged, and C2 is charged to supply through

Q5. For the second phase Q4 turns off and Q3 turns on, pushing C2 above supply (charge is dumped into the gate). Q3 also charges C1. On the third phase Q2 turns off and Q1 turns on, pushing the common point of the two capacitors above supply. Some of the charge in C1 makes its way to the gate. The sequence is repeated by turning Q2 and Q4 back on, and Q1 and Q3 off.

In a low-side application operating on a 12 to 15V supply, the MOSFET is fully enhanced by the action of Q5 alone. On supplies of more than approximately 14V, current flows directly from Q5 through the zener diode to ground. To prevent excessive current flow, the MIC5012 supply should be limited to 15V in low-side applications.

The action of Q5 makes the MIC5012 operate quickly in low-side applications. In high-side applications Q5 precharges the MOSFET gate to supply, leaving the charge pump to carry the gate up to full enhancement 10V above supply. Bootstrapped high-side drivers are as fast as low-side drivers since the chip supply is boosted well above the drain at turn-on.

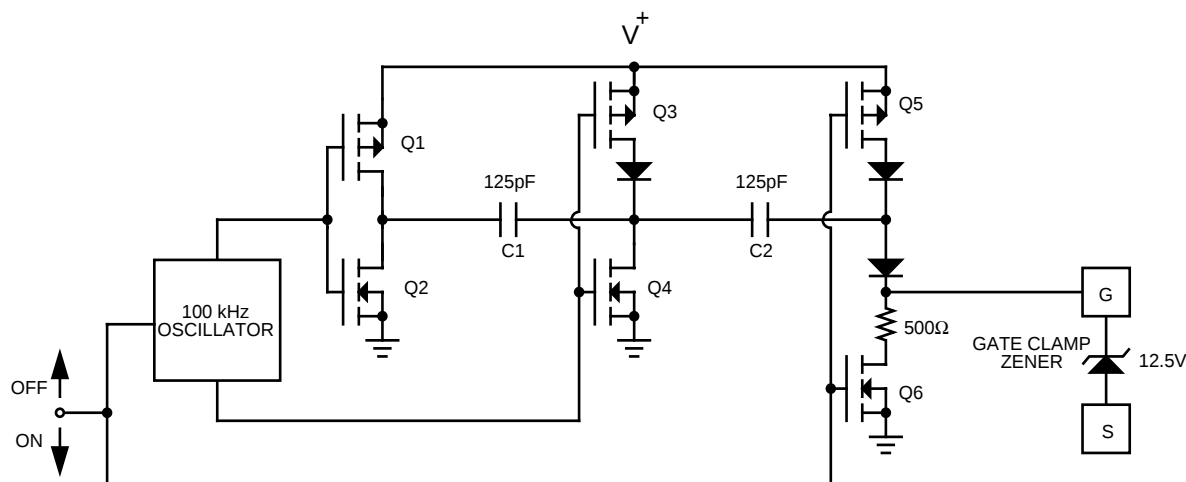


Figure 10. Gate Control Circuit Detail