# 74HC175; 74HCT175

Quad D-type flip-flop with reset; positive-edge trigger

Rev. 7 — 14 March 2024 Product data sheet

### 1. General description

The 74HC175; 74HCT175 is a quad positive-edge triggered D-type flip-flop with individual data inputs (Dn) and complementary outputs (Qn and  $\overline{\text{Qn}}$ ). The common clock (CP) and master reset ( $\overline{\text{MR}}$ ) inputs load and reset all flip-flops simultaneously. The D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. A LOW on  $\overline{\text{MR}}$  causes the flip-flops and outputs to be reset LOW. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

### 2. Features and benefits

- Input levels:
  - For 74HC175: CMOS level
  - For 74HCT175: TTL level
- Four edge-triggered D-type flip-flops
- · Asynchronous master reset
- · Complies with JEDEC standard no. 7A
- · ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C.

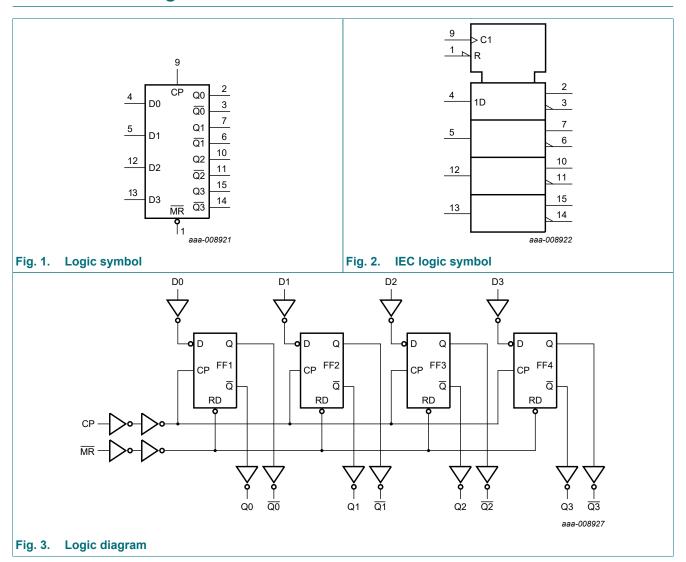
### 3. Ordering information

### Table 1. Ordering information

Type number	Type number Package										
	Temperature range	Name	Description	Version							
74HC175D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1							
74HCT175D			body width 3.9 mm								
74HC175PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads;	SOT403-1							
74HCT175PW			body width 4.4 mm								

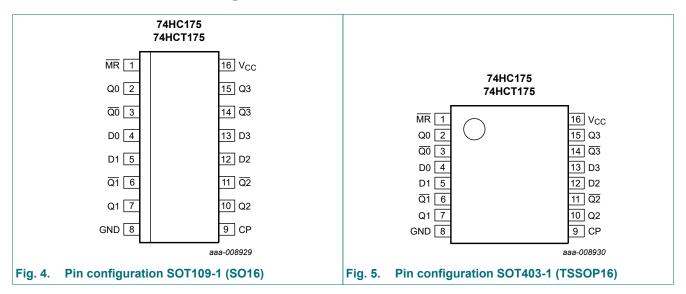


# 4. Functional diagram



### 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
MR	1	asynchronous master reset input (active LOW)
Q0 to Q3	2, 7, 10, 15	flip-flop output
Q0 to Q3	3, 6, 11, 14	complementary flip-flop output
D0 to D3	4, 5, 12, 13	data input
GND	8	ground (0 V)
СР	9	clock input (LOW-to-HIGH edge-triggered)
V <sub>CC</sub>	16	positive supply voltage

## 6. Functional description

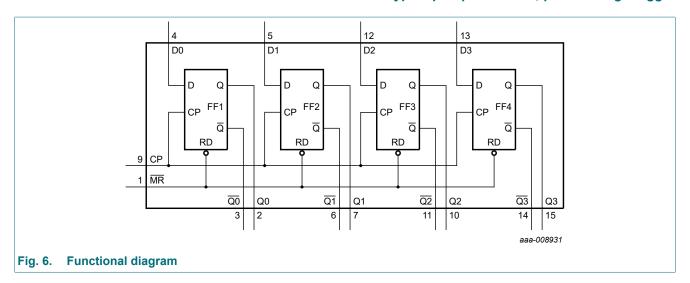
#### Table 3. Function table

 $H = HIGH \ voltage \ level; \ h = HIGH \ voltage \ level \ one \ set-up \ time \ prior \ to \ the \ LOW-to-HIGH \ clock \ transition;$ 

L = LOW voltage level; I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

 $X = don't \ care; \uparrow = LOW-to-HIGH \ clock \ transition.$ 

Operating modes	Inputs		Outputs		
	MR CP Dn		Qn	<u>Qn</u>	
reset (clear)	L	Х	Х	L	Н
load "1"	Н	1	h	Н	L
load "0"	Н	1	I	L	Н



### 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	-	±20	mA
I <sub>OK</sub>	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$	-	±20	mA
Io	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb}$ = -40 °C to +125 °C [1	] -	500	mW

<sup>[1]</sup> For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C. For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

### 8. Recommended operating conditions

### **Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC175			74HCT175			Unit
			Min	Тур	Max	Min	Тур	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

### 9. Static characteristics

#### **Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit	
			Min	Тур	Max	Min	Max	Min	Max		
74HC17	5						1	1	'		
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V	
	input voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V	
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V	
V <sub>IL</sub>	LOW-level	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V	
	input voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V	
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V	
V <sub>OH</sub>	HIGH-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>									
	output voltage	I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V	
		$I_{O}$ = -20 $\mu$ A; $V_{CC}$ = 4.5 $V$		4.5	-	4.4	-	4.4	-	V	
		$I_{O}$ = -20 $\mu$ A; $V_{CC}$ = 6.0 $V$		5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V	
		$I_O = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V	
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$									
	output voltage	I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V	
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V	
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V	
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V	
		$I_O = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V	
I <sub>I</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ	
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μΑ	
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF	

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Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HCT1	75						<b>'</b>	1		
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage V <sub>CC</sub> = 4.5 V to 5.5 V		-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
- OL  -	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ
Icc	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
ΔI <sub>CC</sub>	additional supply current	per input pin; $V_I = V_{CC}$ - 2.1 V; other inputs at $V_{CC}$ or GND; $V_{CC}$ = 4.5 V to 5.5 V								
		Dn input	-	40	144	-	180	-	196	μΑ
		CP input	-	60	216	-	270	-	294	μΑ
		MR input	-	100	360	-	450	-	490	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

# 10. Dynamic characteristics

#### **Table 7. Dynamic characteristics**

GND (ground = 0 V);  $C_L$  = 50 pF unless otherwise specified; for test circuit, see Fig. 10

Symbol	Parameter	Conditions		25 °C		-40 °C to	+85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC17	5									
	propagation	CP to Qn, Qn; see Fig. 7 [1]								
	delay	V <sub>CC</sub> = 2.0 V	-	55	175	-	220	-	265	ns
		V <sub>CC</sub> = 4.5 V	-	20	35	-	44	-	53	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	17	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	16	30	-	37	-	45	ns
t <sub>PHL</sub>	HIGH	MR to Qn, Qn; see Fig. 8								
	to LOW propagation	V <sub>CC</sub> = 2.0 V	-	50	150	-	190	-	225	ns
	delay	V <sub>CC</sub> = 4.5 V	-	18	30	-	38	-	45	ns
	·	V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	15	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	14	26	-	33	-	38	ns

Symbol	Parameter	Conditions		25 °C		-40 °C to	+85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
t <sub>t</sub>	transition	Qn output; see Fig. 7 [2]								
	time	V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns
t <sub>W</sub>	pulse width	CP input HIGH or LOW; see Fig. 7								
		V <sub>CC</sub> = 2.0 V	80	22	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	8	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	6	-	17	-	20	-	ns
		MR input LOW; see Fig. 8								
		V <sub>CC</sub> = 2.0 V	80	19	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	7	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	6	-	17	-	20	-	ns
t <sub>rec</sub>	recovery	MR to CP; see Fig. 8								
100	time	V <sub>CC</sub> = 2.0 V	5	-33	-	5	-	5	-	ns
		V <sub>CC</sub> = 4.5 V	5	-12	-	5	-	5	-	ns
		V <sub>CC</sub> = 6.0 V	5	-10	-	5	-	5	-	ns
t <sub>su</sub>	set-up time	Dn to CP; see Fig. 9								
		V <sub>CC</sub> = 2.0 V	80	3	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	1	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	1	-	17	-	20	-	ns
t <sub>h</sub>	hold time	Dn to CP; see Fig. 9								
		V <sub>CC</sub> = 2.0 V	25	2	-	30	-	40	-	ns
		V <sub>CC</sub> = 4.5 V	5	0	-	6	-	8	-	ns
		V <sub>CC</sub> = 6.0 V	4	0	-	5	-	7	-	ns
f <sub>max</sub>	maximum	CP input; see Fig. 7								
	frequency	V <sub>CC</sub> = 2.0 V	6	25	-	4.8	-	4	-	MHz
		V <sub>CC</sub> = 4.5 V	30	75	-	24	-	20	-	MHz
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	83	-	-	-	-	-	MHz
		V <sub>CC</sub> = 6.0 V	35	89	-	28	-	24	-	MHz
C <sub>PD</sub>	power dissipation capacitance	per package; $V_I = GND$ to $V_{CC}$ [3]	-	32	-	-	-	-	-	pF

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Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HCT1	75									
t <sub>pd</sub>	propagation	CP to Qn, Qn; see Fig. 7 [1]								
	delay	V <sub>CC</sub> = 4.5 V	-	19	33	-	41	-	50	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	16	-	-	-	-	-	ns
t <sub>PHL</sub>	HIGH	MR to Qn; see Fig. 8								
	to LOW propagation	V <sub>CC</sub> = 4.5 V	-	22	38	-	48	-	57	ns
	delay	V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	19	-	-	-	-	-	ns
	·	MR to Qn; see Fig. 8								
		V <sub>CC</sub> = 4.5 V	-	19	35	-	44	-	53	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	16	-	-	-	-	-	ns
t <sub>t</sub>	transition	Qn output; see Fig. 7 [2]								
	time	V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
t <sub>W</sub>	pulse width	CP input HIGH or LOW; see Fig. 7								
		V <sub>CC</sub> = 4.5 V	20	12	-	25	-	30	-	ns
		MR input LOW; see Fig. 8								
		V <sub>CC</sub> = 4.5 V	20	11	-	25	-	30	-	ns
t <sub>rec</sub>	recovery	MR to CP; see Fig. 8								
	time	V <sub>CC</sub> = 4.5 V	5	-10	-	5	-	5	-	ns
t <sub>su</sub>	set-up time	Dn to CP; see Fig. 9								
		V <sub>CC</sub> = 4.5 V	16	5	-	20	-	24	-	ns
t <sub>h</sub>	hold time	Dn to CP; see Fig. 9								
		V <sub>CC</sub> = 4.5 V	5	0	-	5	-	5	-	ns
f <sub>max</sub>	maximum	CP input; see Fig. 7								
	frequency	V <sub>CC</sub> = 4.5 V	25	49	-	20	-	17	-	MHz
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	54	-	-	-	-	-	MHz
C <sub>PD</sub>	power dissipation capacitance	per package; [3] V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V	-	34	-	-	-	-	-	pF

t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.
 t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.
 C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).
 P<sub>D</sub> = C<sub>PD</sub> x V<sub>CC</sub><sup>2</sup> x f<sub>i</sub> + Σ (C<sub>L</sub> x V<sub>CC</sub><sup>2</sup> x f<sub>o</sub>) where:
 f<sub>i</sub> = input frequency in MHz;

 $f_o$  = output frequency in MHz;

 $\Sigma$  (C<sub>L</sub> x V<sub>CC</sub>  $^2$  x f<sub>o</sub>) = sum of outputs;

C<sub>L</sub> = output load capacitance in pF;

 $V_{CC}$  = supply voltage in V.

#### 10.1. Waveforms and test circuit

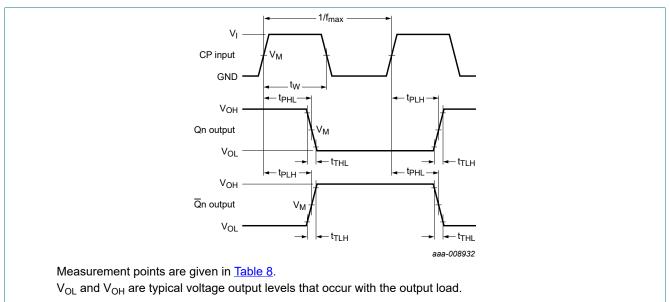


Fig. 7. Input to output propagation delay, output transition time, clock input pulse width and maximum frequency

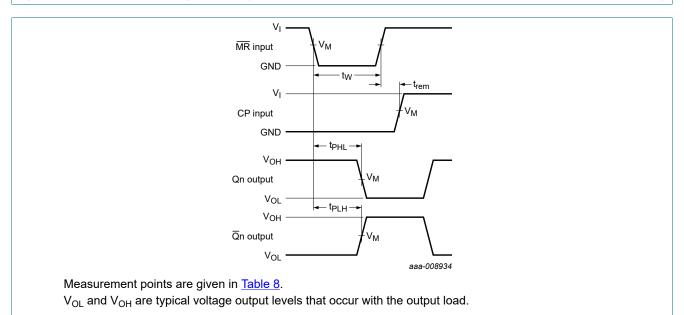
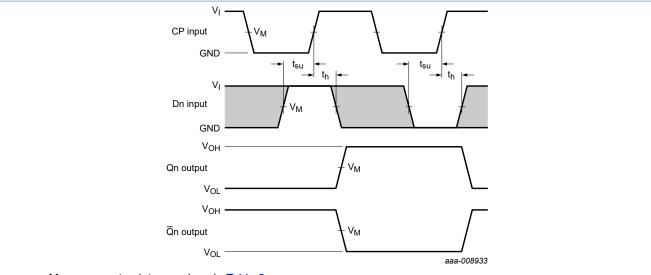


Fig. 8. Master reset to output propagation delays, master reset pulse width and master reset to clock recovery time



Measurement points are given in <u>Table 8</u>.

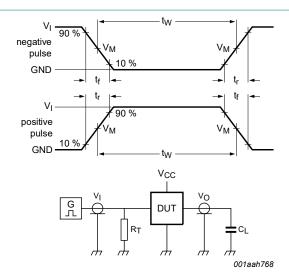
 $\ensuremath{V_{\text{OL}}}$  and  $\ensuremath{V_{\text{OH}}}$  are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 9. Data set-up and hold times for data input

**Table 8. Measurement points** 

Туре	Input	Output	
	v <sub>M</sub>		V <sub>M</sub>
74HC175	V <sub>CC</sub>	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>
74HCT175	3 V	1.3 V	1.3 V



Test data is given in Table 9.

Definitions for test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

 $C_L$  = Load capacitance including jig and probe capacitance.

 $R_L$  = Load resistance.

Fig. 10. Test circuit for measuring switching times

Table 9. Test data

Туре	Input		Load	Test	
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	
74HC175	V <sub>CC</sub>	6 ns	15 pF, 50 pF	1 kΩ	t <sub>PLH</sub> , t <sub>PHL</sub>
74HCT175	3 V	6 ns	15 pF, 50 pF	1 kΩ	t <sub>PLH</sub> , t <sub>PHL</sub>

### 11. Package outline

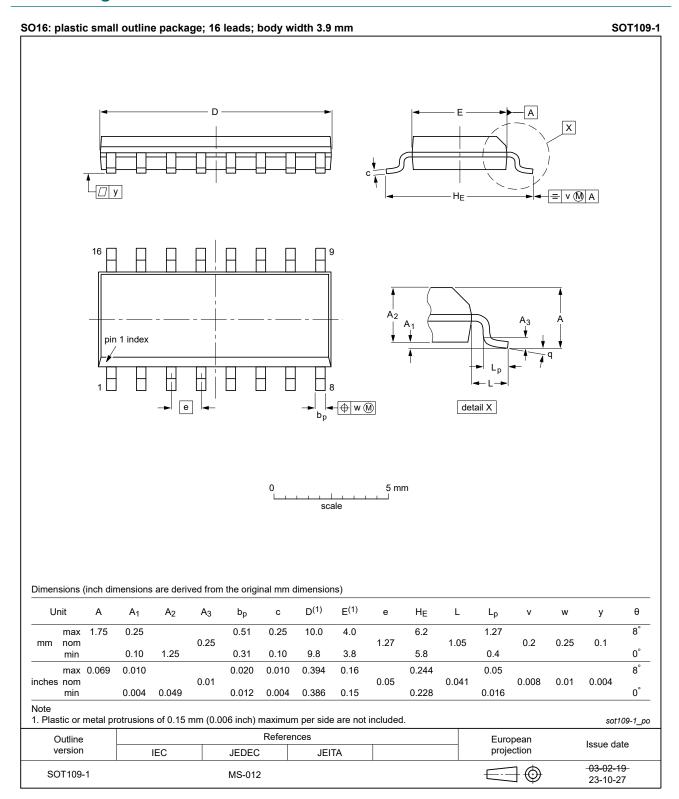


Fig. 11. Package outline SOT109-1 (SO16)

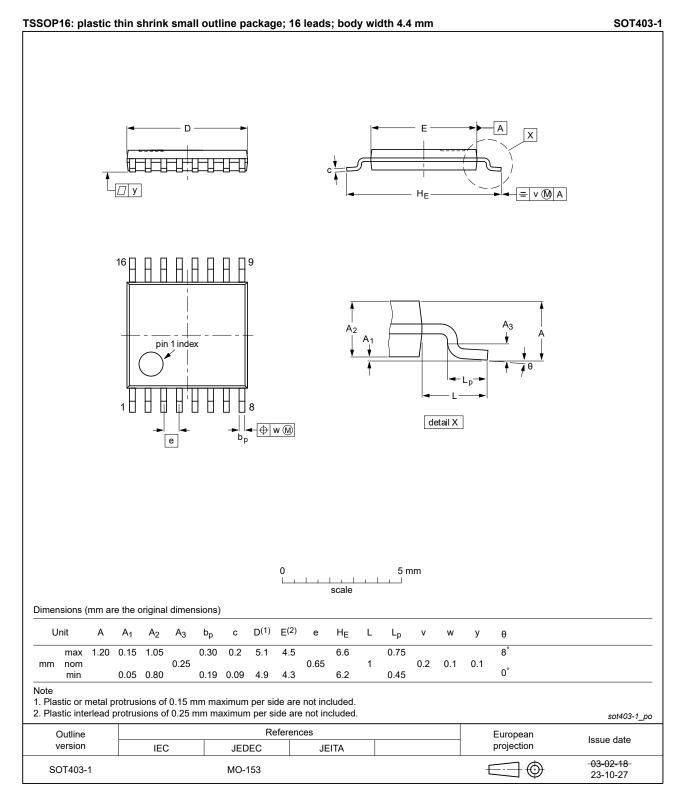


Fig. 12. Package outline SOT403-1 (TSSOP16)

### 12. Abbreviations

#### **Table 10. Abbreviations**

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

# 13. Revision history

#### **Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC_HCT175 v.7	20240314	Product data sheet	-	74HC_HCT175 v.6	
Modifications:	<ul> <li>Fig. 11, Fig. 12: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.</li> <li>Section 2: ESD specification updated according to the latest JEDEC standard.</li> </ul>				
74HC_HCT175 v.6	20210204	Product data sheet	-	74HC_HCT175 v.5	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74HC175DB and 74HCT175DB (SOT338-1 / SSOP16) removed.</li> <li>Section 7: Derating values for P<sub>tot</sub> total power dissipation updated.</li> </ul>				
74HC_HCT175 v.5	20160129	Product data sheet	-	74HC_HCT175 v.4	
Modifications:	Type numbers 74HC175N and 74HCT175N (SOT38-4) removed.				
74HC_HCT175 v.4	20140408	Product data sheet	-	74HC_HCT175 v.3	
Modifications:	General description corrected (errata).				
74HC_HCT175 v.3	20140331	Product data sheet	-	74HC_HCT175_CNV_2	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>				
74HC HCT175 CNV 2	19980708	Product specification	-	-	

### 14. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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#### Quad D-type flip-flop with reset; positive-edge trigger

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For more information, please visit: http://www.nexperia.com For sales office addresses, please send an email to: salesaddresses@nexperia.com Date of release: 14 March 2024

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