



UTRON

Rev 1.7

UT61L1024

128K X 8 BIT HIGH SPEED CMOS SRAM

## REVISION HISTORY

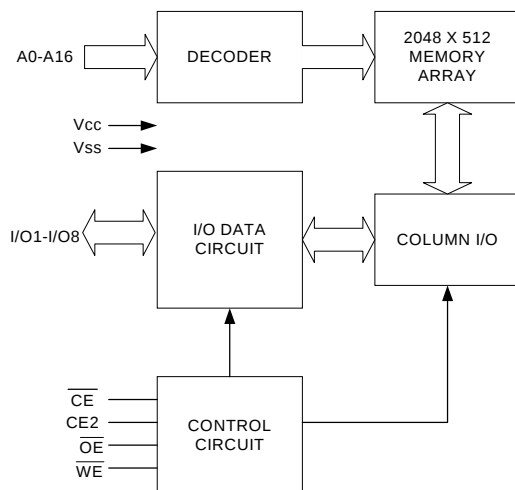
| REVISION | DESCRIPTION                                                                                                                                                           | Released Date |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| Rev. 1.0 | Original.                                                                                                                                                             | Apr. 05 2000  |
| Rev. 1.1 | Add TSOP-I Package                                                                                                                                                    | Aug. 29.2000  |
| Rev. 1.2 | Modify the format of power consumption                                                                                                                                | Sep. 01.2000  |
| Rev. 1.3 | 1. $V_{OH}$ : 2.4 -> 2.2<br>2. Input Rise & Fall times : 5->3ns<br>3. The symbols CE1# ,OE# & WE# are revised as $\overline{CE1}$ , $\overline{OE}$ & $\overline{WE}$ | Jun. 18,2001  |
| Rev.1.4  | Add SOP Package.                                                                                                                                                      | Jul. 6,2001   |
| Rev. 1.5 | 1. Revised TSOP- /STSOP pin configuration typing error :<br>Pin 5= $\overline{WE}$ 、 pin 6=CE2<br>2. Revised package outline dimension                                | Apr 16,2002   |
| Rev. 1.6 | 1. Revised Vcc:<br>Rev. 1.5 : Vcc=3.1V~3.6V<br>Rev. 1.6 : Vcc=3.0V~3.6V<br>2. Add data retention characteristics and waveforms<br>3. Revised function block diagram   | May 8,2002    |
| Rev. 1.7 | 1. Add order information for lead free product<br>2. Revised timing read/write waveform<br>3. Add $*V_{IL}=-3.0V$ for pulse width less than 10ns into DC table        | May 22,2003   |



## FEATURES

- Fast access time : 12/15ns (max.)
- Low power operating : 60mA (typ.)
- Single 3.0V~3.6V power supply
- All TTL compatible inputs and outputs
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)
- Package : 32-pin 300 mil skinny PDIP  
32-pin 300 mil SOJ  
32-pin 450mil SOP  
32-pin 8mm x 20mm TSOP-1  
32-pin 8mm x 13.4mm STSOP

## FUNCTIONAL BLOCK DIAGRAM



## PIN DESCRIPTION

| SYMBOL                | DESCRIPTION            |
|-----------------------|------------------------|
| A0 - A16              | Address Inputs         |
| I/O1 - I/O8           | Data Inputs/Outputs    |
| $\overline{CE}$ , CE2 | Chip enable 1,2 Inputs |
| $\overline{WE}$       | Write Enable Input     |
| $\overline{OE}$       | Output Enable Input    |
| V <sub>CC</sub>       | Power Supply           |
| V <sub>SS</sub>       | Ground                 |
| NC                    | No Connection          |

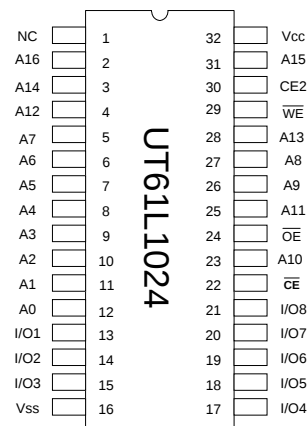
## GENERAL DESCRIPTION

The UT61L1024 is a 1,048,576-bit high-speed CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

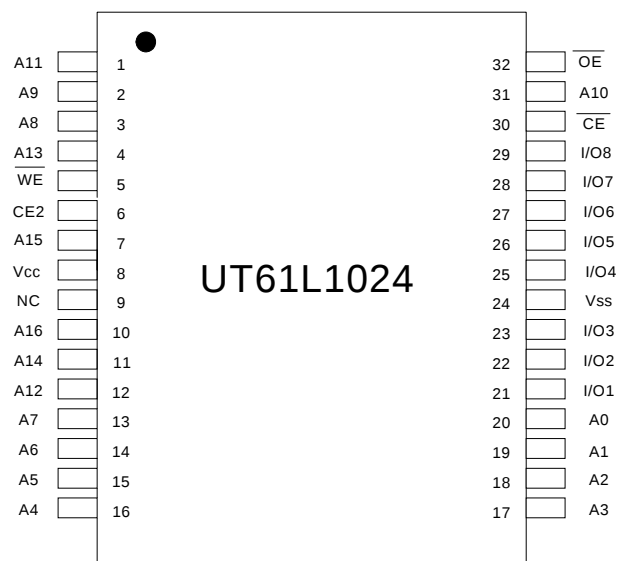
The UT61L1024 is designed for high-speed system applications. It is particularly suited for use in high-density high-speed system applications.

The UT61L1024 operates from a single 3.3V power supply and all inputs and outputs are fully TTL compatible.

## PIN CONFIGURATION



PDIP / SOJ/SOP



TSOP-I/STSOP

**ABSOLUTE MAXIMUM RATINGS\***

| PARAMETER                                        | SYMBOL              | RATING      | UNIT |
|--------------------------------------------------|---------------------|-------------|------|
| Terminal Voltage with Respect to V <sub>SS</sub> | V <sub>TERM</sub>   | -0.5 to 4.6 | V    |
| Operating Temperature                            | T <sub>A</sub>      | 0 to 70     |      |
| Storage Temperature                              | T <sub>STG</sub>    | -65 to 150  |      |
| Power Dissipation                                | P <sub>D</sub>      | 1           | W    |
| DC Output Current                                | I <sub>OUT</sub>    | 50          | mA   |
| Soldering Temperature (under 10 sec)             | T <sub>solder</sub> | 260         |      |

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

| MODE           | $\overline{CE}$ | CE2 | $\overline{OE}$ | $\overline{WE}$ | I/O OPERATION    | SUPPLY CURRENT                     |
|----------------|-----------------|-----|-----------------|-----------------|------------------|------------------------------------|
| Standby        | H               | X   | X               | X               | High - Z         | I <sub>SB</sub> , I <sub>SB1</sub> |
| Standby        | X               | L   | X               | X               | High - Z         | I <sub>SB</sub> , I <sub>SB1</sub> |
| Output Disable | L               | H   | H               | H               | High - Z         | I <sub>CC</sub>                    |
| Read           | L               | H   | L               | H               | D <sub>OUT</sub> | I <sub>CC</sub>                    |
| Write          | L               | H   | X               | L               | D <sub>IN</sub>  | I <sub>CC</sub>                    |

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> = 3.0V 3.6V, T<sub>A</sub> = 0 to 70 )

| PARAMETER                      | SYMBOL           | TEST CONDITION                                                                                                                                                   | MIN.         | MAX.                 | UNIT |
|--------------------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|----------------------|------|
| Power Voltage                  | V <sub>CC</sub>  |                                                                                                                                                                  | 3.0          | 3.6                  | V    |
| Input High Voltage             | V <sub>IH</sub>  |                                                                                                                                                                  | 2.0          | V <sub>CC</sub> +0.5 | V    |
| Input Low Voltage              | V <sub>IL</sub>  |                                                                                                                                                                  | - 0.5        | 0.6                  | V    |
| Input Leakage Current          | I <sub>LI</sub>  | V <sub>SS</sub> V <sub>IN</sub> V <sub>CC</sub>                                                                                                                  | - 1          | 1                    | μA   |
| Output Leakage Current         | I <sub>LO</sub>  | V <sub>SS</sub> V <sub>I/O</sub> V <sub>CC</sub><br>$\overline{CE} = V_{IH}$ or CE2 = V <sub>IL</sub><br>or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ | - 1          | 1                    | μA   |
| Output High Voltage            | V <sub>OH</sub>  | I <sub>OH</sub> = - 4mA                                                                                                                                          | 2.2          | -                    | V    |
| Output Low Voltage             | V <sub>OL</sub>  | I <sub>OL</sub> = 8mA                                                                                                                                            | -            | 0.4                  | V    |
| Operating Power Supply Current | I <sub>CC</sub>  | Cycle time=Min, I <sub>I/O</sub> = 0mA<br>$\overline{CE} = V_{IL}$ , CE2 = V <sub>IH</sub>                                                                       | - 12<br>- 15 | 100<br>90            | mA   |
| Standby Power Supply Current   | I <sub>SB</sub>  | $\overline{CE} = V_{IH}$ or CE2 = V <sub>IL</sub>                                                                                                                | -            | 20                   | mA   |
|                                | I <sub>SB1</sub> | $\overline{CE} = V_{CC}-0.2V$ ;or CE2 = 0.2V                                                                                                                     | -            | 3                    | mA   |

Notes:

1. Overshoot : V<sub>CC</sub>+3.0v for pulse width less than 8ns.
2. Undershoot : V<sub>SS</sub>-3.0v for pulse width less than 8ns.
3. Overshoot and Undershoot are sampled, not 100% tested.



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## CAPACITANCE ( $T_A=25^\circ\text{C}$ , $f=1.0\text{MHz}$ )

| PARAMETER                | SYMBOL    | MIN. | MAX. | UNIT |
|--------------------------|-----------|------|------|------|
| Input Capacitance        | $C_{IN}$  | -    | 8    | pF   |
| Input/Output Capacitance | $C_{I/O}$ | -    | 10   | pF   |

Note : These parameters are guaranteed by device characterization, but not production tested.

## AC TEST CONDITIONS

|                                          |                                                            |
|------------------------------------------|------------------------------------------------------------|
| Input Pulse Levels                       | 0V to 3.0V                                                 |
| Input Rise and Fall Times                | 3ns                                                        |
| Input and Output Timing Reference Levels | 1.5V                                                       |
| Output Load                              | $C_L=30\text{pF}$ , $I_{OH}/I_{OL}=-4\text{mA}/8\text{mA}$ |

## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 3.0\text{V}$ 3.6V, $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ )

### (1) READ CYCLE

| PARAMETER                          | SYMBOL                    | UT61L1024-12 |      | UT61L1024-15 |      | UNIT |
|------------------------------------|---------------------------|--------------|------|--------------|------|------|
|                                    |                           | MIN.         | MAX. | MIN.         | MAX. |      |
| Read Cycle Time                    | $t_{RC}$                  | 12           | -    | 15           | -    | ns   |
| Address Access Time                | $t_{AA}$                  | -            | 12   | -            | 15   | ns   |
| Chip Enable Access Time            | $t_{ACE1}$ , $t_{ACE1}$   | -            | 12   | -            | 15   | ns   |
| Output Enable Access Time          | $t_{OE}$                  | -            | 6    | -            | 7    | ns   |
| Chip Enable to Output in Low Z     | $t_{CLZ1*}$ , $t_{CLZ2*}$ | 3            | -    | 4            | -    | ns   |
| Output Enable to Output in Low Z   | $t_{OLZ*}$                | 0            | -    | 0            | -    | ns   |
| Chip Disable to Output in High Z   | $t_{CHZ1*}$ , $t_{CHZ2*}$ | -            | 6    | -            | 7    | ns   |
| Output Disable to Output in High Z | $t_{OHZ*}$                | -            | 6    | -            | 7    | ns   |
| Output Hold from Address Change    | $t_{OH}$                  | 3            | -    | 3            | -    | ns   |

### (2) WRITE CYCLE

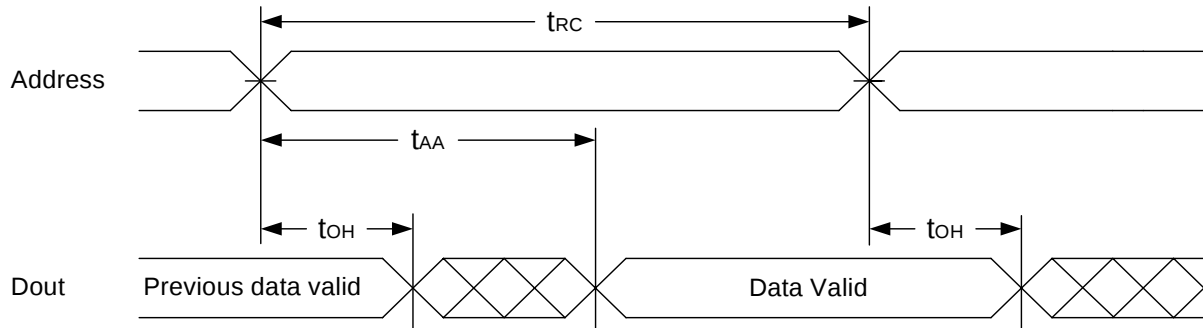
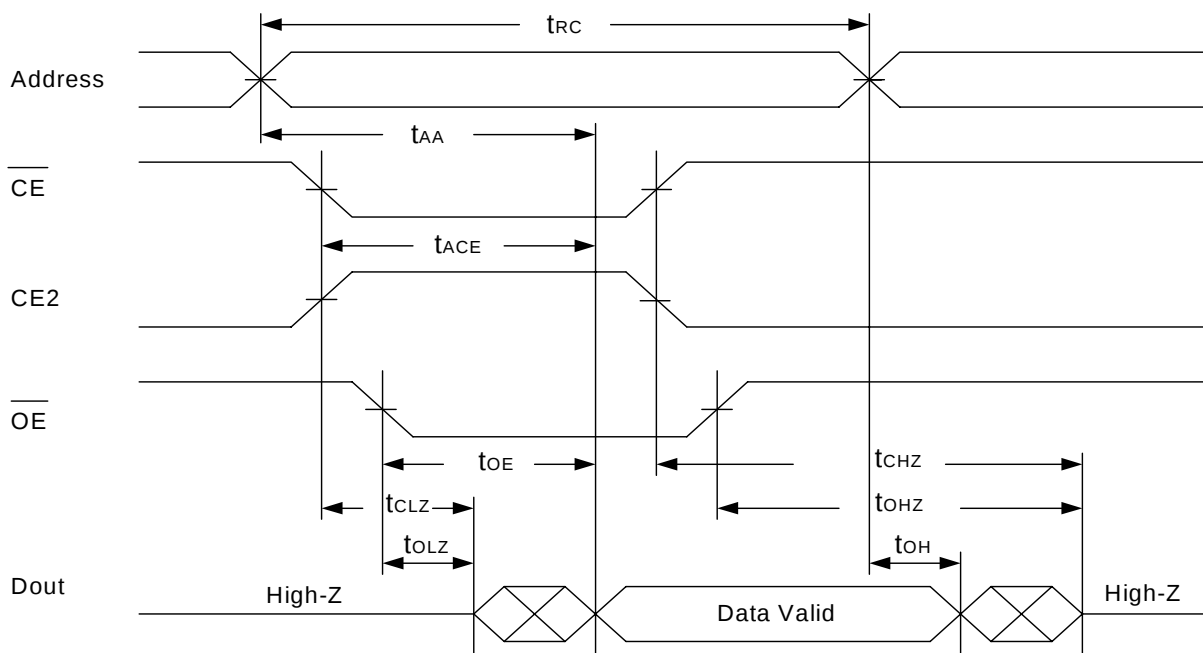
| PARAMETER                        | SYMBOL                | UT61L1024-12 |      | UT61L1024-15 |      | UNIT |
|----------------------------------|-----------------------|--------------|------|--------------|------|------|
|                                  |                       | MIN.         | MAX. | MIN.         | MAX. |      |
| Write Cycle Time                 | $t_{WC}$              | 12           | -    | 15           | -    | ns   |
| Address Valid to End of Write    | $t_{AW}$              | 10           | -    | 12           | -    | ns   |
| Chip Enable to End of Write      | $t_{CW1}$ , $t_{CW2}$ | 10           | -    | 12           | -    | ns   |
| Address Set-up Time              | $t_{AS}$              | 0            | -    | 0            | -    | ns   |
| Write Pulse Width                | $t_{WP}$              | 9            | -    | 10           | -    | ns   |
| Write Recovery Time              | $t_{WR}$              | 0            | -    | 0            | -    | ns   |
| Data to Write Time Overlap       | $t_{DW}$              | 7            | -    | 8            | -    | ns   |
| Data Hold from End of Write Time | $t_{DH}$              | 0            | -    | 0            | -    | ns   |
| Output Active from End of Write  | $t_{OW*}$             | 3            | -    | 4            | -    | ns   |
| Write to Output in High Z        | $t_{WHZ*}$            | -            | 7    | -            | 8    | ns   |

\*These parameters are guaranteed by device characterization, but not production tested.



## TIMING WAVEFORMS

## READ CYCLE 1 (Address Controlled) (1,2)

READ CYCLE 2 ( $\overline{CE}$  and CE2 and  $\overline{OE}$  Controlled) (1,3,4,5)

## Notes :

1.  $\overline{WE}$  is high for read cycle.
2. Device is continuously selected  $\overline{OE}$  =low,  $\overline{CE}$  =low, CE2=high.
3. Address must be valid prior to or coincident with  $\overline{CE}$  =low, CE2=high; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OHZ}$  are specified with  $C_L=5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .



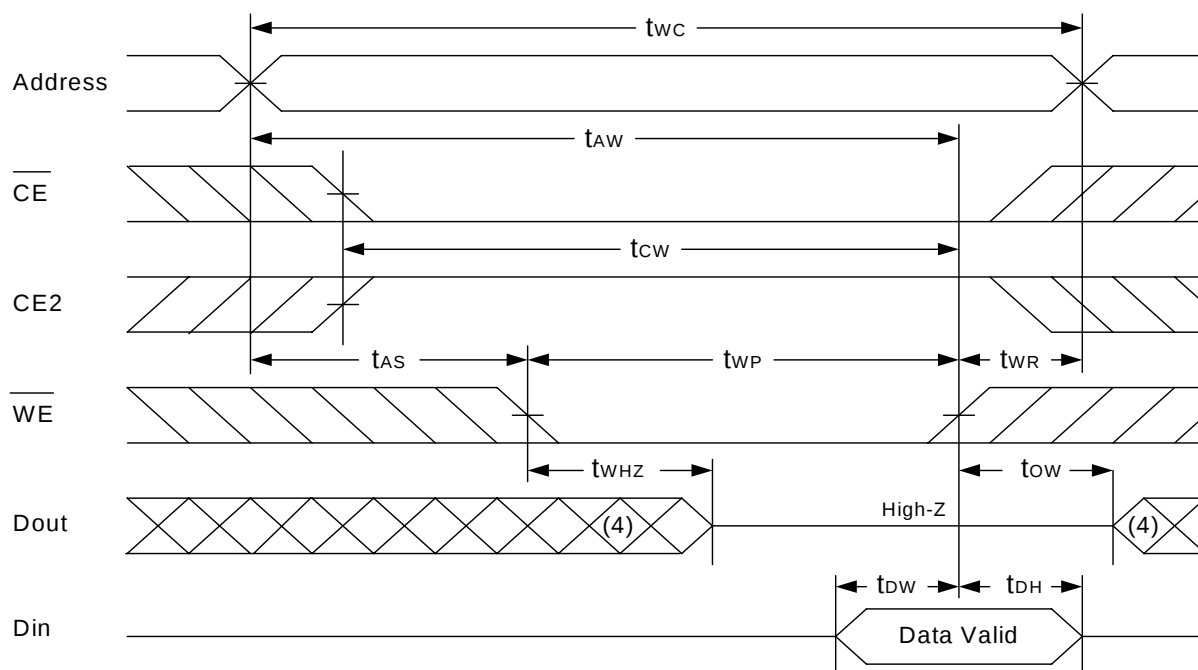
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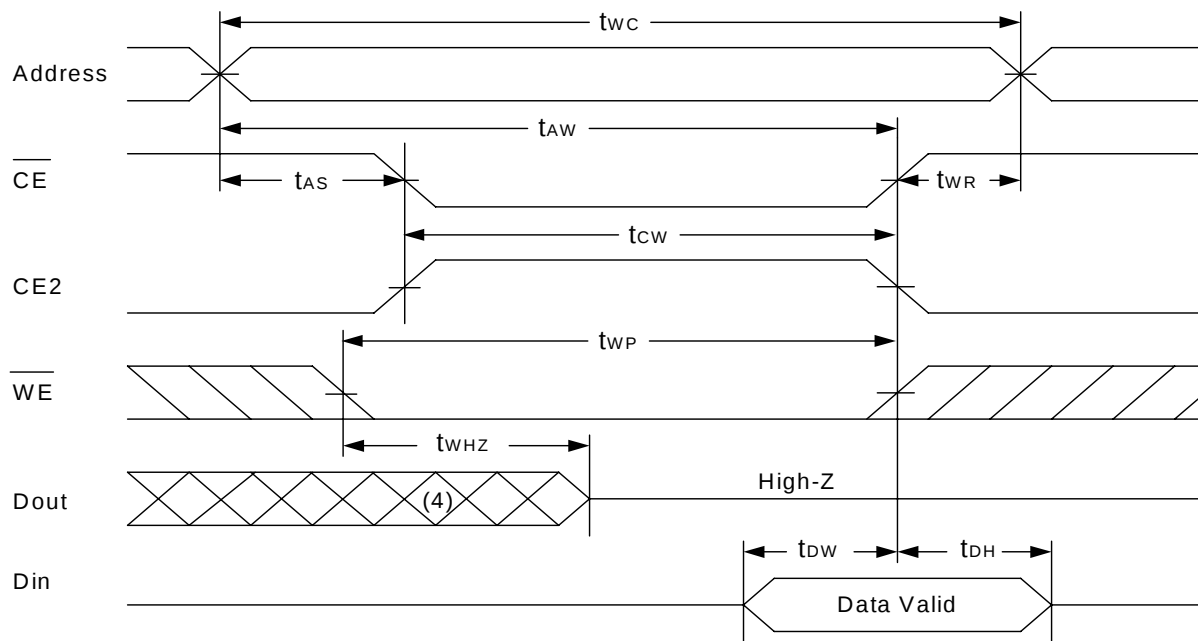
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**WRITE CYCLE 1** ( $\overline{WE}$  Controlled) (1,2,3,5,6)



**WRITE CYCLE 2** ( $\overline{CE}$  and  $\overline{CE2}$  Controlled) (1,2,5,6)





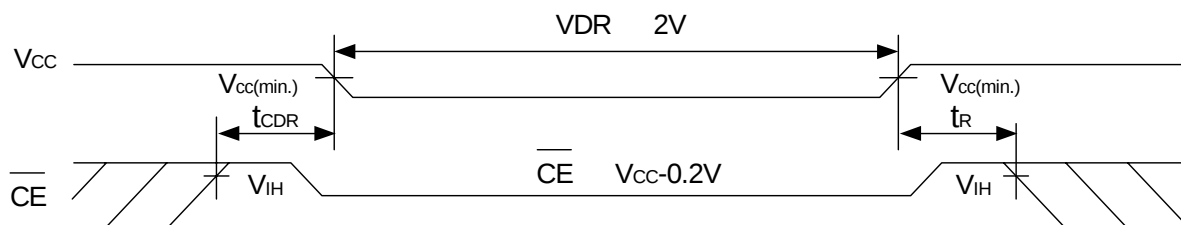
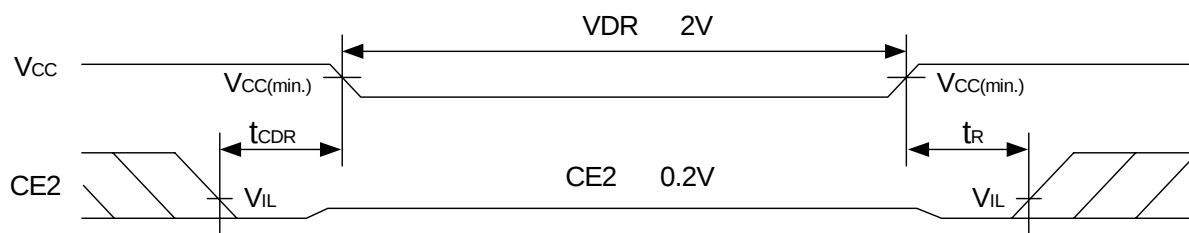
## Notes :

1.  $\overline{WE}$ ,  $\overline{CE}$  must be high or  $\overline{CE2}$  must be low during all address transitions.
2. A write occurs during the overlap of a low  $\overline{CE}$ , high  $\overline{CE2}$ , low  $\overline{WE}$ .
3. During a  $\overline{WE}$  controlled write cycle with  $\overline{OE}$  low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{DW}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CE}$  low transition and  $\overline{CE2}$  high transition occurs simultaneously with or after  $\overline{WE}$  low transition, the outputs remain in a high impedance state.
6.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.

DATA RETENTION CHARACTERISTICS ( $T_A = 0$  to  $+70$ )

| PARAMETER                           | SYMBOL    | TEST CONDITION                                                             | MIN. | MAX. | UNIT |
|-------------------------------------|-----------|----------------------------------------------------------------------------|------|------|------|
| Vcc for Data Retention              | $V_{DR}$  | $\overline{CE}$ $V_{CC}-0.2V$ or $\overline{CE2} \leq 0.2V$                | 2.0  | 3.6  | V    |
| Data Retention Current              | $I_{DR}$  | $V_{CC}=2V$<br>$\overline{CE}$ $V_{CC}-0.2V$ or $\overline{CE2} \leq 0.2V$ | -    | 3    | mA   |
| Chip Disable to Data Retention Time | $t_{CDR}$ | See Data Retention Waveforms                                               | 0    | -    | ms   |
| Recovery Time                       | $t_R$     |                                                                            | 5    | -    | ms   |

## DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) ( $\overline{CE}$  controlled)Low Vcc Data Retention Waveform (2) ( $\overline{CE2}$  controlled)



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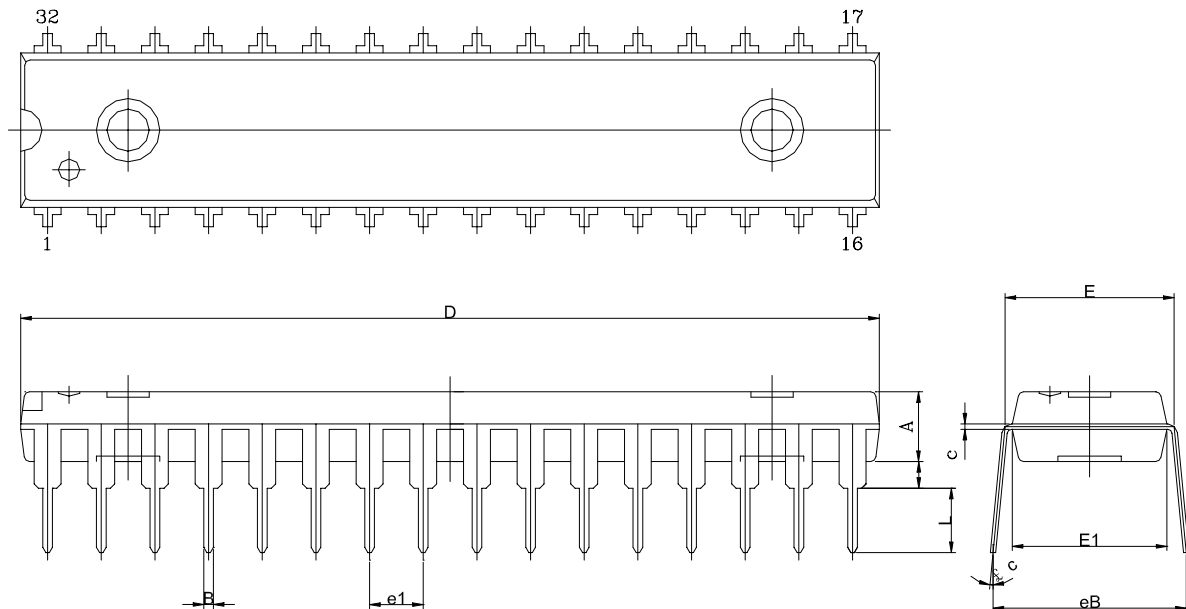
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## PACKAGE OUTLINE DIMENSION

### 32-pin Skinny PDIP Package Outline Dimension



| UNIT<br>SYMBOL | INCH(BASE)   | MM(REF)       |
|----------------|--------------|---------------|
| A              | 0.130 ±0.005 | 3.302 ±0.127  |
| B              | 0.018 ±0.004 | 0.457 ±0.102  |
| c              | 0.010 ±0.004 | 0.254 ±0.102  |
| D              | 1.600 ±0.005 | 40.640 ±0.127 |
| E              | 0.315 ±0.010 | 8.001 ±0.254  |
| E1             | 0.288 ±0.004 | 7.315 ±0.102  |
| e1             | 0.100 (TYP)  | 2.540 (TYP)   |
| eB             | 0.350 ±0.020 | 8.890 ±0.508  |
| L              | 0.125 (MIN)  | 3.175 (MIN)   |
| ±c             | 0° 10°       | 0° 10°        |



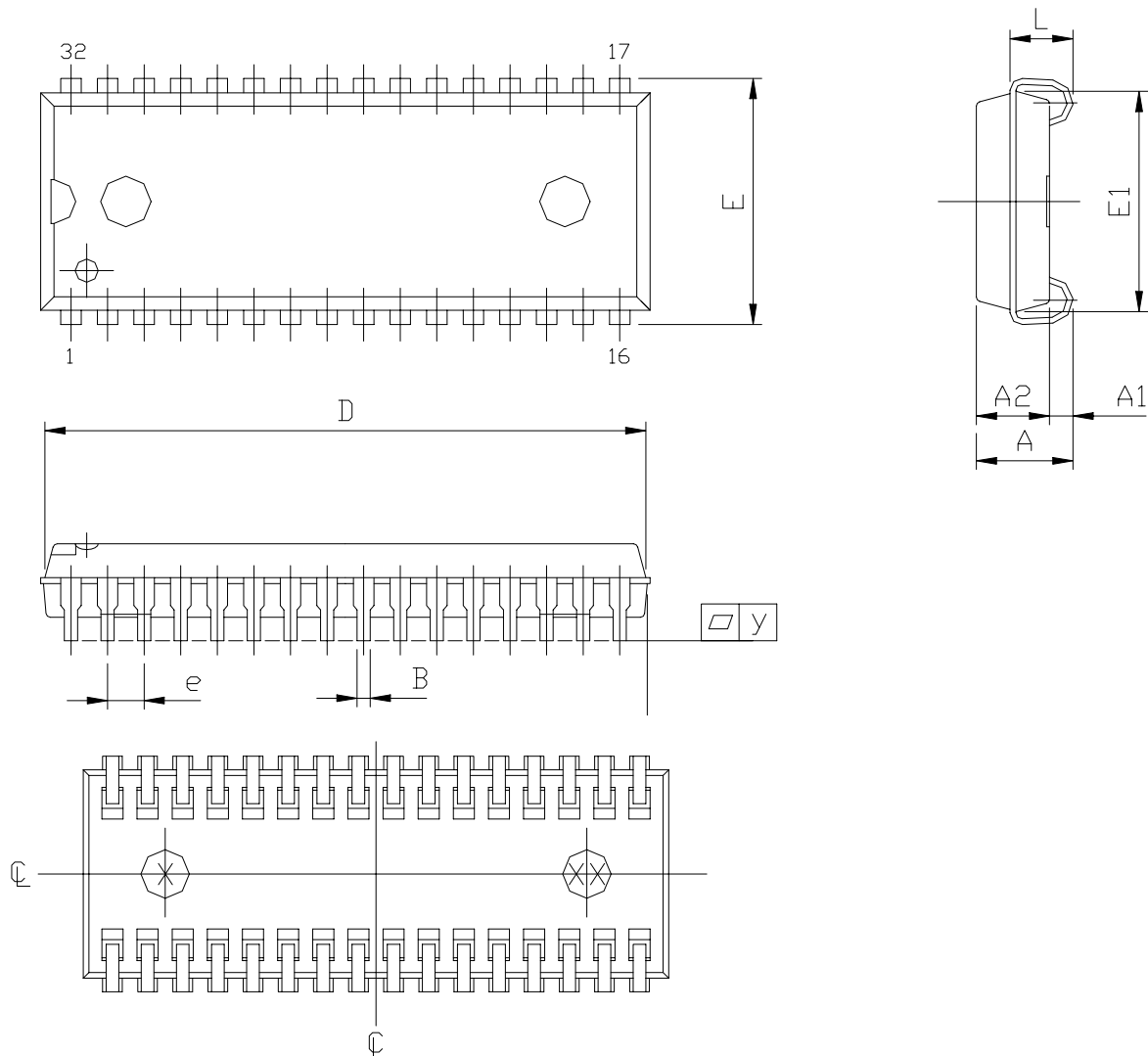
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32-pin 300mil SOJ Package Outline Dimension



| SYMBOL \ UNIT | INCH(BASE)   | MM(REF)      |
|---------------|--------------|--------------|
| A             | 0.148 (MAX)  | 3.759 (MAX)  |
| A1            | 0.026 (MIN)  | 0.660 (MIN)  |
| A2            | 0.100 ±0.005 | 2.540 ±0.127 |
| B             | 0.018 (TYP)  | 0.457 (TYP)  |
| D             | 0.830 (MAX)  | 21.082 (MAX) |
| E             | 0.335 (TYP)  | 8.509 (TYP)  |
| E1            | 0.300 ±0.005 | 7.620 ±0.127 |
| e             | 0.050 (TYP)  | 1.270 (TYP)  |
| L             | 0.086 ±0.010 | 2.184 ±0.254 |
| y             | 0.003 (MAX)  | 0.076 (MAX)  |



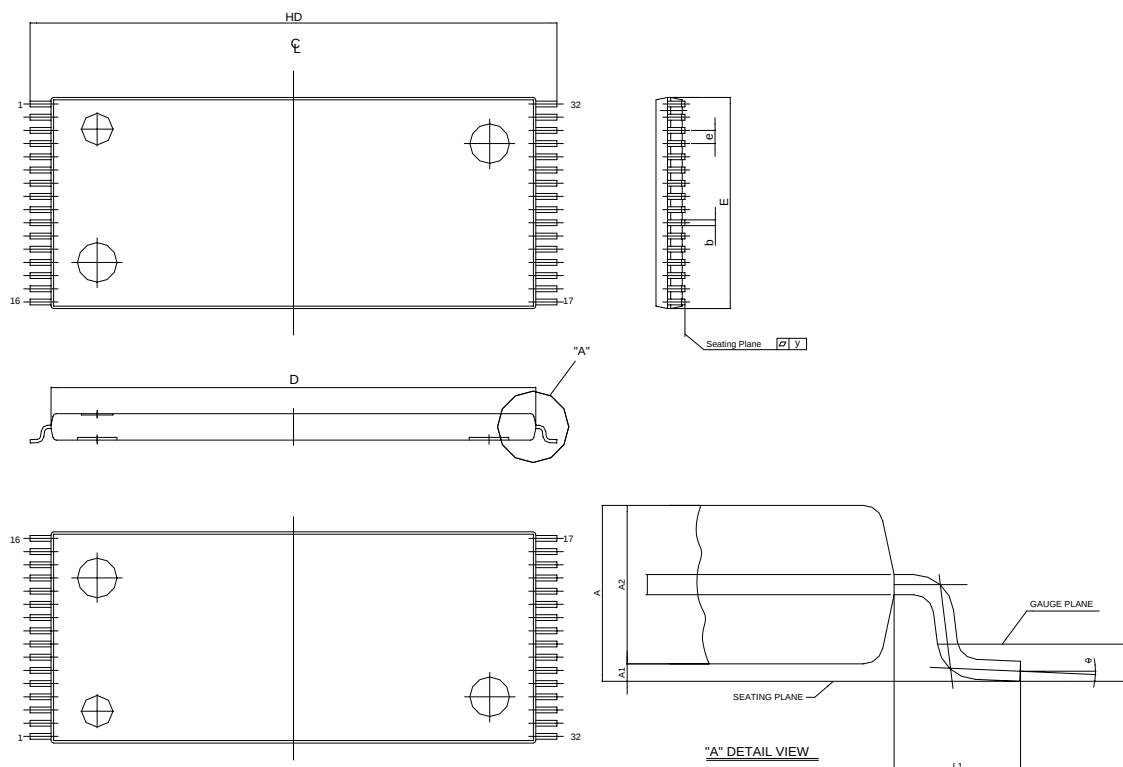
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## 128K X 8 BIT HIGH SPEED CMOS SRAM

### 32-pin 8mm × 20mm TSOP-I Package Outline Dimension



| UNIT<br>SYMBOL | INCH(BASE)               | MM(REF)              |
|----------------|--------------------------|----------------------|
| A              | 0.047 (MAX)              | 1.20 (MAX)           |
| A1             | 0.004 ±0.002             | 0.10 ±0.05           |
| A2             | 0.039 ±0.002             | 1.00 ±0.05           |
| b              | 0.008 + 0.002<br>- 0.001 | 0.20 + 0.05<br>-0.03 |
| D              | 0.724 ±0.004             | 18.40 ±0.10          |
| E              | 0.315 ±0.004             | 8.00 ±0.10           |
| e              | 0.020 (TYP)              | 0.50 (TYP)           |
| HD             | 0.787 ±0.008             | 20.00 ±0.20          |
| L1             | 0.0315 ±0.004            | 0.80 ±0.10           |
| y              | 0.003 (MAX)              | 0.076 (MAX)          |
| Θ              | 0° 5°                    | 0° 5°                |



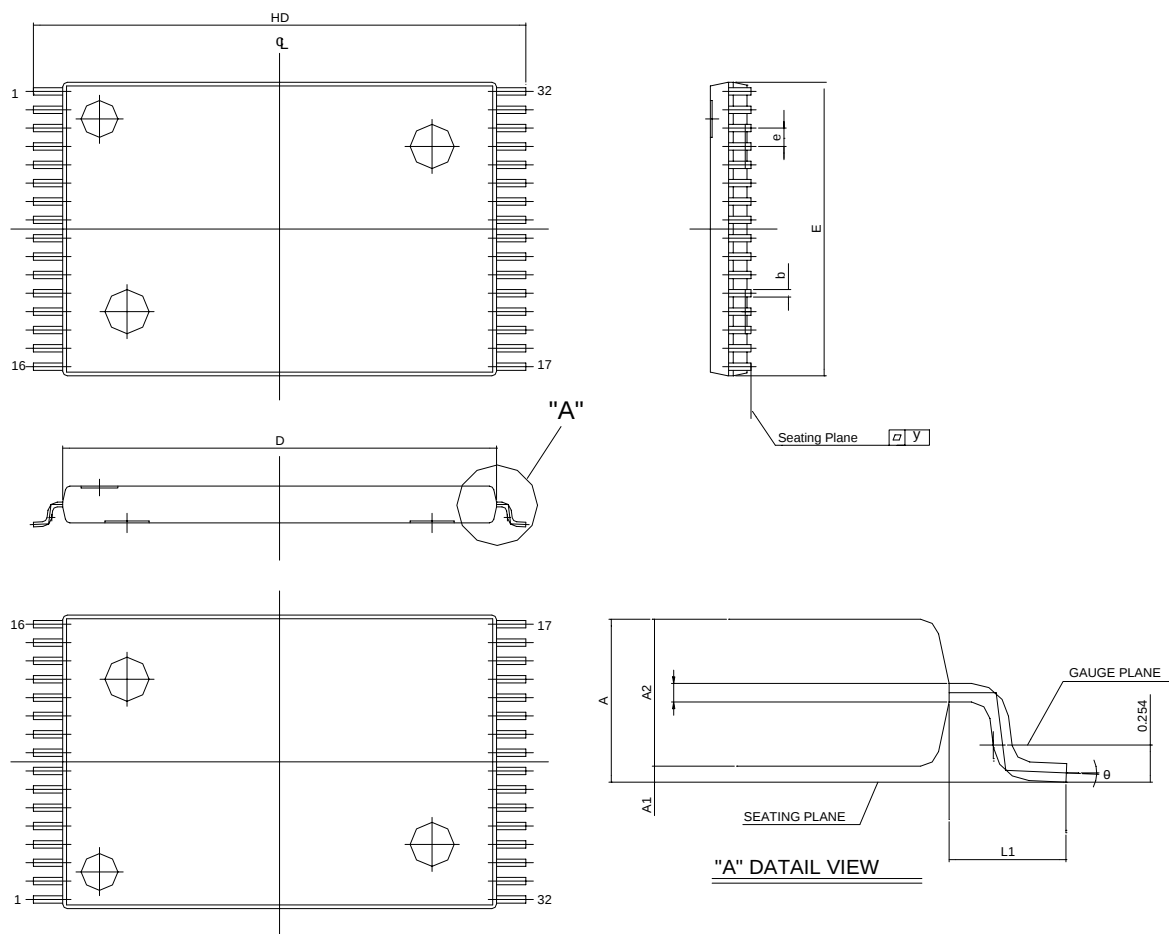
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32-pin 8mm x 13.4mm STSOP Package Outline Dimension



| SYMBOL | UNIT | INCH(BASE)    | MM(REF)       |
|--------|------|---------------|---------------|
| A      |      | 0.047 (MAX)   | 1.20 (MAX)    |
| A1     |      | 0.004 ±0.002  | 0.10 ±0.05    |
| A2     |      | 0.039 ±0.002  | 1.00 ±0.05    |
| b      |      | 0.008 ±0.001  | 0.200 ±0.025  |
| D      |      | 0.465 ±0.004  | 11.800 ±0.100 |
| E      |      | 0.315 ±0.004  | 8.000 ±0.100  |
| e      |      | 0.020 (TYP)   | 0.50 (TYP)    |
| HD     |      | 0.528 ±0.008  | 13.40 ±0.20.  |
| L1     |      | 0.0315 ±0.004 | 0.80 ±0.10    |
| y      |      | 0.003 (MAX)   | 0.076 (MAX)   |
| Θ      |      | 0° 5°         | 0° 5°         |



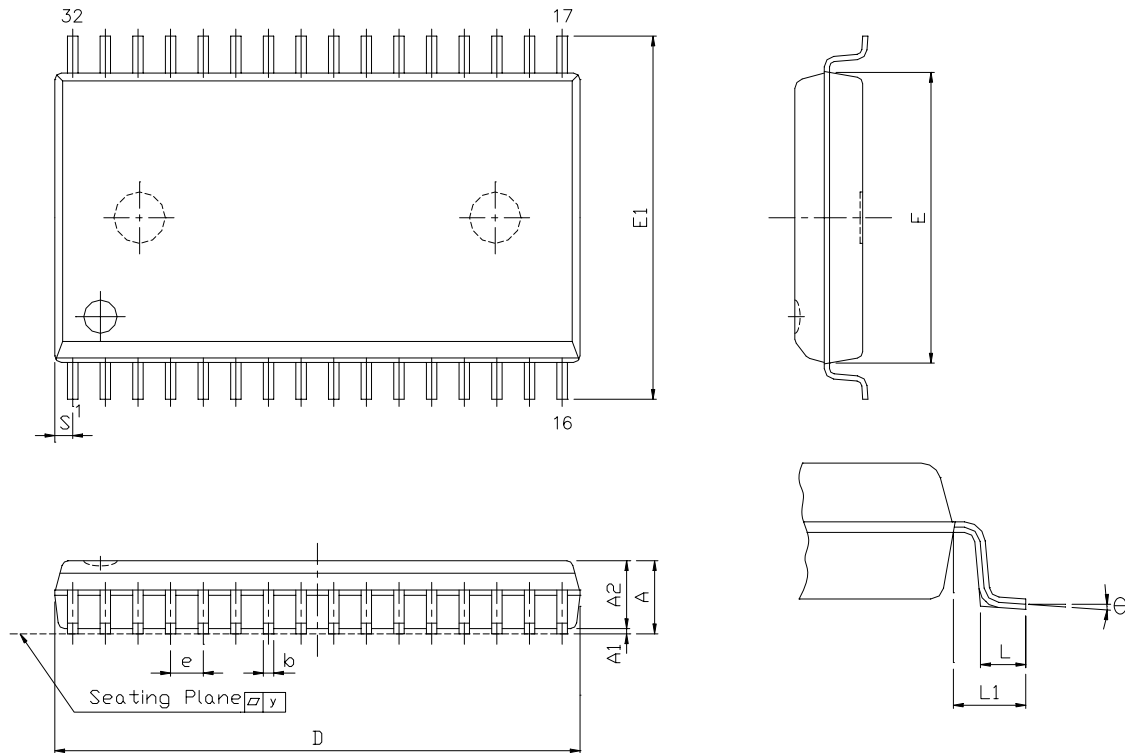
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32-pin 450mil SOP Package Outline Dimension



| SYMBOL \ UNIT | INCH(BASE)    | MM(REF)       |
|---------------|---------------|---------------|
| A             | 0.118 (MAX)   | 2.997 (MAX)   |
| A1            | 0.004 (MIN)   | 0.102 (MIN)   |
| A2            | 0.111 (MAX)   | 2.82 (MAX)    |
| b             | 0.016 (TYP)   | 0.406 (TYP)   |
| D             | 0.817 (MAX)   | 20.75 (MAX)   |
| E             | 0.445 ±0.005  | 11.303 ±0.127 |
| E1            | 0.555 ±0.012  | 14.097 ±0.305 |
| e             | 0.050 (TYP)   | 1.270 (TYP)   |
| L             | 0.0347 ±0.008 | 0.881 ±0.203  |
| L1            | 0.055 ±0.008  | 1.397 ±0.203  |
| S             | 0.026 (MAX)   | 0.660 (MAX)   |
| y             | 0.004 (MAX)   | 0.101 (MAX)   |
| Θ             | 0°~10°        | 0°~10°        |



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## ORDERING INFORMATION

| PART NO.       | ACCESS TIME (ns) | PACKAGE           |
|----------------|------------------|-------------------|
| UT61L1024KC-12 | 12               | 32PIN SKINNY PDIP |
| UT61L1024KC-15 | 15               | 32PIN SKINNY PDIP |
| UT61L1024JC-12 | 12               | 32PIN SOJ         |
| UT61L1024JC-15 | 15               | 32PIN SOJ         |
| UT61L1024SC-12 | 12               | 32PIN SOP         |
| UT61L1024SC-15 | 15               | 32PIN SOP         |
| UT61L1024LC-12 | 12               | 32PIN TSOP-1      |
| UT61L1024LC-15 | 15               | 32PIN TSOP-1      |
| UT61L1024LS-12 | 12               | 32PIN STSOP       |
| UT61L1024LS-15 | 15               | 32PIN STSOP       |

## ORDERING INFORMATION (for lead free product)

| PART NO.        | ACCESS TIME (ns) | PACKAGE           |
|-----------------|------------------|-------------------|
| UT61L1024KCL-12 | 12               | 32PIN SKINNY PDIP |
| UT61L1024KCL-15 | 15               | 32PIN SKINNY PDIP |
| UT61L1024JCL-12 | 12               | 32PIN SOJ         |
| UT61L1024JCL-15 | 15               | 32PIN SOJ         |
| UT61L1024SCL-12 | 12               | 32PIN SOP         |
| UT61L1024SCL-15 | 15               | 32PIN SOP         |
| UT61L1024LCL-12 | 12               | 32PIN TSOP-1      |
| UT61L1024LCL-15 | 15               | 32PIN TSOP-1      |
| UT61L1024LSL-12 | 12               | 32PIN STSOP       |
| UT61L1024LSL-15 | 15               | 32PIN STSOP       |



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