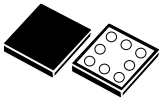
# LD3986 SERIES

## DUAL ULTRA LOW DROP-LOW NOISE BICMOS VOLTAGE REG. FOR USE WITH VERY LOW ESR OUT. CAPACITORS

- INPUT VOLTAGE FROM 2.5V TO 6V
- STABLE WITH LOW ESR CERAMIC CAPACITORS
- ULTRA LOW DROPOUT VOLTAGE (60mV TYP. AT 150mA LOAD, 0.4mV TYP. AT 1mA LOAD)
- VERY LOW QUIESCENT CURRENT (155µA TYP. AT NO LOAD, 290µA TYP. AT 150mA LOAD; MAX 2µA IN OFF MODE)
- GUARANTEED OUTPUT CURRENT UP TO 150mA FOR BOTH OUTPUTS
- DUAL OUTPUT VOLTAGES
- FAST TURN-ON TIME: TYP. 120µs ($C_O$=1µF, $C_{BYP}$=10nF AND $I_O$=1mA)
- LOGIC-CONTROLLED ELECTRONIC SHUTDOWN
- INTERNAL CURRENT AND THERMAL LIMIT
- OUTPUT LOW NOISE VOLTAGE 30µ$V_{RMS}$ OVER 10Hz to 100KHz
- S.V.R. OF 50dB AT 1KHz, 40dB AT 10KHz
- TEMPERATURE RANGE: -40°C TO 125°C

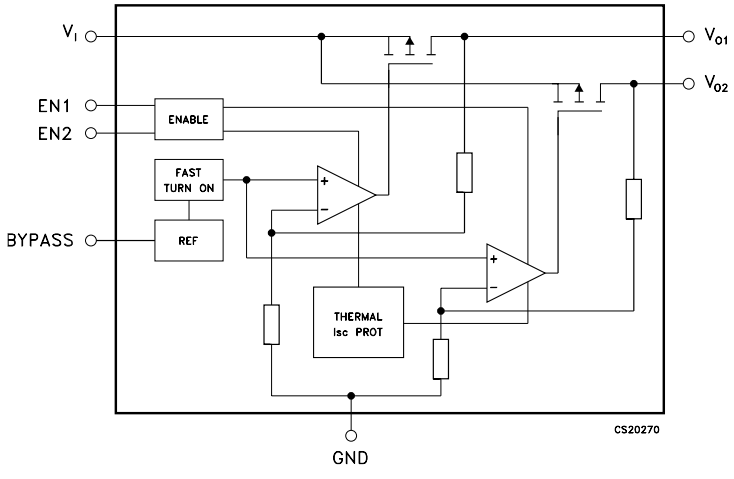


**Flip-Chip**

### DESCRIPTION

The LD3986 provides up to 150mA at each output, from 2.5V to 6V input voltage. The ultra low drop-voltage, low quiescent current and low noise make it suitable for low power applications and in battery powered systems. Regulator ground current increases only slightly in dropout, further prolonging the battery life. Power supply rejection is 50 dB at 1KHz and 40 dB at 10KHz. High power supply rejection is maintained down to low input voltage levels common to battery operated circuits. Shutdown Logic Control function is available for each output, this means that when the device is used as local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. The LD3986 is designed to work with low ESR ceramic capacitors. Typical applications are in mobile phone and similar battery powered wireless systems.

**Figure 1: Schematic Diagram**



### Table 1: Order Codes

| Flip-Chip | 1 OUTPUT VOLTAGES | 2 OUTPUT VOLTAGES |
|---|---|---|
| LD3986J12248R (*) | 1.22 V | 4.8 V |
| LD3986J2528R (*) | 2.5 V | 2.8 V |
| LD3986J2818R (*) | 2.8 V | 1.8 V |
| LD3986J285R | 2.85 V | 2.85 V |
| LD3986J29R (*) | 2.9 V | 2.9 V |
| LD3986J30R (*) | 3.0 V | 3.0 V |
| LD3986J2830R (*) | 2.8 V | 3.0 V |
| LD3986J3131R (*) | 3.1 V | 3.1 V |
| LD3986J3133R (*) | 3.1 V | 3.3 V |
| LD3986J3333R (*) | 3.3 V | 3.3 V |

(*) Available on Request.

### Table 2: Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_I$ | DC Input Voltage | -0.3 to 6 | V |
| $V_{O1,2}$ | DC Output Voltage | -0.3 to $V_I$+0.3 | V |
| $V_{EN1,2}$ | ENABLE Input Voltage | -0.3 to $V_I$+0.3 | V |
| $I_O$ | Output Current | Internally limited | |
| $P_D$ | Power Dissipation | Internally limited | |
| $T_{STG}$ | Storage Temperature Range | -65 to 150 | °C |
| $T_{OP}$ | Operating Junction Temperature Range | -40 to 125 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

### Table 3: Thermal Data

| Symbol | Parameter | Flip-Chip | Unit |
|---|---|---|---|
| $R_{thj\text{-}amb}$ | Thermal Resistance Junction-Ambient | 120 | °C/W |

**Figure 2: Pin Connection** (top through view)

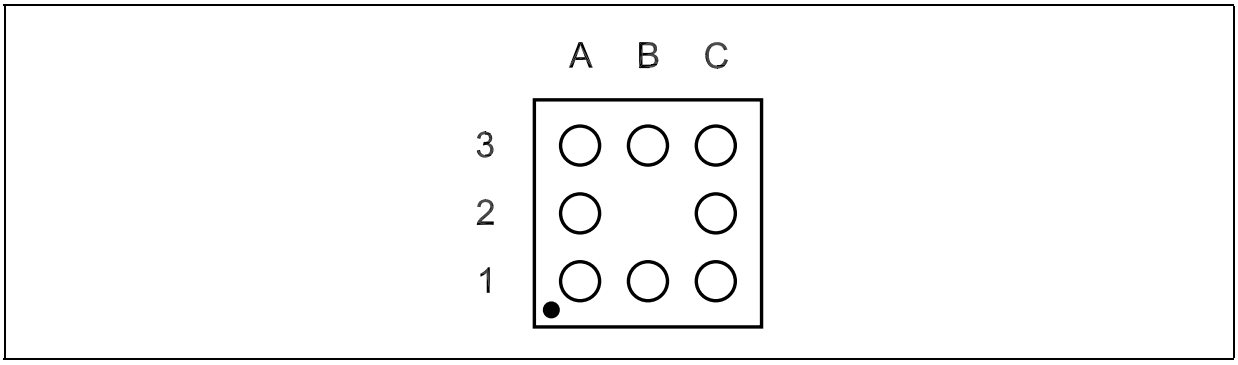



**Table 4: Pin Description**

| Symbol | Pin N° | Name and Function |
|---|---|---|
| $V_{O2}$ | A1 | Output Voltage 2 of the dual LDO |
| EN2 | B1 | Enables voltage for output voltage 2: ON MODE when $V_{EN} \geq 1.4V$, OFF MODE when $V_{EN} \leq 0.4V$ (Do not leave floating, not internally pulled down/up) |
| BYPASS | C1 | Bypass Pin: Connect an external capacitor (usually 10nF) to minimize noise voltage |
| GND | C2 | Common Ground |
| GND | C3 | Common Ground |
| EN1 | B3 | Enables voltage for output voltage 1: ON MODE when $V_{EN} \geq 1.4V$, OFF MODE when $V_{EN} \leq 0.4V$ (Do not leave floating, not internally pulled down/up) |
| $V_{O1}$ | A3 | Output Voltage 1 of the dual LDO |
| $V_I$ | A2 | Input Voltage for both LDO |

**Figure 3: Typical Application Circuit**

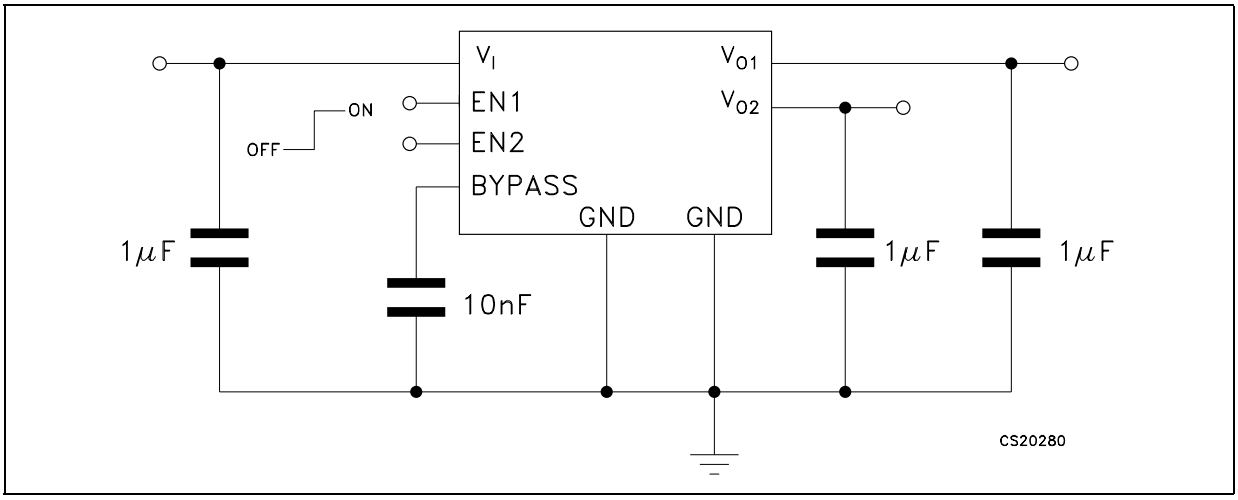


**Table 5: Electrical Characteristics For LD3986** ($T_j$ = 25°C, $V_I = V_{O(NOM)}$ +0.5V, $C_I = C_O$ =1µF, $C_{BYP}$ = 10nF, $I_O$ = 1mA, $V_{EN}$ = 1.4V, unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_I$ | Operating Input Voltage | | 2.5 | | 6 | V |
| $\Delta V_O$ | Output Voltage Tolerance | $I_O$ = 1mA | -2.5 | | 2.5 | % of $V_O$ |
| | | $T_J$= -40 to 125°C | -3 | | 3 | |
| $\Delta V_O$ | Line Regulation (Note 1) | $V_I = V_{O(NOM)}$ + 0.5 V to 6V | | 0.006 | 0.092 | %/V |
| | | $T_J$= -40 to 125°C | | | 0.128 | |
| $\Delta V_O$ | Load Regulation | $I_O$ = 1 mA to 150mA | | 0.003 | 0.006 | %/mA |
| | | $T_J$= -40 to 125°C | | | 0.01 | |
| $\Delta V_O$ | Output AC Line Regulation (See fig. 5) | $V_I = V_{O(NOM)}$ + 1 V, $I_O$ = 150mA, $t_R = t_F$ = 30µs | | 1.5 | | $mV_{PP}$ |
| $I_Q$ | Quiescent Current BOTH ON MODE: $V_{EN}$ = 1.4V | $I_O$ = 0 | | 150 | | µA |
| | | $I_O$ = 0 $T_J$= -40 to 125°C | | | 200 | |
| | | $I_O$ = 0 to 150mA | | 290 | | |
| | | $I_O$ = 0 to 150mA $T_J$= -40 to 125°C | | | 370 | |
| | BOTH OFF MODE: $V_{EN}$ = 0.4V | | | 0.001 | 2 | |
| | | $T_J$= -40 to 125°C | | | 4 | |
| | ONE REGULATOR ON MODE: $V_{EN}$ = 1.4V | $I_O$ = 0 | | 95 | | |
| | | $I_O$ = 0 $T_J$= -40 to 125°C | | | 130 | |
| | | $I_O$ = 0 to 150mA | | 165 | | |
| | | $I_O$ = 0 to 150mA $T_J$= -40 to 125°C | | | 220 | |
| $V_{DROP}$ | Dropout Voltage (Note 2) | $I_O$ = 1mA | | 0.4 | | mV |
| | | $I_O$ = 1mA $T_J$= -40 to 125°C | | | 2 | |
| | | $I_O$ = 150mA | | 50 | | |
| | | $I_O$ = 150mA $T_J$= -40 to 125°C | | | 100 | |
| SVR | Supply Voltage Rejection (See fig. 4) | $V_I = V_{O(NOM)}$+0.25V ± $V_{RIPPLE}$ = 0.1V, $I_O$= 50mA $V_{O(NOM)}$ < 2.5V, $V_I$ = 2.55V — f = 1KHz | | 50 | | dB |
| | | f = 10KHz | | 40 | | |
| $I_{SC}$ | Short Circuit Current | $R_L$ = 0 | | 600 | | mA |
| $I_{O(PK)}$ | Peak Output Current | $V_O \geq V_{O(NOM)}$ - 5% | 300 | 550 | | mA |
| $V_{EN}$ | Enable Input Logic Low (Note 3) | $V_I$ = 2.5V to 6V $T_J$= -40 to 125°C | | | 0.4 | V |
| | Enable Input Logic High (Note 3) | | 1.4 | | | |
| $I_{EN}$ | Enable Input Current | $V_{EN}$ = 0.4V $V_I$ = 6V | | ±10 | | nA |
| $X_{TALK}$ | Crosstalk Rejection | $\Delta I_{LOAD1}$ = 150 mA at 1KHz rate $I_{LOAD2}$ = 1 mA, $V_{O2}$ under test | | 40 | | µV |
| | | $\Delta I_{LOAD2}$ = 150 mA at 1KHz rate $I_{LOAD1}$ = 1 mA, $V_{O1}$ under test | | 40 | | |
| eN | Output Noise Voltage | $B_W$ = 10 Hz to 100 KHz $C_O$ = 1 µF | | 30 | | $\mu V_{RMS}$ |
| $t_{ON}$ | Turn On Time (Note 4) | $C_{BYP}$ = 10 nF | | 50 | | µs |
| $T_{SHDN}$ | Thermal Shutdown (Note 4) | (Note 3) | | 160 | | °C |

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_O$ | Output Capacitor | Capacitance | 1 | | 22 | µF |
| | | ESR | 0.005 | | 5 | Ω |

Note 1: For $V_O$< 2V, $V_I$=2.5V
Note 2: Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply for input voltages below 2.5V.
Note 3: Enable pin must be driven with a $T_R = T_F < 10ms$
Note 4: Turn-on time is time measured between the enable input just exceeding $V_{INH}$ High Value and the output voltage just reaching 95% of its nominal value
Note 5: Typical thermal protection hysteresis is 20°C

**Figure 4: SVR Input Voltage Test Signal**

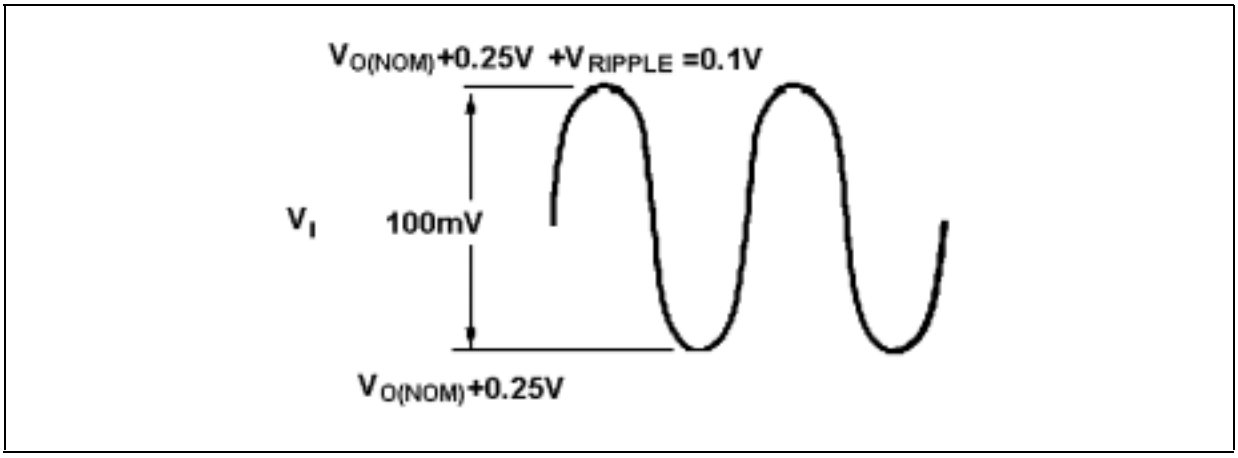
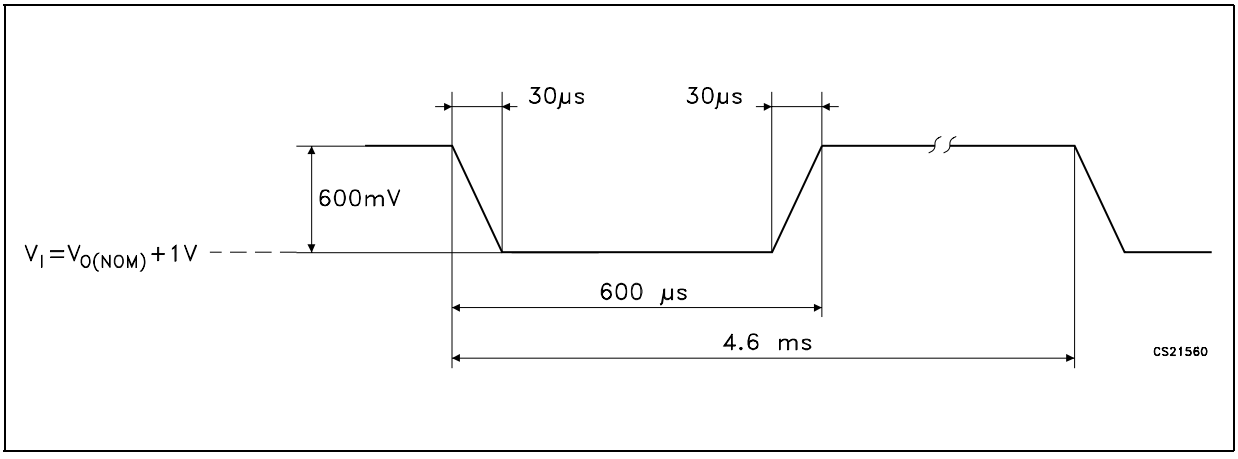



**Figure 5: AC Line Regulation Input Voltage Test Signal**



**TYPICAL PERFORMANCE CHARACTERISTICS** ($T_j$ = 25°C, $V_I = V_{O(NOM)}$ +0.5V, $C_I = C_O$ = 1µF, $C_{BYP}$ = 10nF, $I_O$ = 1mA, $V_{EN}$ = 1.4V, unless otherwise specified)

**Figure 6:** $V_{O1,2}$ vs Temperature

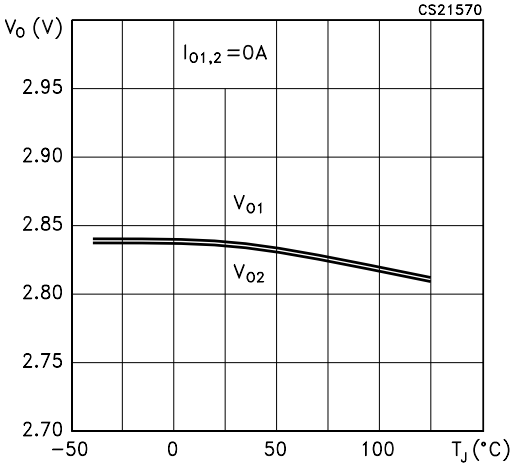



**Figure 7:** $V_{O1,2}$ vs Temperature

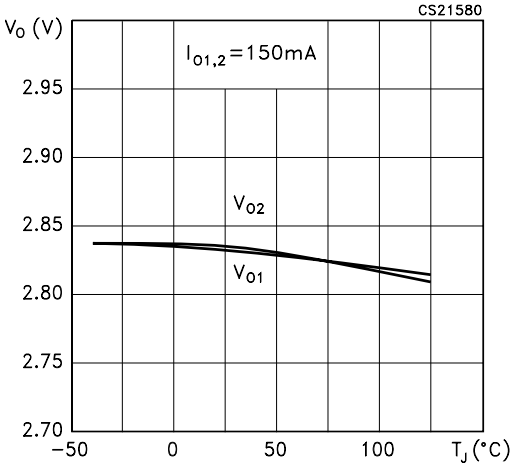



**Figure 8:** Line Regulation vs Temperature

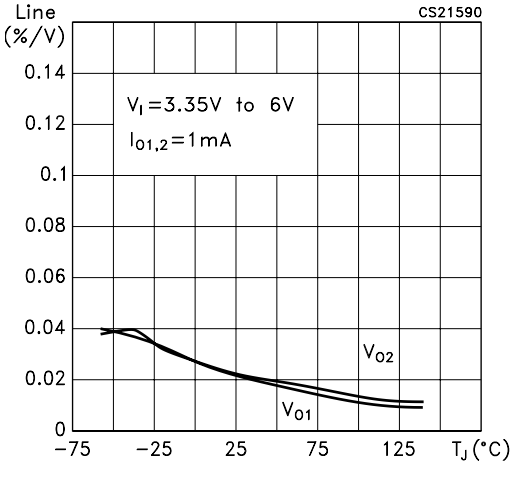



**Figure 9:** Load Regulation vs Temperature

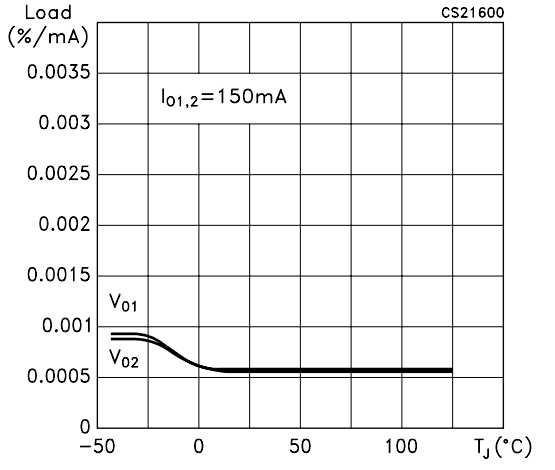



**Figure 10:** Quiescent Current vs Temperature

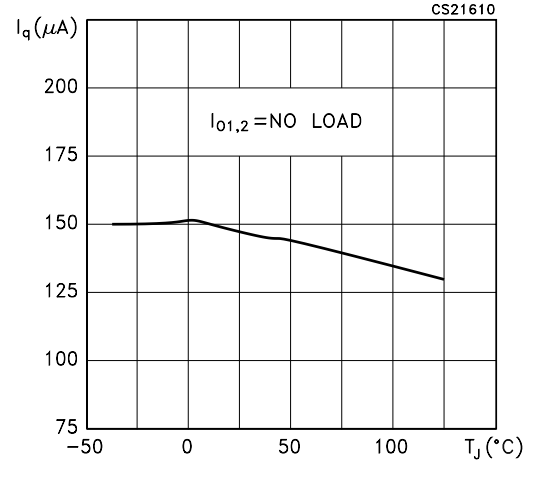



**Figure 11:** Quiescent Current vs Temperature

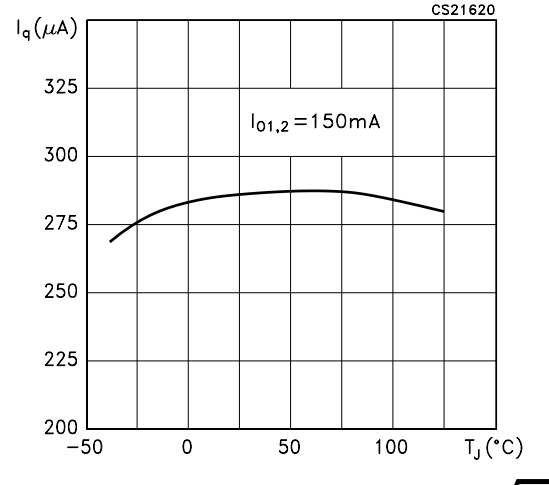


**Figure 12:** Supply Voltage Rejection vs Frequency

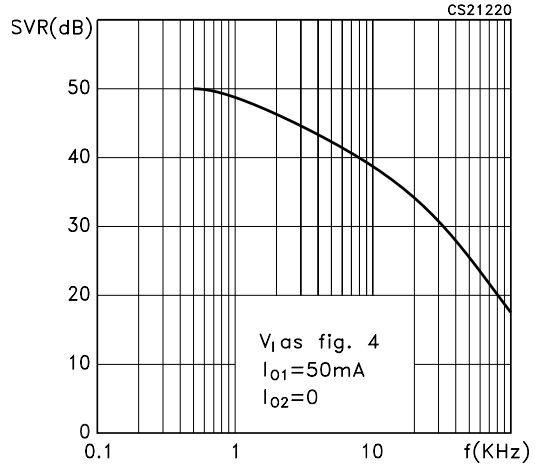



**Figure 13:** Supply Voltage Rejection vs Temperature

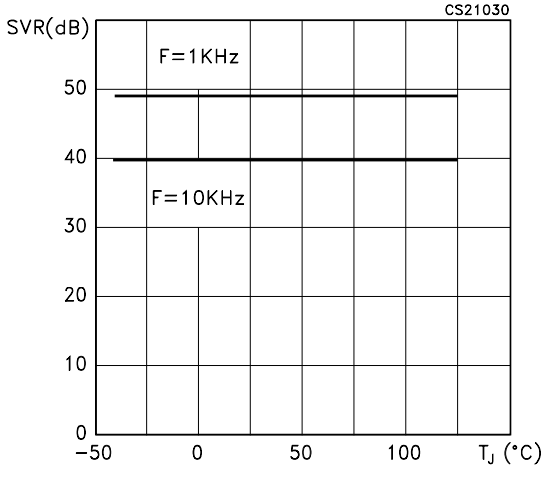
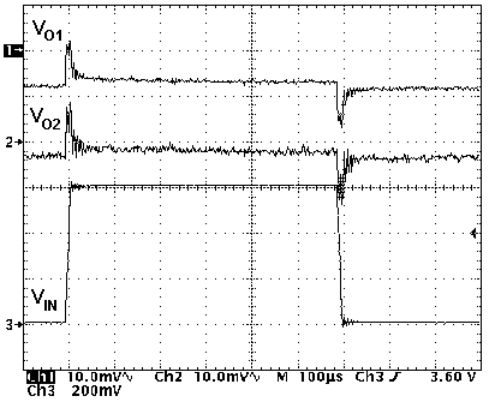
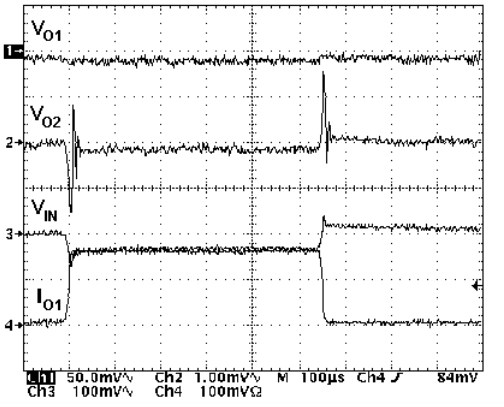



**Figure 14:** Line Transient Response



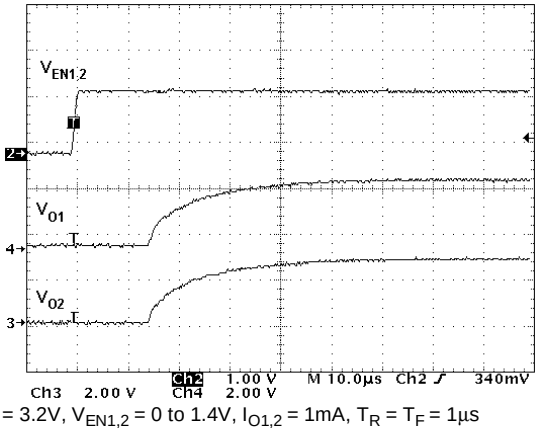

$V_I$ = 3.2V to 3.8V, $I_{O1}$ = $I_{O2}$ = 150mA, $T_R$ = $T_F$ = 10µs

**Figure 15:** Load Transient Response



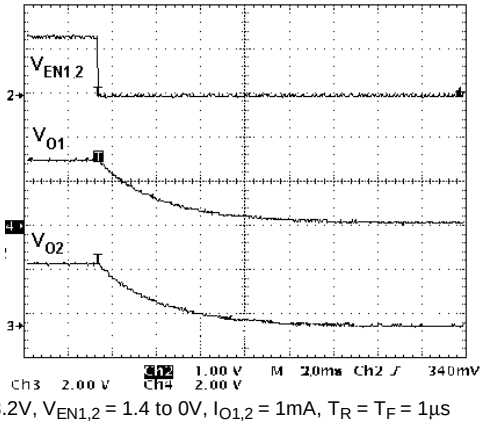

$I_{O1}$ = 1 mA, $I_{O2}$ = 0mA, $T_R$ = $T_F$ = 10µs

**Figure 16:** TURN-ON




$V_I$ = 3.2V, $V_{EN1,2}$ = 0 to 1.4V, $I_{O1,2}$ = 1mA, $T_R$ = $T_F$ = 1µs

**Figure 17:** TURN-OFF




$V_I$ = 3.2V, $V_{EN1,2}$ = 1.4 to 0V, $I_{O1,2}$ = 1mA, $T_R$ = $T_F$ = 1µs

## APPLICATION INFORMATION

### CURRENT LIMIT

The device includes short-circuit protection. It includes a current limiter that controls the pass transistor's gate voltage to limit the output current to about 600mA.

### THERMAL OVERLOAD PROTECTION

The Thermal over load protection limits total power dissipation in the device. When the junction temperature ($T_J$) exceeds +160°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistors and allowing the device to cool. The pass transistors turns on again after the device's junction temperature typically cools by 20°C, resulting in a pulsed output during continuous thermal overload conditions.

### POWER DISSIPATION

Maximum power dissipation of the device depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipated by the device is:

$$P_D = I_O (V_I - V_O)$$

The maximum power dissipation is:

$$P_{MAX} = (T_{JMAX} - T_A) / R_{TH}$$

Where:
$T_{JMAX}$ = +125°C
$T_A$ is the ambient temperature
$R_{TH}$ thermal resistance.
The device's pins perform the dual function of providing an electrical connection as well as channeling heat away from the die. Use wide circuit-board traces and large, solid copper polygons to improve power dissipation. Using multiple vias to buried ground planes further enhances thermal conductivity.

### INPUT CAPACITOR

An input capacitance of ≈ 1µF is required between the LD3986 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.
There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure
the capacitance will be ≈ 1µF over the entire operating temperature range.

### OUTPUT CAPACITOR

The LD3986 is designed specifically to work with very small ceramic output capacitors, any ceramic capacitor (temperature characteristics X7R, X5R, Z5U or Y5V) in 1 to 22 µF range with 5m. to 500m. ESR range is suitable in the LD3986 application circuit. it may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost.
The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range.

### NOISE BYPASS CAPACITOR

Connecting a 0.01µF capacitor between the $C_{BYP}$ pin and ground significantly reduces noise on both regulator outputs.
This cap is connected directly to a high impedance node in the band gap reference circuit. Any significant loading on this node will cause a change on the regulated output voltage.
For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy. The use of this 0.01µF bypass capacitor is strongly recommended to prevent overshoot on the output during start up.
The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. Polypropylene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current. Unlike many other LDO's, addition of a noise reduction capacitor does not effect the transient response of the device.

### TURN-ON/OFF INPUT OPERATION

Each LD3986 output is turned off by pulling the relevant EN pin low, and turned on by pulling it high. To assure proper operation, the signal

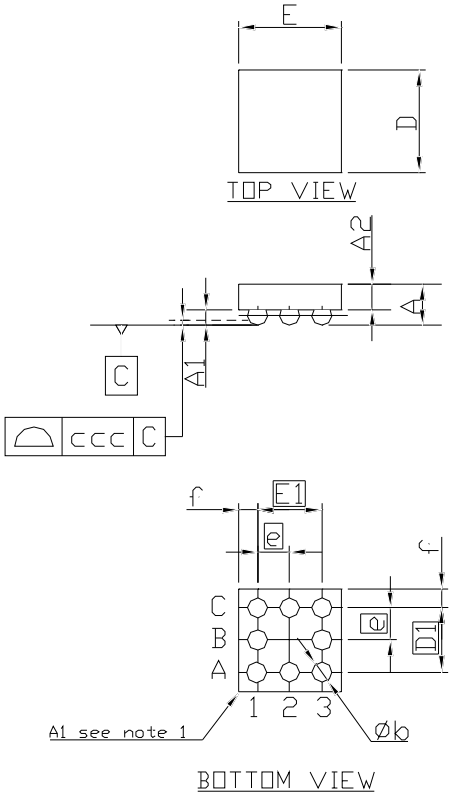
source used to drive the EN input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under Enable Input Logic Low and Enable Input Logic High.
Proper operation of the Enable function is guaranteed by driving EN pins with $T_R$ and $T_F$ = 10 ms.

**FAST ON-TIME**

The LD3986 outputs are turned on after $V_{REF}$ voltage reaches its final value (1.23V nominal). To speed up this process, the noise reduction capacitor at the bypass pin is charged with an internal 70µA current source. The current source is turned off when the bandgap voltage reaches approximately 95% of its final value. The turn on time is determined by the time constant of the bypass capacitor. The smaller the capacitor value, the shorter the turn on time, but less noise gets reduced. As a result, turn on time and noise reduction need to be taken into design consideration when choosing the value of the bypass capacitor.

## Flip-Chip8 MECHANICAL DATA

| DIM. | mm. | | | mils | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 0.585 | 0.65 | 0.715 | 23.0 | 25.6 | 28.1 |
| A1 | 0.21 | 0.25 | 0.29 | 8.3 | 9.8 | 11.4 |
| A2 | | 0.40 | | | 15.7 | |
| b | 0.265 | 0.315 | 0.365 | 10.4 | 12.4 | 14.4 |
| D | 1.52 | 1.57 | 1.62 | 59.8 | 61.8 | 63.8 |
| D1 | | 1 | | | 39.4 | |
| E | 1.52 | 1.57 | 1.62 | 59.8 | 61.8 | 63.8 |
| E1 | | 1 | | | 39.4 | |
| e | 0.45 | 0.5 | 0.55 | 17.7 | 19.7 | 20.7 |
| f | | 0.285 | | | 11.2 | |
| ccc | | 0.080 | | | 3.1 | |




7224720E

**Table 6: Revision History**

| Date | Revision | Description of Changes |
|---|---|---|
| 07-Dec-2004 | 1 | First Release. |