

9-bit bus interface latch with set and reset (3-State)

74ABT843

FEATURES

- High speed parallel latches
- Extra data width for wide address/data paths or buses carrying parity
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Slim DIP 300 mil package
- Broadside pinout
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Power-up 3-State
- Power-up reset

DESCRIPTION

The 74ABT843 Bus interface latch is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT843 consists of nine D-type latches with 3-State outputs. In addition to the LE and OE pins, it has a Master Reset (MR) pin and Preset (PRE) pin. These pins are ideal for parity bus interfacing in high performance systems. When MR is Low, the outputs are Low if OE is Low. When MR is High, data can be entered into the latch. When PRE is Low, the outputs are High, if OE is Low. PRE overrides MR.

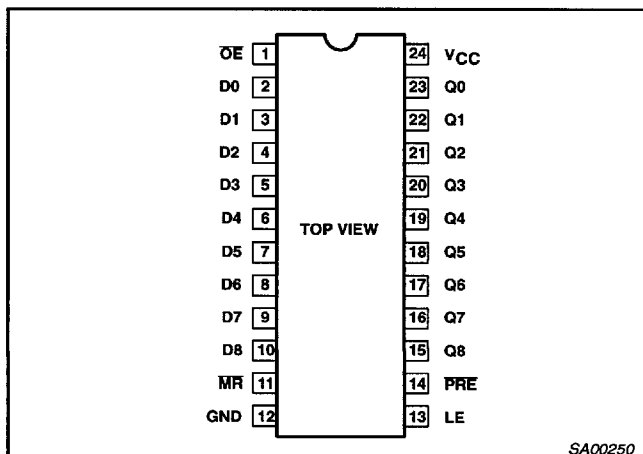
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	$C_L = 50\text{pF}$; $V_{CC} = 5\text{V}$	5.0	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	-40°C to $+85^{\circ}\text{C}$	74ABT843 N	74ABT843 N	SOT1222-1
24-Pin plastic SO	-40°C to $+85^{\circ}\text{C}$	74ABT843 D	74ABT843 D	SOT137-1
24-Pin Plastic SSOP Type II	-40°C to $+85^{\circ}\text{C}$	74ABT843 DB	74ABT843 DB	SOT340-1
24-Pin Plastic TSSOP Type I	-40°C to $+85^{\circ}\text{C}$	74ABT843 PW	74ABT843PW DH	SOT355-1

PIN CONFIGURATION



PIN DESCRIPTION

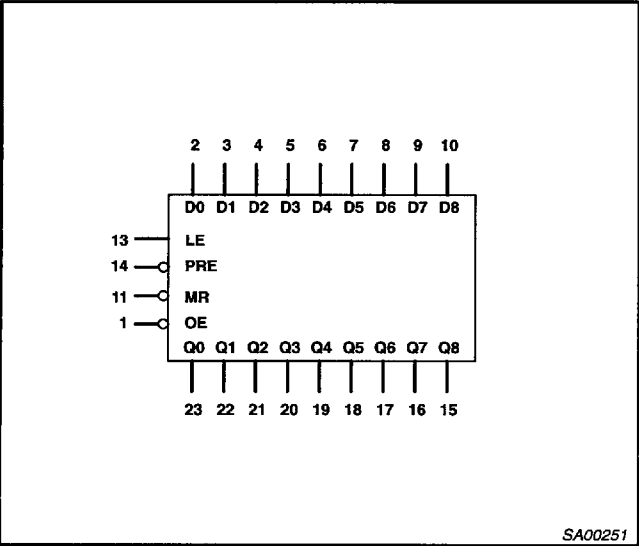
PIN NUMBER	SYMBOL	FUNCTION
1	OE	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10	D0-D8	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15	Q0-Q8	Data outputs
11	MR	Master reset input (active-Low)
13	LE	Latch enable input (active rising edge)
14	PRE	Preset input (active-Low)
12	GND	Ground (0V)
24	VCC	Positive supply voltage

9-bit bus interface latch with set and reset

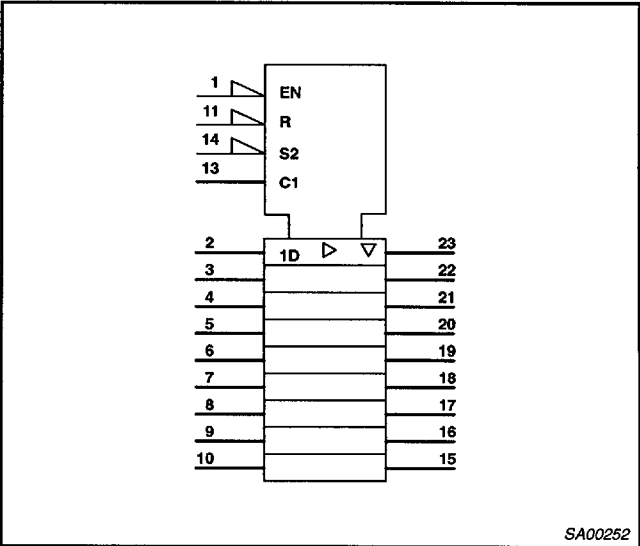
(3-State)

74ABT843

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

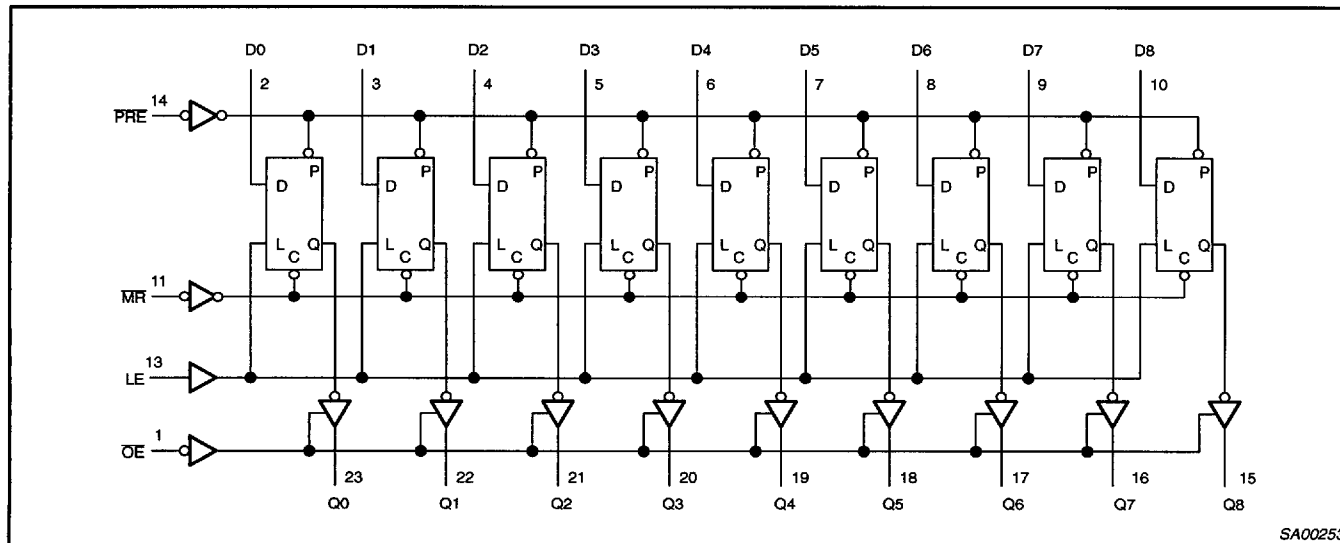
INPUTS					OUTPUTS	OPERATING MODE
OE	PRE	MR	LE	Dn	Qn	
L	L	X	X	X	H	Preset
L	H	L	X	X	L	Clear
L	H	H	H	L	L	Transparent
L	H	H	H	H	H	
L	H	H	↓	l	L	Latched
L	H	H	↓	h	H	
H	X	X	X	X	Z	High impedance
L	H	H	L	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low LE transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low LE transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low transition

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LOGIC DIAGRAM

**ABSOLUTE MAXIMUM RATINGS^{1, 2}**

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		−0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	−18	mA
V _I	DC input voltage ³		−1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	−50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	−0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		−65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C			T _{amb} = −40°C to +85°C		
			Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = −18mA		−0.9	−1.2		−1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = −32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
V _{RST}	Power-up output low voltage ³	V _{CC} = 5.5V; I _O = 1mA; V _I = V _{CC} or GND		0.13	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	μA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	μA
I _{PU} /I _{PD}	Power-up/down 3-state output current ⁴	V _{CC} = 2.0V; V _O = 0.5V; V _{OE} = V _{CC} ; V _I = GND or V _{CC}		±5.0	±50		±50	μA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		5.0	50		50	μA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		−5.0	−50		−50	μA
I _{CEX}	Output high leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	−50	−80	−180	−50	−180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		0.5	250		250	μA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		25	34		34	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		0.5	250		250	μA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		0.5	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For $V_{CC} = 2.1\text{V}$ to $V_{CC} = 5\text{V} \pm 10\%$, a transition time of up to 100 μsec is permitted.

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AC CHARACTERISTICS

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Dn to Qn	1	1.6 2.2	3.6 5.0	5.2 6.3	1.6 2.2	6.0 7.2	ns
t _{PLH} t _{PHL}	Propagation delay LE to Qn	2	2.0 2.8	4.1 4.8	5.6 6.3	2.0 2.8	6.5 6.9	ns
t _{PLH} t _{PHL}	Propagation delay PRE to Qn	1	2.2 3.0	4.7 5.2	6.2 6.5	2.2 3.0	7.4 7.2	ns
t _{PLH} t _{PHL}	Propagation delay MR to Qn	1	2.5 3.1	5.0 5.5	6.3 6.8	2.5 3.1	7.1 8.0	ns
t _{pZH} t _{pZL}	Output enable time OE to Qn	4 5	1.0 2.0	2.7 4.2	4.2 5.5	1.0 2.0	5.2 6.5	ns
t _{pHZ} t _{pLZ}	Output disable time OE to Qn	4 5	2.9 2.2	4.9 5.0	6.2 6.3	2.9 2.2	6.8 6.7	ns

AC SETUP REQUIREMENTS

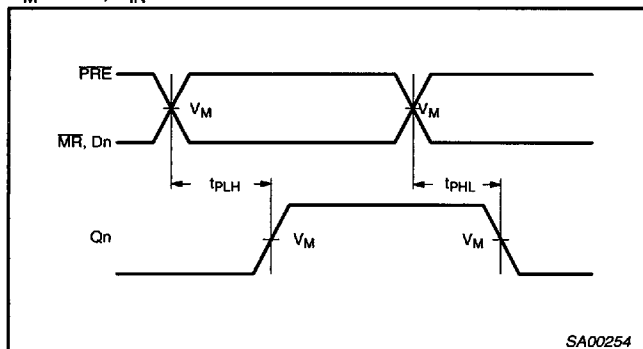
GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_{amb} = -40 \text{ to } +85^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 0.5\text{V}$	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to LE	3	2.5 3.0	1.1 1.3	2.5 3.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to LE	3	1.0 1.0	-1.0 -1.0	1.0 1.0	ns
$t_w(H)$	LE pulse width, High	3	3.3	1.8	3.3	ns
$t_w(L)$	PRE pulse width, Low	6	4.5	3.0	4.5	ns
$t_w(L)$	MR pulse width, Low	6	5.5	4.0	5.5	ns
t_{rec}	PRE recovery time	6	2.9	1.6	2.9	ns
t_{rec}	MR recovery time	6	3.6	2.0	3.6	ns

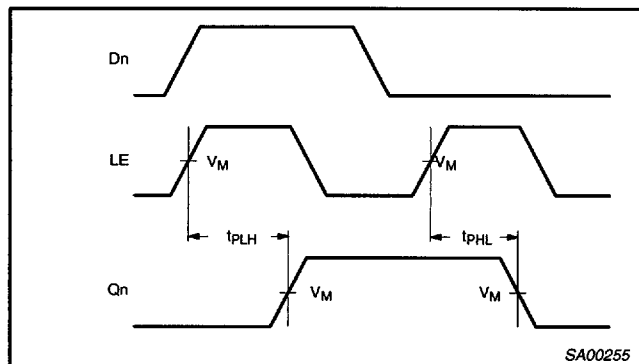
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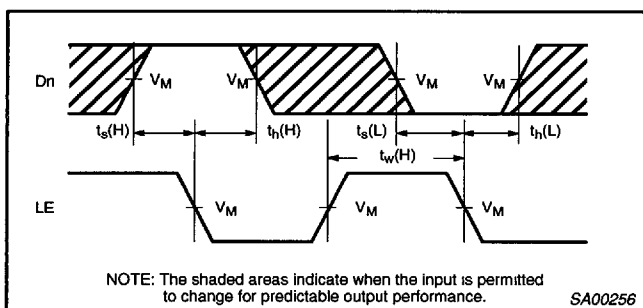
AC WAVEFORMS

 $V_M = 1.5V$, $V_{IN} = GND$ to $3.0V$


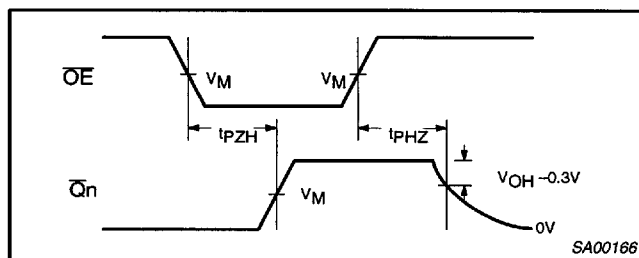
**Waveform 1. Propagation Delay, Data to Output,
Master Reset to Output, Preset to Output**



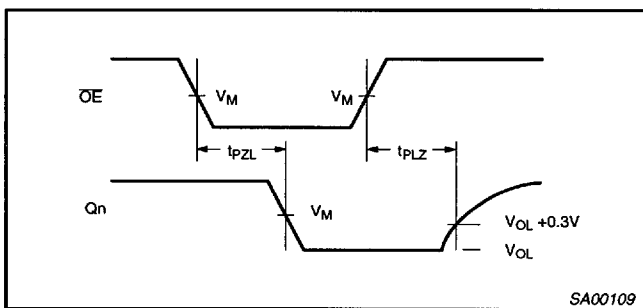
**Waveform 2. Propagation Delay, Latch Enable
to Output**



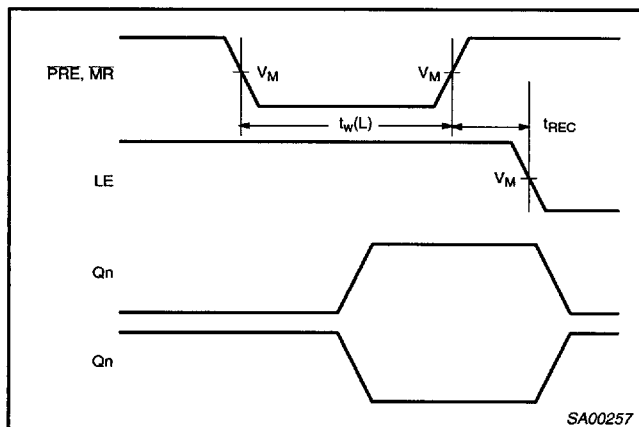
**Waveform 3. Data Setup and Hold Times and Latch Enable
Pulse Width**



**Waveform 4. 3-State Output Enable Time to High Level and
Output Disable Time from High Level**



**Waveform 5. 3-State Output Enable Time to Low Level and
Output Disable Time from Low Level**

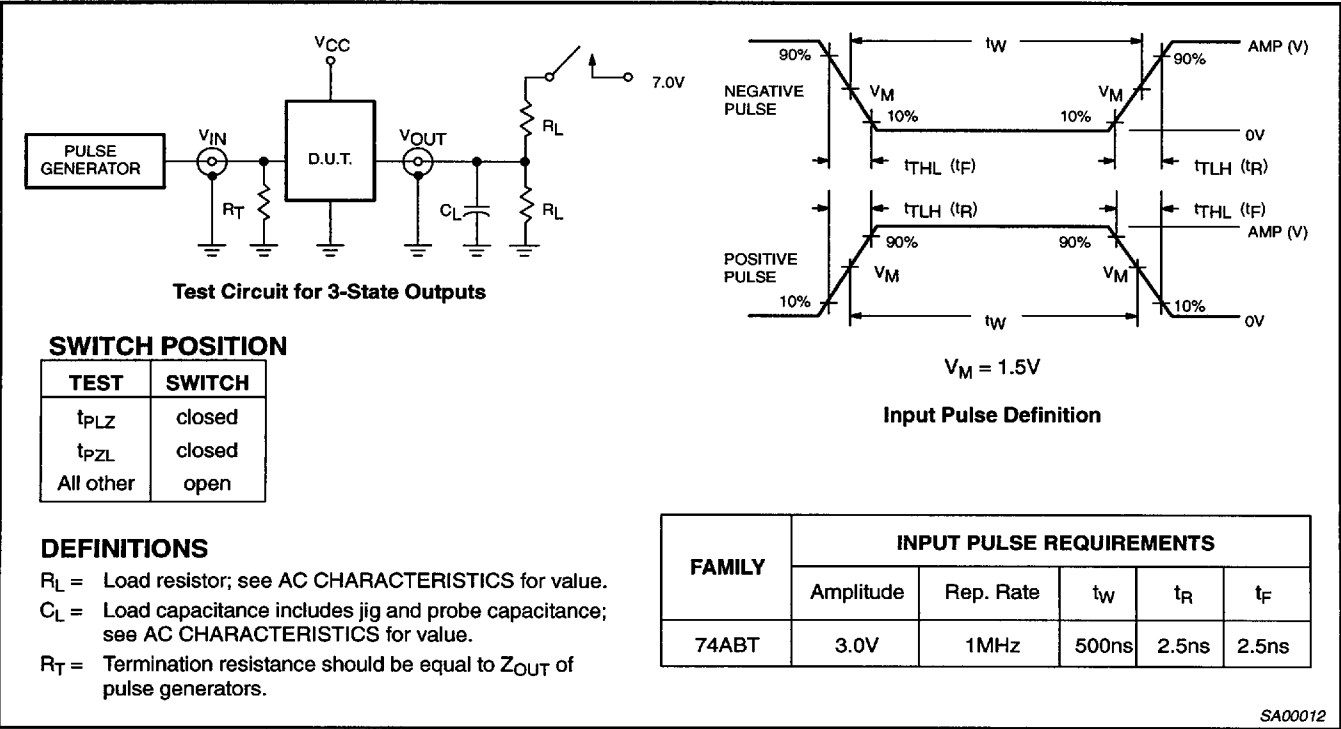


**Waveform 6. Master Reset and Preset Pulse Width,
Master Reset and Preset to Latch Enable Recovery Time**

9-bit bus interface latch with set and reset
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TEST CIRCUIT AND WAVEFORM



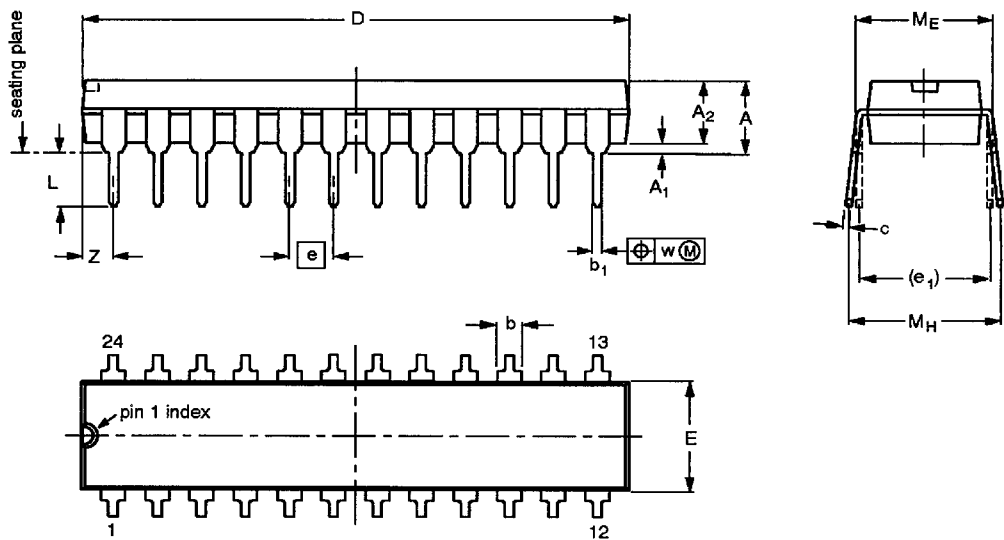
SA00012

9-bit bus interface latch with set and reset
(3-State)

74ABT843

DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

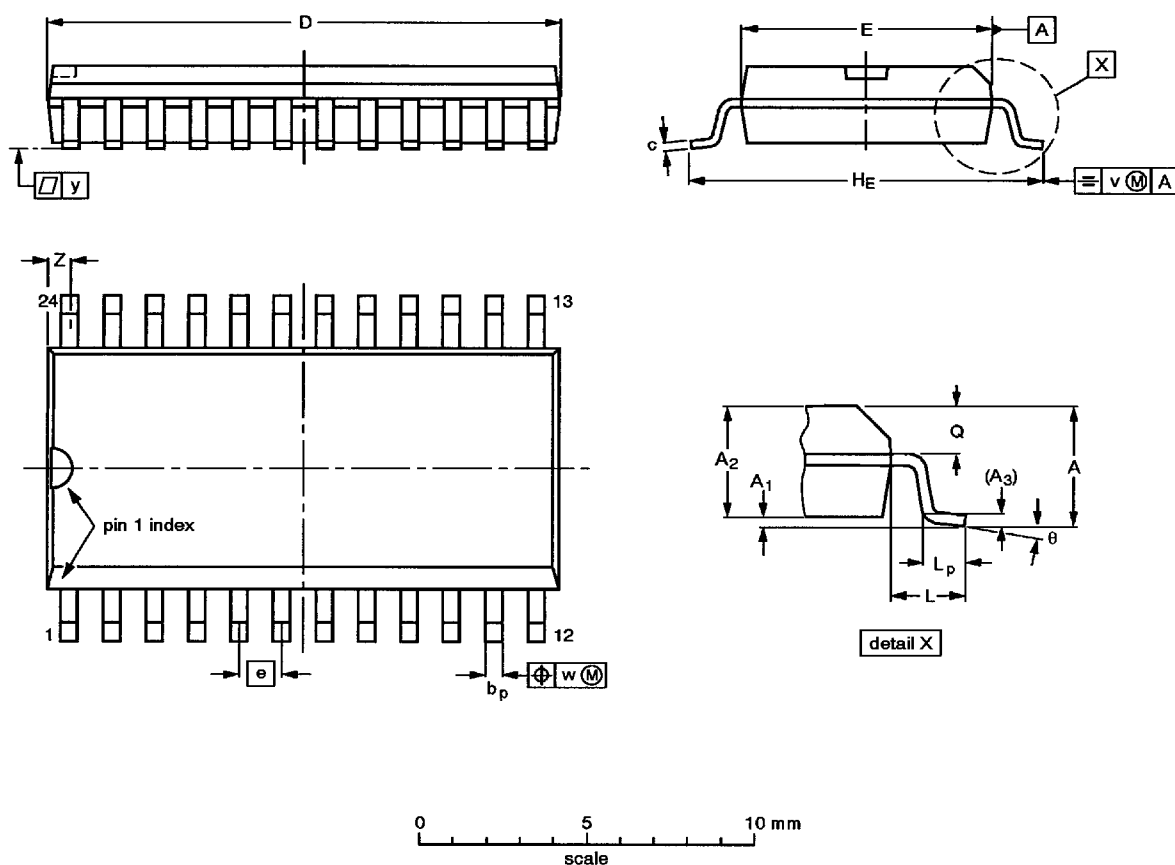
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

9-bit bus interface latch with set and reset (3-State)

74ABT843

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0'
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

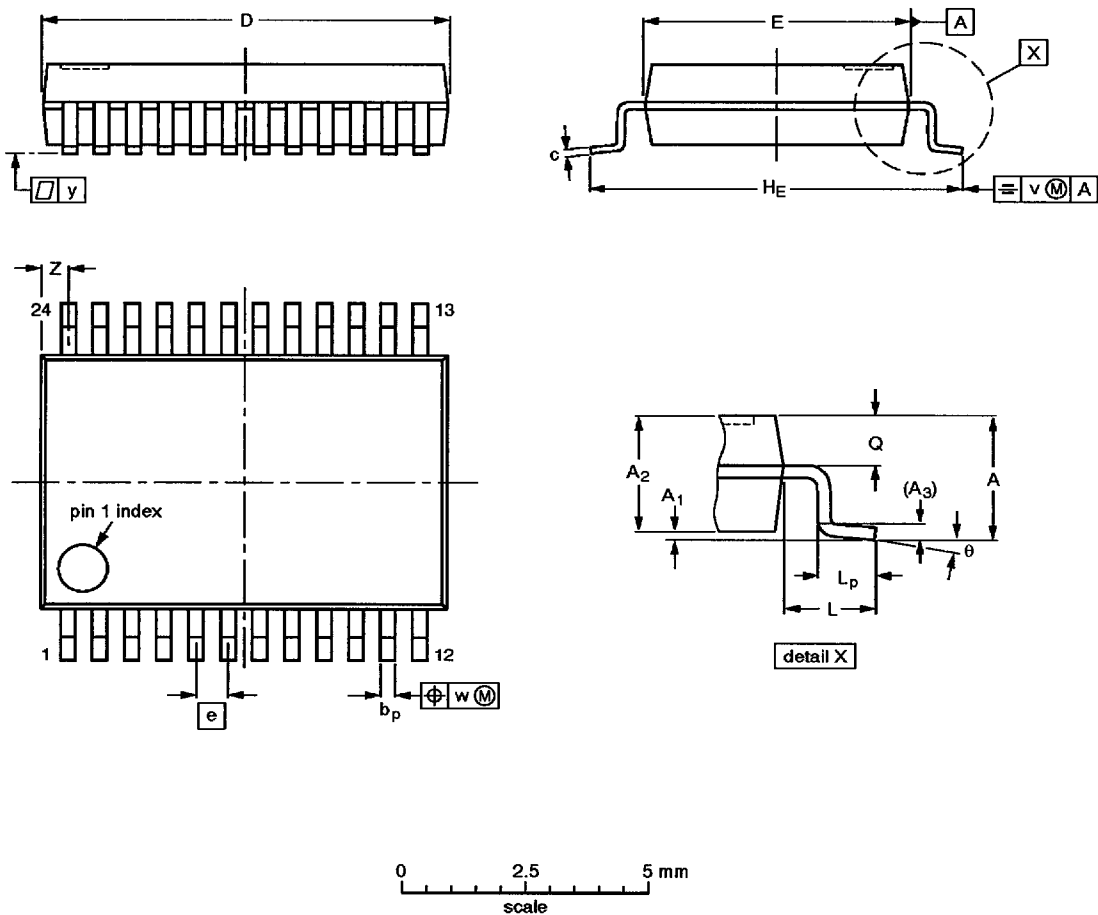
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				92-11-17 95-01-24

9-bit bus interface latch with set and reset
(3-State)

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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

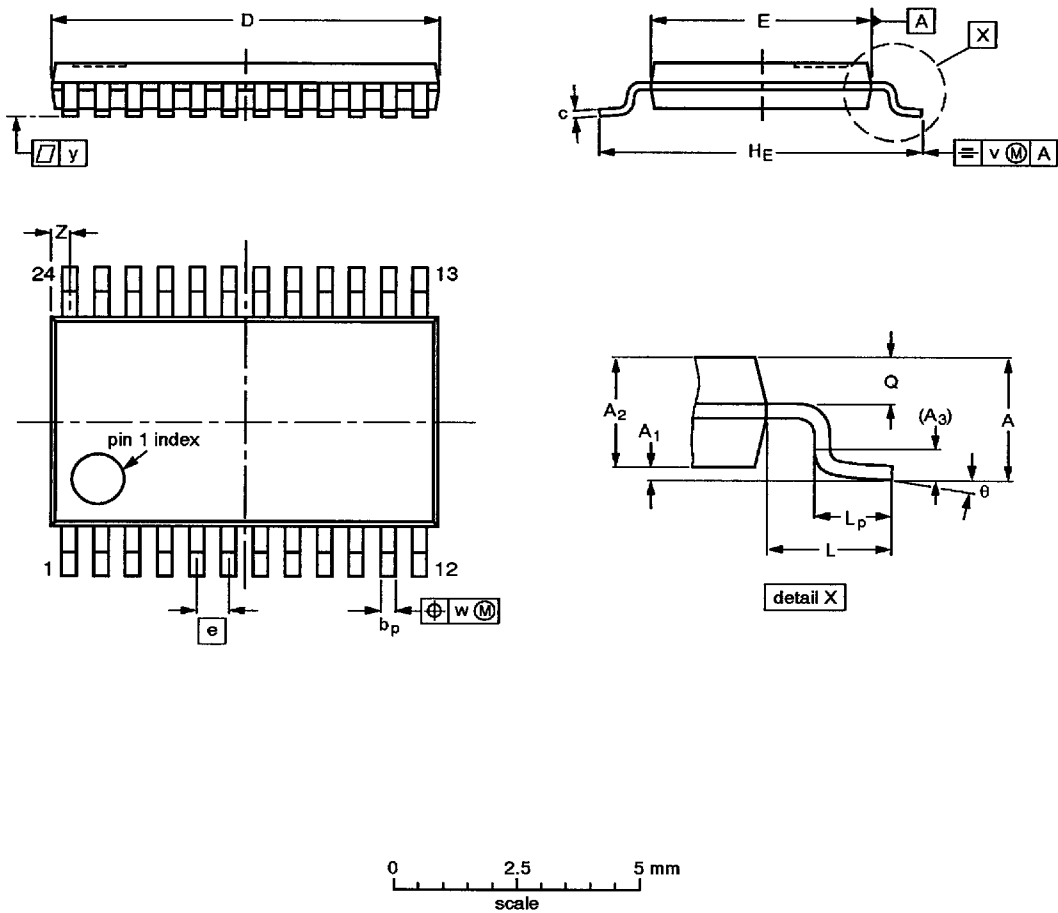
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				93-09-08 95-02-04

9-bit bus interface latch with set and reset
(3-State)

74ABT843

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				93-06-16 95-02-04