Special-Package High-Performance Surface-Mount TTL Delay Lines

GCTTLDL, GTTLDL

- Five equal taps in 20% increments of total delay.
- Lumped constant, active series.
- Transfer-molded packaging for highest reliability.
- Designed for leading edge timing. Trailing edge timing available.
- Supports Schottky TTL, FAST, and FACT logics.
- Fanout 1 -- 20 loads; logic 0 -- 10 loads.
- Temperature coefficient ±2 ns or ±4% (whichever is greater) at maximum delay, 0 to 70°C.
- Military models with temperature range -55 to +125°C and ceramic package IC to meet MIL-STD-883C, but not screened to that specification, add suffix "M" to part number.
- Military models as above, but with ceramic package IC screened to MIL-STD 883C and 38510, add suffix "MX" to part number.
- Military models as "MX" above, but with in-house burn-in and thermal shock, add suffix "MY".

GCTTLL SURFACE-MOUNT 5-TAP DELAY LINES

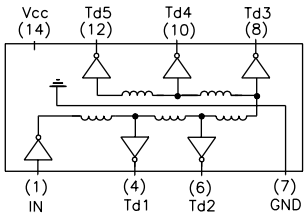
1/8" HEIGHT

TECHNITROL PART NO.	TAP DELAYS (ns)					ALL TAPS	
	T_D1	T_D2	T_D3	T_D4	T_D5	T_{RO}	T_{FO}
GCTTLDL025AMX	5.0	10.0	15.0	20.0	25.0	2.0	2.0
GCTTLDL050AMX	10.0	20.0	30.0	40.0	50.0	2.0	2.0
GCTTLDL075AMX	15.0	30.0	45.0	60.0	75.0	2.0	2.0
GCTTLDL100AMX	20.0	40.0	60.0	80.0	100.0	2.0	5.0
GCTTLDL125AMX	25.0	50.0	75.0	100.0	125.0	2.0	6.0
GCTTLDL150AMX	30.00	60.0	90.0	120.0	150.0	2.0	7.0
GCTTLDL200AMX	40.00	80.0	120.0	160.0	200.0	2.0	8.0

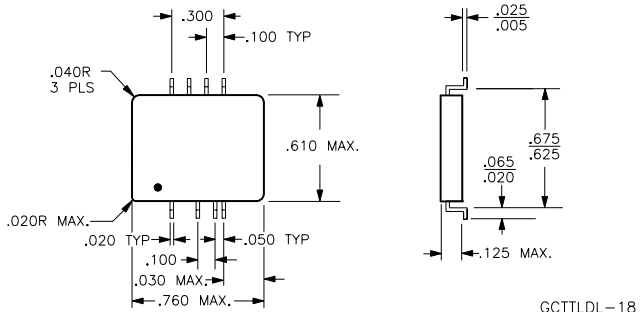
For TTL delay lines qualified to MIL-D-83532, refer to PSC information sheet entitled "QPL Active Delay Lines."

Delay Characteristics measured at V_{CC} = 5.0V, 25°C, no load.
Delay Tolerance ±2 ns or 5%, whichever is greater.
Rise time measured @ 0.8V to 2.0V levels.
For minimum input pulse width -- contact factory.

SCHEMATIC



MECHANICAL OUTLINE



Notes

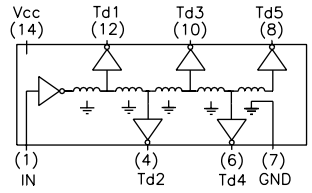
- Pin numbers shown are for reference only and are not necessarily marked on unit.
- Only the pins specified in the schematics are provided with each package.
- Lead material is electro tin plated (alloy 42) or solder dipped.
- All specifications are subject to change without notice.

GTTL SURFACE-MOUNT 5-TAP DELAY LINES

TECHNITROL PART NO.	TAP DELAYS (ns)					ALL TAPS	
	T_D1	T_D2	T_D3	T_D4	T_D5	T_{RO}	T_{FO}
GTTLDL025MX	5.0	10.0	15.0	20.0	25.0	2.0	2.0
GTTLDL050MX	10.0	20.0	30.0	40.0	50.0	2.0	2.0
GTTLDL075MX	15.0	30.0	45.0	60.0	75.0	2.0	2.0
GTTLDL100MX	20.0	40.0	60.0	80.0	100.0	2.0	2.0
GTTLDL125MX	25.0	50.0	75.0	100.0	125.0	2.0	2.0
GTTLDL150MX	30.00	60.0	90.0	120.0	150.0	2.0	5.0
GTTLDL200MX	40.00	80.0	120.0	160.0	200.0	2.0	5.0
GTTLDL250MX	50.00	100.0	150.0	200.0	250.0	2.0	9.0
GTTLDL500MX	100.00	200.0	300.0	400.0	500.0	2.0	9.0

Delay Characteristics measured at V_{CC} = 5.0V, 25°C, no load.
Delay Tolerance ±2 ns or 5%, whichever is greater.
Rise time measured @ 0.8V to 2.0V levels.
For minimum input pulse width -- contact factory.

SCHEMATIC



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MECHANICAL OUTLINE