

DS26401DK

Octal T1/E1/J1 Framer Design Kit

Daughter Card

www.maxim-ic.com

GENERAL DESCRIPTION

The DS26401DK is an easy-to-use evaluation board for the DS26401 octal T1/E1/J1 framer. It is intended to be used as a daughter card with the DK101 motherboard or the DK2000 motherboard. The DS26401DK comes complete with a DS26401 octal framer, two DS21448 quad LIUs, transformers, termination resistors, network connectors, and motherboard connectors. The DK101/DK2000 motherboard and the Dallas' ChipView software give point-and-click access to configurations and status registers from a Windows®-based PC. On-board LEDs indicate loss-of-signal, loss-of-frame, and interrupt status.

Each DS26401DK is shipped with a free DK101 motherboard. For complex applications, the DK2000 high-performance demo kit motherboard can be purchased separately.

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DESIGN KIT CONTENTS

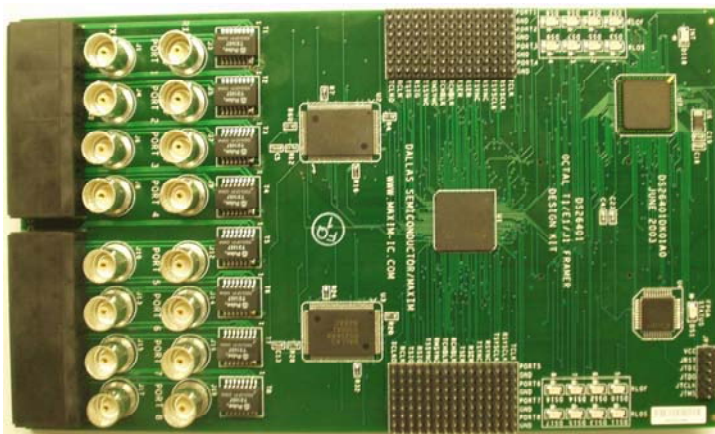
DS26401DK Board
 DK101 Low-Cost Motherboard
 CD-ROM
 ChipView Software
 DS26401DK Data Sheet
 DK101 Data Sheet
 DS26401 Data Sheet
 DS21448 Data Sheet
 DS26401 Errata Sheet
 DS21448 Errata Sheet

FEATURES

- Demonstrates Key Functions of the DS26401 Octal T1/E1/J1 Framer
- Includes Two DS21448 Quad LIUs, Transformers, BNC and RJ45 Connectors, and Termination Passives
- Compatible with DK101 and DK2000 Demo Kit Motherboards
- DK101/DK2000 and ChipView Software Provide Point-and-Click Access to the DS26401 Register Set
- All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink
- Memory-Mapped FPGA Provides Flexible Clock/Data/Sync Connections Among Framer Ports and DK2000 Motherboard
- LEDs for Loss-of-Signal, Loss-of-Frame, and Interrupt
- Easy-to-Read Silk-Screen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs

ORDERING INFORMATION

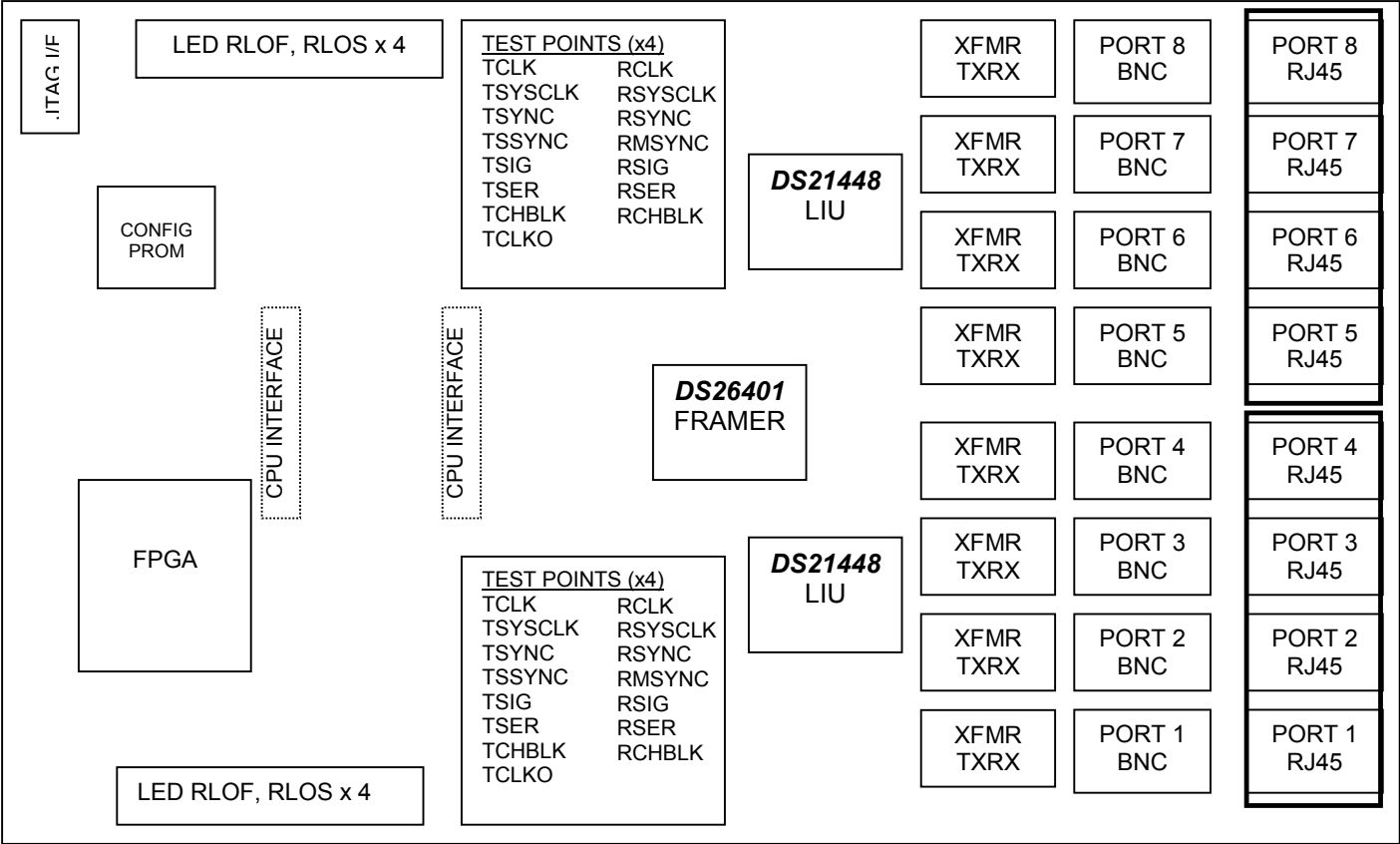
PART	DESCRIPTION
DS26401DK	DS26401 Demo Kit Daughter Card (with included DK101 motherboard)



COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1, C3, C5, C7, C9, C11, C13, C15, C17–C24, C26, C28–C31, C35–C42	29	00.1 μ F 20%, 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
C2, C4, C6, C8, C10, C12, C14, C16	8	1 μ F 10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
DS1, DS18	2	LED, green, SMD	Panasonic	LN1351C
DS2–DS17	16	LED, red, SMD	Panasonic	LN1251C
J1, J3–J10, J12–J18	16	5-pin connectors, 75 Ω BNC vertical	Bourns	CP-BNCPC-004
J2, J11	2	Right-angle, RJ45 8-pin 4-port jack	3M Electronics	43223-8140
J19, J20	2	50-pin headers, socket, SMD dual row, vertical	Samtec	TFM-125-02-S-D-LC
J21, J23, J25, J27, J29, J31, J33, J35	8	20-pin headers, dual row, vertical	Samtec	HDR-TSW-110-14-T-D
J22, J24, J26, J28, J30, J32, J34, J36	8	10-pin headers, dual row, vertical	Murrietta	N/A
JP1	1	12-pin connector, dual row, vertical	Murrietta	N/A
R1, R2, R5, R6, R9, R10, R13, R14, R17, R18, R21, R22, R25, R26, R29, R30, R67	17	0 Ω 1%, 1/16W resistors (0603)	AVX	CJ10-000F
R3, R4, R7, R8, R11, R12, R15, R16, R19, R20, R23, R24, R27, R28, R31, R32	16	60.4 Ω 1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF60R4V
R33–R35	3	10k Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
R36, R37, R68	3	330 Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ331V
R38, R59–R66	9	30.1 Ω 1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF30R1V
R39–R54	16	300 Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ301V
R55–R58	4	10.0k Ω 1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF1002V
T1–T8	8	XFMR, dual, 16-pin SMT	Pulse Engineering	TX1467
U1	1	Octal T1/E1/J1 framer	Dallas Semiconductor	DS26401
U2, U3	2	3.3V E1/T1/J1 quad LIU 128-pin LQFP, 0°C to +70°C	Dallas Semiconductor	DS21448L
U4	1	1M PROM for FPGA 44-pin TQFP	Xilinx	XC18V01VQ44C_U
U6	1	8-pin μ MAX/SO 2.5V or Adj	Maxim	MAX1792EUA25
U7	1	XILINX Spartan 2.5V FPGA, 256-pin BGA	Xilinx	XC2S50-5FG256C

BOARD FLOORPLAN



QUICK SETUP (REGISTER VIEW)

- Connect DS26401DK to DK101 motherboard.
- Connect serial cable to a PC and DK101.
- Power DK101 with 3.3V.
- Load ChipView software.
- Select COM port.
- Select Register View.
- For T1 applications, load the *401_global_t1_DS26401DC.def* file. For E1 applications, load the *401_global_e1_DS26401DC.def* file.
- Make sure that all the register settings are correct for the proper function desired for the DS26401DK.

Please refer to the DS26401 data sheet (www.maxim-ic.com/DS26401) and the DS21448 data sheet (www.maxim-ic.com/DS21448) for all questions pertaining to device functionality.

ADDRESS MAP

DK101 daughter card address space begins at 0x81000000.

DK2000 daughter card address space begins at:

0x30000000 for slot 0

0x40000000 for slot 1

0x50000000 for slot 2

0x60000000 for slot 3

All offsets given below are relative to the beginning of the daughter card address space.

Table 1. Daughter Card Address Map

SPAN NUMBER	OFFSET		
	DS26401	DS21448	FPGA
1	0x1000	0x2000	0x10
2	0x1200	0x3000	0x20
3	0x1400	0x4000	0x30
4	0x1600	0x5000	0x40
5	0x1800	0x6000	0x50
6	0x1A00	0x7000	0x60
7	0x1C00	0x8000	0x70
8	0x1E00	0x9000	0x80

Registers in the FPGA can be easily modified using ChipView.exe host-based user-interface software along with the definition file named *DS26401DC_FPGA.def*.

FPGA REGISTER MAP

Table 2. FPGA Register map

OFFSET	NAME	TYPE	DESCRIPTION
0X0000	BID	Read-Only	Board ID
0X0002	XBIDH	Read-Only	High Nibble Extended Board ID
0X0003	XBIDM	Read-Only	Middle Nibble Extended Board ID
0X0004	XBIDL	Read-Only	Low Nibble Extended Board ID
0X0005	BREV	Read-Only	Board FAB Revision
0X0006	AREV	Read-Only	Board Assembly Revision
0X0007	PREV	Read-Only	PLD Revision
0X0010 0x0020 0x0030 0x0040 0x0050 0x0060 0x0070 0x0080	TSIG_SR –1 TSIG_SR –2 TSIG_SR –3 TSIG_SR –4 TSIG_SR –5 TSIG_SR –6 TSIG_SR –7 TSIG_SR –8	Control	DS26401 TSIG Pin Setting Port 1 DS26401 TSIG Pin Setting Port 2 DS26401 TSIG Pin Setting Port 3 DS26401 TSIG Pin Setting Port 4 DS26401 TSIG Pin Setting Port 5 DS26401 TSIG Pin Setting Port 6 DS26401 TSIG Pin Setting Port 7 DS26401 TSIG Pin Setting Port 8
0X0011 0X0021 0X0031 0X0041 0x0051 0x0061 0x0071 0x0081	TSER_SR –1 TSER_SR –2 TSER_SR –3 TSER_SR –4 TSER_SR –5 TSER_SR –6 TSER_SR –7 TSER_SR –8	Control	DS26401 TSER Pin Setting Port 1 DS26401 TSER Pin Setting Port 2 DS26401 TSER Pin Setting Port 3 DS26401 TSER Pin Setting Port 4 DS26401 TSER Pin Setting Port 5 DS26401 TSER Pin Setting Port 6 DS26401 TSER Pin Setting Port 7 DS26401 TSER Pin Setting Port 8
0X0012 0X0022 0X0032 0X0042 0X0052 0X0062 0X0072 0X0082	TSSYNC_SR –1 TSSYNC_SR –2 TSSYNC_SR –3 TSSYNC_SR –4 TSSYNC_SR –5 TSSYNC_SR –6 TSSYNC_SR –7 TSSYNC_SR –8	Control	DS26401 TSSYNC Source Port 1 DS26401 TSSYNC Source Port 2 DS26401 TSSYNC Source Port 3 DS26401 TSSYNC Source Port 4 DS26401 TSSYNC Source Port 5 DS26401 TSSYNC Source Port 6 DS26401 TSSYNC Source Port 7 DS26401 TSSYNC Source Port 8
0X0013 0X0023 0X0033 0X0043 0X0053 0X0063 0X0073 0X0083	TSYSCLK –1 TSYSCLK –2 TSYSCLK –3 TSYSCLK –4 TSYSCLK –5 TSYSCLK –6 TSYSCLK –7 TSYSCLK –8	Control	DS26401 TSYSCLK Source Port 1 DS26401 TSYSCLK Source Port 2 DS26401 TSYSCLK Source Port 3 DS26401 TSYSCLK Source Port 4 DS26401 TSYSCLK Source Port 5 DS26401 TSYSCLK Source Port 6 DS26401 TSYSCLK Source Port 7 DS26401 TSYSCLK Source Port 8
0X0014 0X0024 0X0034 0X0044 0X0054 0X0064 0X0074 0X0084	RSYSCLK –1 RSYSCLK –2 RSYSCLK –3 RSYSCLK –4 RSYSCLK –5 RSYSCLK –6 RSYSCLK –7 RSYSCLK –8	Control	DS26401 RSYSCLK Source Port 1 DS26401 RSYSCLK Source Port 2 DS26401 RSYSCLK Source Port 3 DS26401 RSYSCLK Source Port 4 DS26401 RSYSCLK Source Port 5 DS26401 RSYSCLK Source Port 6 DS26401 RSYSCLK Source Port 7 DS26401 RSYSCLK Source Port 8

Table 2. Register Map (continued)

OFFSET	NAME	TYPE	DESCRIPTION
0X0015	TCLK –1	Control	DS26401TCLK Source Port 1
0X0025	TCLK –2		DS26401TCLK Source Port 2
0X0035	TCLK –3		DS26401TCLK Source Port 3
0X0045	TCLK –4		DS26401TCLK Source Port 4
0X0055	TCLK –5		DS26401TCLK Source Port 5
0X0065	TCLK –6		DS26401TCLK Source Port 6
0X0075	TCLK –7		DS26401TCLK Source Port 7
0X0085	TCLK –8		DS26401TCLK Source Port 8
0X0016	RSYNC –1	Control	DS26401RSYNC Source Port 1
0X0026	RSYNC –2		DS26401RSYNC Source Port 2
0X0036	RSYNC –3		DS26401RSYNC Source Port 3
0X0046	RSYNC –4		DS26401RSYNC Source Port 4
0X0056	RSYNC –5		DS26401RSYNC Source Port 5
0X0066	RSYNC –6		DS26401RSYNC Source Port 6
0X0076	RSYNC –7		DS26401RSYNC Source Port 7
0X0086	RSYNC –8		DS26401RSYNC Source Port 8
0X0017	TSYNC –1	Control	DS26401TSYNC Source Port 1
0X0027	TSYNC –2		DS26401TSYNC Source Port 2
0X0037	TSYNC –3		DS26401TSYNC Source Port 3
0X0047	TSYNC –4		DS26401TSYNC Source Port 4
0X0057	TSYNC –5		DS26401TSYNC Source Port 5
0X0067	TSYNC –6		DS26401TSYNC Source Port 6
0X0077	TSYNC –7		DS26401TSYNC Source Port 7
0X0087	TSYNC –8		DS26401TSYNC Source Port 8
0X0090	CLK	Control	LIU MCLK and REF CLK Source

ID Registers**BID: BOARD ID (Offset = 0X0000)**

BID is read-only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0X0002)

XBIDH is read-only with a value of 0x0.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0X0003)

XBIDM is read-only with a value of 0x1.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0X0004)

XBIDL is read-only with a value of 0x6.

BREV: BOARD FAB REVISION (Offset = 0X0005)

BREV is read-only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset = 0X0006)

AREV is read-only and displays the current assembly revision.

PREV: PLD REVISION (Offset = 0X0007)

PREV is read-only and displays the current PLD firmware revision.

Control Registers

Register Name: **TSIG_SR**

Register Description: **DS26401 TSIG x Pin Setting**

Register Offset: **0x0010, 0x0020, 0x0030, 0x0040, 0x0050, 0x0060, 0x0070, 0x0080**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bit 0 to 7: DS26401 Port x TSIG Source (D7, D6, D5, D4, D3, D2, D1, D0)

The source for TSER is Defined as shown in Table 3.

Table 3. TSERx Source Definition

D3, D2, D1, D0	TSIG CONNECTION
0000	Tri-state TSIG
0001	Drive TSIG with RSIG1
0010	Drive TSIG with RSIG2
0011	Drive TSIG with RSIG3
0100	Drive TSIG with RSIG4
0101	Drive TSIG with RSIG5
0110	Drive TSIG with RSIG6
0111	Drive TSIG with RSIG7
1000	Drive TSIG with RSIG8
1010	Drive TSIG with T1 OSC
1011	Drive TSIG with E1 OSC
1100	Drive TSIG with 16.384MHz
1101	Drive TSIG with a logic 0
1110	Drive TSIG with a logic 1
1111	Tri-state TSIG

Note: Initial values are such that all values are tri-stated.

Register Name: **TSER_SR**

Register Description: **DS26401 TSERx Pin Setting**

Register Offset: **0x0011, 0x0021, 0x0031, 0x0041, 0x0051, 0x0061, 0x0071, 0x0081**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

Bit 0 to 3: DS26401 Port x TSER Source (D3, D2, D1, D0)

The source for TSER is Defined as shown in Table 4.

Table 4. TSERx Source Definition

D3, D2, D1, D0	TSER CONNECTION
0000	Tri-state TSER
0001	Drive TSER with RSER1
0010	Drive TSER with RSER2
0011	Drive TSER with RSER3
0100	Drive TSER with RSER4
0101	Drive TSER with RSER5
0110	Drive TSER with RSER6
0111	Drive TSER with RSER7
1000	Drive TSER with RSER8
1010	Drive TSER with T1 OSC
1011	Drive TSER with E1 OSC
1100	Drive TSER with 16.384MHz
1101	Drive TSER with a logic 0
1110	Drive TSER with a logic 1
1111	Tri-state TSER

Note: Initial values are such that all ports are tri-stated.

Register Name: **TSSYNC_SR**

Register Description: **DS26401 TSSYNCx Pin Setting**

Register Offset: **0x0012, 0x0022, 0x0032, 0x0042, 0x0052, 0x0062, 0x0072, 0x0082**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0
Default	0	0	0	0	0	1	0	1

Bit 0 to 2: DS26401 Port x TSSYNC Source (D3, D2, D1, D0)

The source for TSSYNC is Defined as shown in Table 5.

Table 5. TSSYNCx Source Definition

D3, D2, D1, D0	TSSYNC CONNECTION
0000	Tri-state TSSYNC
0001	Drive TSSYNC with RMSYNC1
0010	Drive TSSYNC with RMSYNC2
0011	Drive TSSYNC with RMSYNC3
0100	Drive TSSYNC with RMSYNC4
0101	Drive TSSYNC with RMSYNC5
0110	Drive TSSYNC with RMSYNC6
0111	Drive TSSYNC with RMSYNC7
1000	Drive TSSYNC with RMSYNC8
1010	Drive TSSYNC with T1 OSC
1011	Drive TSSYNC with E1 OSC
1100	Drive TSSYNC with 16.385MHz
1101	Drive TSSYNC with a logic 0
1110	Drive TSSYNC with a logic 1
1111	Tri-state TSSYNC

Note: Initial values are such that all ports are tri-stated.

Register Name: **TSYSCLK_SR**

Register Description: **DS26401 TSYSCLKx Pin Setting**

Register Offset: **0x0013, 0x0023, 0x0033, 0x0043, 0x0053, 0x0063, 0x0073, 0x0083**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

Bit 0 to 2: DS26401 Port x TSYSCLKC Source (D3, D2, D1, D0)

The source for TSYSCLK is Defined as shown in Table 6.

Table 6. TSYSCLKx Source Definition

D3, D2, D1, D0	TSYSCLK CONNECTION
0000	Tri-state TSYSCLK
0001	Drive TSYSCLK with RCHBLK 1
0010	Drive TSYSCLK with RCHBLK 2
0011	Drive TSYSCLK with RCHBLK 3
0100	Drive TSYSCLK with RCHBLK 4
0101	Drive TSYSCLK with RCHBLK 5
0110	Drive TSYSCLK with RCHBLK 6
0111	Drive TSYSCLK with RCHBLK 7
1000	Drive TSYSCLK with RCHBLK 8
1001	BPCLK
1010	Drive TSYSCLK with T1 OSC
1011	Drive TSYSCLK with E1 OSC
1100	Drive TSYSCLK with 16.385MHz
1101	Drive TSYSCLK with a logic 0
1110	Drive TSYSCLK with a logic 1
1111	Tri-state TSYSCLK

Note: Initial values are such that all ports are tri-stated.

Register Name: **RSYSCLK_SR**

Register Description: **DS26401 RSYSCLKx Pin Setting**

Register Offset: **0x0014, 0x0024, 0x0034, 0x0044, 0x0054, 0x0064, 0x0074, 0x0084**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

Bit 0 to 2: DS26401 Port x RSYSCLKC Source (D3, D2, D1, D0)

The source for RSYSCLK is Defined as shown in Table 7.

Table 7. RSYSCLKx Source Definition

D3, D2, D1, D0	RSYSCLK CONNECTION
0000	Tri-state RSYSCLK
0001	Drive RSYSCLK with TCHBLK 1
0010	Drive RSYSCLK with TCHBLK 2
0011	Drive RSYSCLK with TCHBLK 3
0100	Drive RSYSCLK with TCHBLK 4
0101	Drive RSYSCLK with TCHBLK 5
0110	Drive RSYSCLK with TCHBLK 6
0111	Drive RSYSCLK with TCHBLK 7
1000	Drive RSYSCLK with TCHBLK 8
1001	BPCLK
1010	Drive RSYSCLK with T1 OSC
1011	Drive RSYSCLK with E1 OSC
1100	Drive RSYSCLK with 16.385MHz
1101	Drive RSYSCLK with a logic 0
1110	Drive RSYSCLK with a logic 1
1111	Tri-state RSYSCLK

Note: Initial values are such that all ports are tri-stated.

Register Name: **TCLK_SR**

Register Description: **DS26401 TCLKx Pin Setting**

Register Offset: **0x0015, 0x0025, 0x0035, 0x0045, 0x0055, 0x0065, 0x0075, 0x0085**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

Bit 0 to 2: DS26401 Port x TCLK Source (D3, D2, D1, D0)

The source for TCLK is Defined as shown in Table 8.

Table 8. TCLKx Source Definition

D3, D2, D1, D0	TCLK CONNECTION
0000	Tri-state TCLK
0001	Drive TCLK with TCLK 1
0010	Drive TCLK with TCLK 2
0011	Drive TCLK with TCLK 3
0100	Drive TCLK with TCLK 4
0101	Drive TCLK with TCLK 5
0110	Drive TCLK with TCLK 6
0111	Drive TCLK with TCLK 7
1000	Drive TCLK with TCLK 8
1010	Drive TCLK with T1 OSC
1011	Drive TCLK with E1 OSC
1100	Drive TCLK with 16.385MHz
1101	Drive TCLK with a logic 0
1110	Drive TCLK with a logic 1
1111	Tri-state TCLK

Note: Initial values are such that all ports are tri-stated.

Also note that RCLK from the LIU (DS21448) does not go directly to the FPGA. However, it is routed to the DS26401 and a test header. To get RCLK to fan out to all the ports on the DS26401, simply tri-state a port on the FPGA and manually jumper the RCLK X pin to the TCLK X pin. Then you can route that signal with register values 0001 to 1000 in the TCLK_SR.

Register Name: **RSYNC_SR**

Register Description: **DS26401 RSYNCx Pin Setting**

Register Offset: **0x0016, 0x0026, 0x0036, 0x0046, 0x0056, 0x0066, 0x0076, 0x0086**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

Bit 0 to 2: DS26401 Port x RSYNC Source (D3, D2, D1, D0)

The source for RSYNC is Defined as shown in Table 9.

Table 9. RSYNCx Source Definition

D3, D2, D1, D0	RSYNC CONNECTION
0000	Tri-state RSYNC
0001	Drive RSYNC with TSYNC 1
0010	Drive RSYNC with TSYNC 2
0011	Drive RSYNC with TSYNC 3
0100	Drive RSYNC with TSYNC 4
0101	Drive RSYNC with TSYNC 5
0110	Drive RSYNC with TSYNC 6
0111	Drive RSYNC with TSYNC 7
1000	Drive RSYNC with TSYNC 8
1010	Drive RSYNC with T1 OSC
1011	Drive RSYNC with E1 OSC
1100	Drive RSYNC with 16.385MHz
1101	Drive RSYNC with a logic 0
1110	Drive RSYNC with a logic 1
1111	Tri-state RSYNC

Note: Initial values are such that all ports are tri-stated.

Register Name: **TSYNC_SR**

Register Description: **DS26401 TSYNCx Pin Setting**

Register Offset: **0x0017, 0x0027, 0x0037, 0x0047, 0x0057, 0x0067, 0x0077, 0x0087**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	D4	D3	D2	D1	D0

Bit 0 to 2: DS26401 Port x TSYNC Source (D4, D3, D2, D1, D0)

The source for TSYNC is Defined as shown in Table 10.

Table 10. TSYNCx Source Definition

D4, D3, D2, D1, D0	TSYNC CONNECTION
00000	Tri-state TSYNC
00001	Drive TSYNC with RSYNC 1
00010	Drive TSYNC with RSYNC 2
00011	Drive TSYNC with RSYNC 3
00100	Drive TSYNC with RSYNC 4
00101	Drive TSYNC with RSYNC 5
00110	Drive TSYNC with RSYNC 6
00111	Drive TSYNC with RSYNC 7
01000	Drive TSYNC with RSYNC 8
01010	Drive TSYNC with T1 OSC
01011	Drive TSYNC with E1 OSC
01100	Drive TSYNC with 16.385MHz
01101	Drive TSYNC with a logic 0
01110	Drive TSYNC with a logic 1
10001	Drive TSYNC with RMSYNC 1
10010	Drive TSYNC with RMSYNC 2
10011	Drive TSYNC with RMSYNC 3
10100	Drive TSYNC with RMSYNC 4
10101	Drive TSYNC with RMSYNC 5
10110	Drive TSYNC with RMSYNC 6
10111	Drive TSYNC with RMSYNC 7
11000	Drive TSYNC with RMSYNC 8
11111	Tri-state TSYNC

Note: Initial values are such that all ports are tri-stated.

Register Name: **CLK_SR**Register Description: **DS21448 MCLK A, DS21448 MCLK B, and REF CLK**Register Offset: **0x0090**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Table 11. MCLK A Source Definition

D1, D0	MCLK A (DS21448 PORTS 1 TO 4)
00	Tri-state MCLK
01	Drive MCLK with 1.544MHz
10	Drive MCLK with 2.048MHz
11	Tri-state MCLK

Note: Initial values are such that MCLK is 2.048MHz.**Table 12. MCLK B Source Definition**

D3, D2	MCLK B (DS21448 PORTS 5 TO 8)
00	Tri-state MCLK
01	Drive MCLK with 1.544MHz
10	Drive MCLK with 2.048MHz
11	Tri-state MCLK

Note: Initial values are such that that MCLK is 2.048MHz.**Table 13. MCLK A Source Definition**

D5, D4	REF CLK
00	Tri-state REF CLK
01	Drive REF with 1.544MHz
10	Drive REF with 2.048MHz
11	Tri-state REF CLK

Note: Initial values are such that REF is 2.048MHz.

DS26401 AND DS21448 INFORMATION

For more information about the DS26401 and DS21448, please consult the respective data sheets, available on our website at www.maxim-ic.com/DS26401 and www.maxim-ic.com/DS21448.

TECHNICAL SUPPORT

For technical support, please email your questions to telecom.support@dalsemi.com.

SCHEMATICS

The DS26401DK schematics are featured in the following pages.

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DS26401 DESIGN KIT

CREATED BY

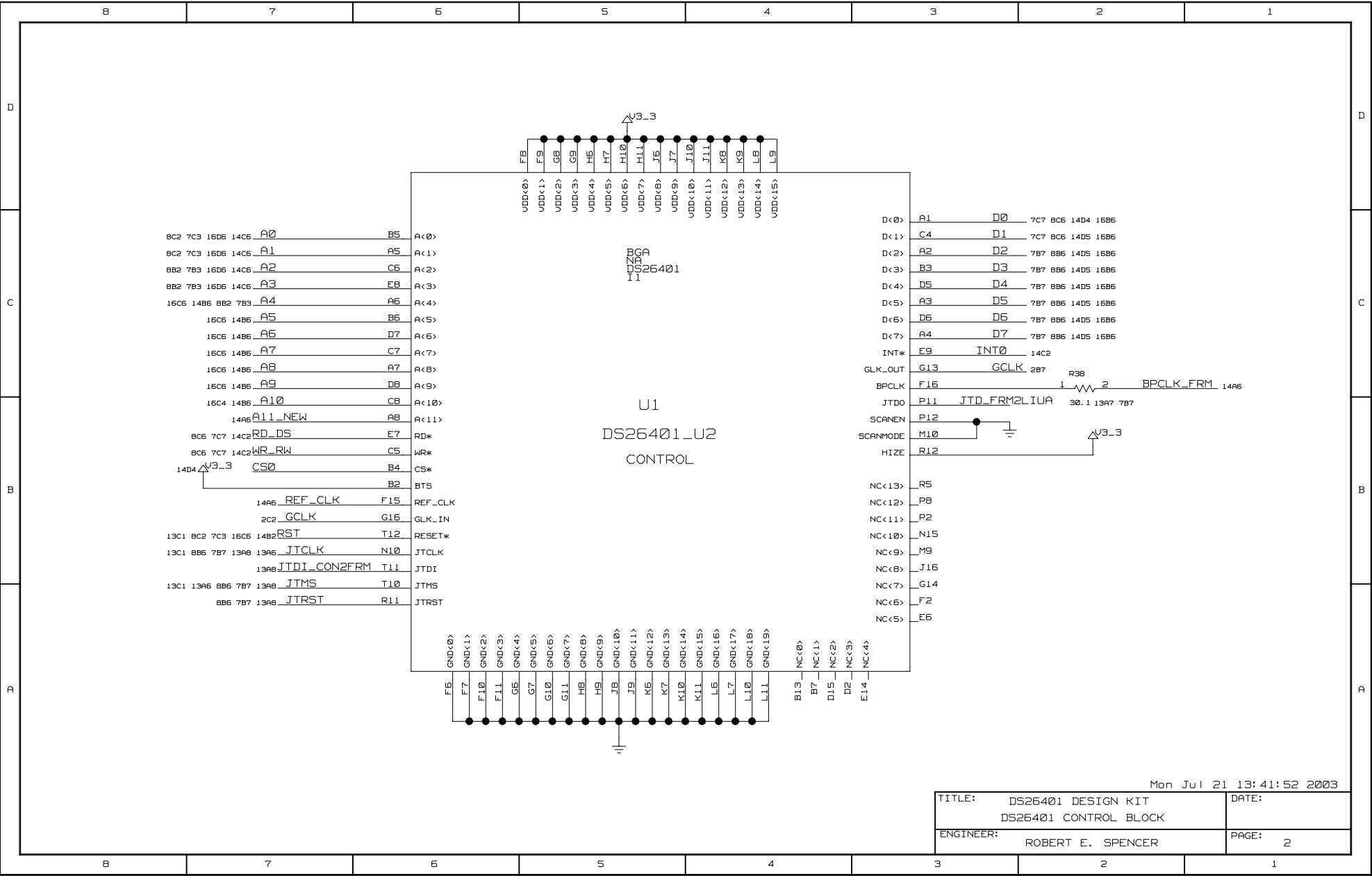
ROBERT E. SPENCER

JUNE 3, 2003

DALLAS SEMICONDUCTOR / MAXIM

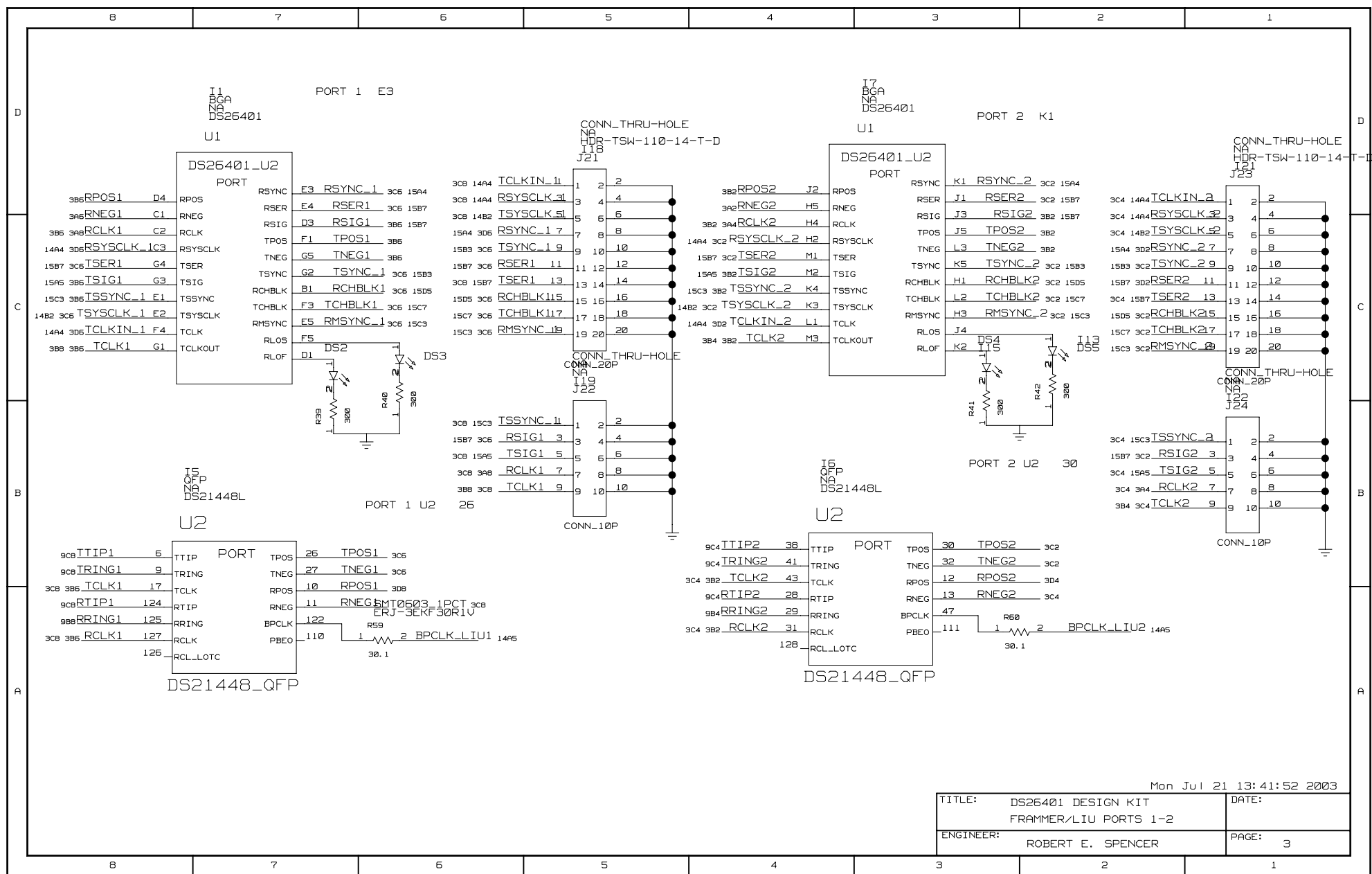
Mon Jul 21 13:41:48 2003

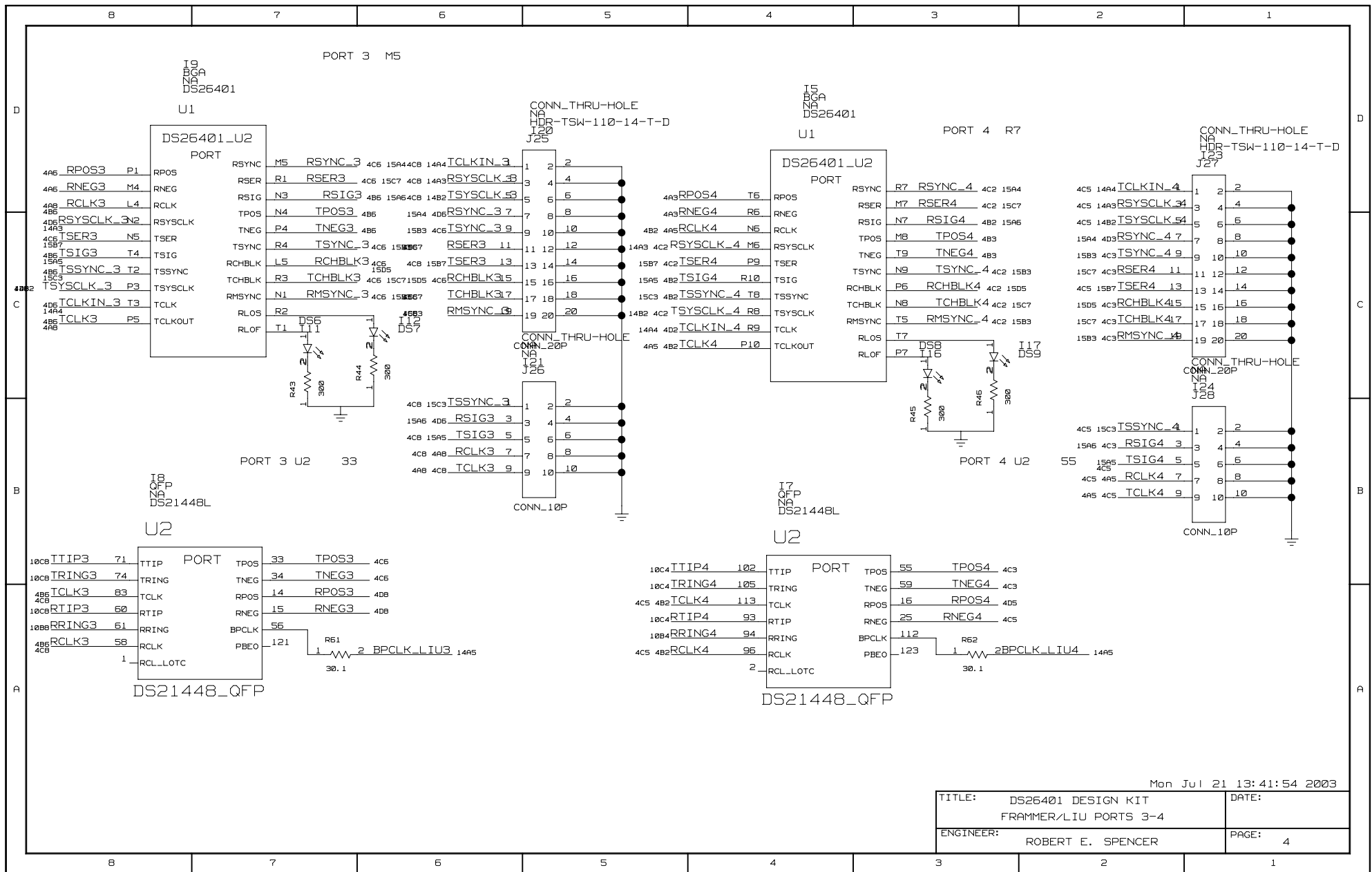
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TITLE PAGE		
ENGINEER:	ROBERT E. SPENCER	PAGE: 1



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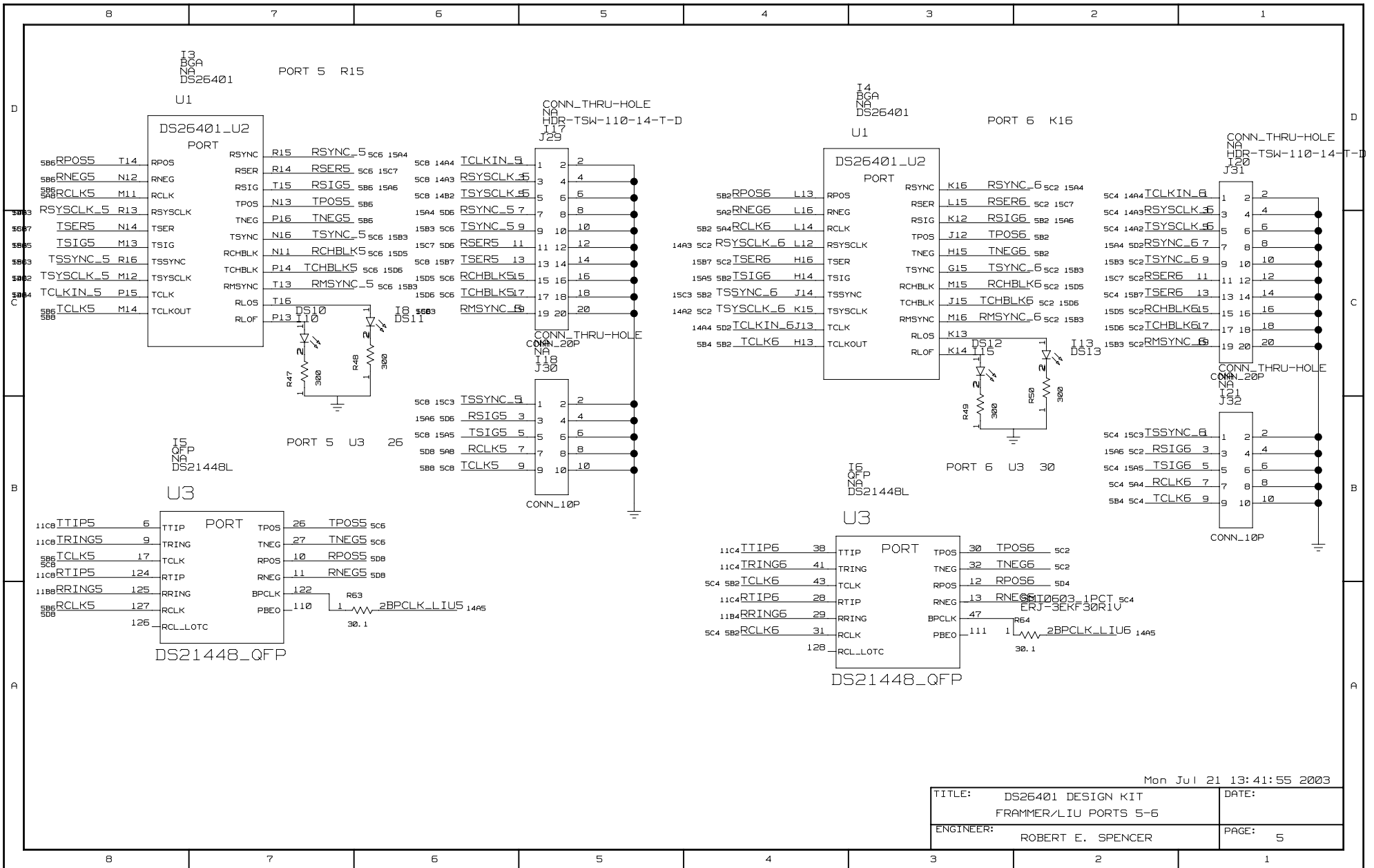
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	DS26401 CONTROL BLOCK		
ENGINEER:	ROBERT E. SPENCER	PAGE:	2

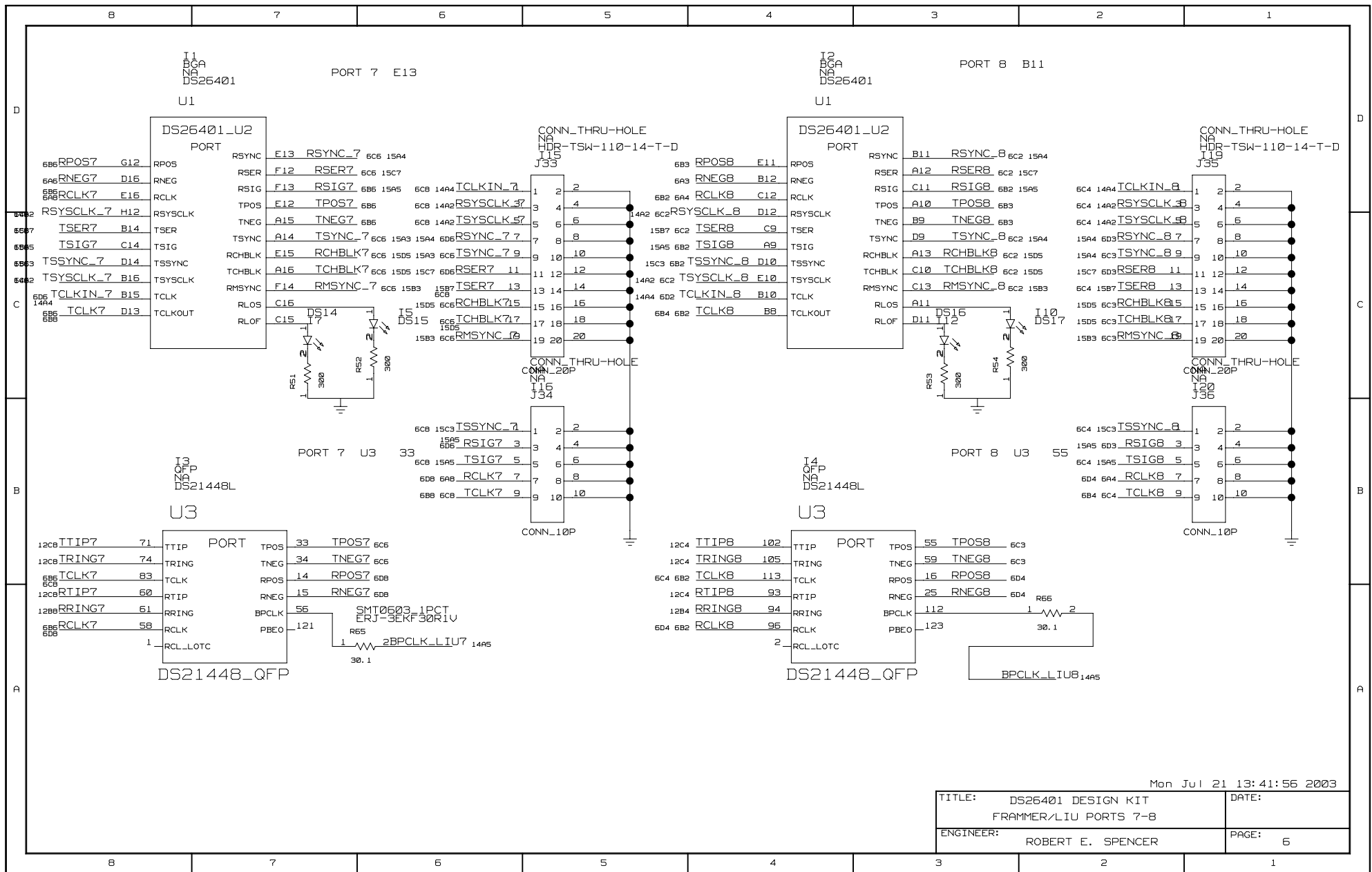


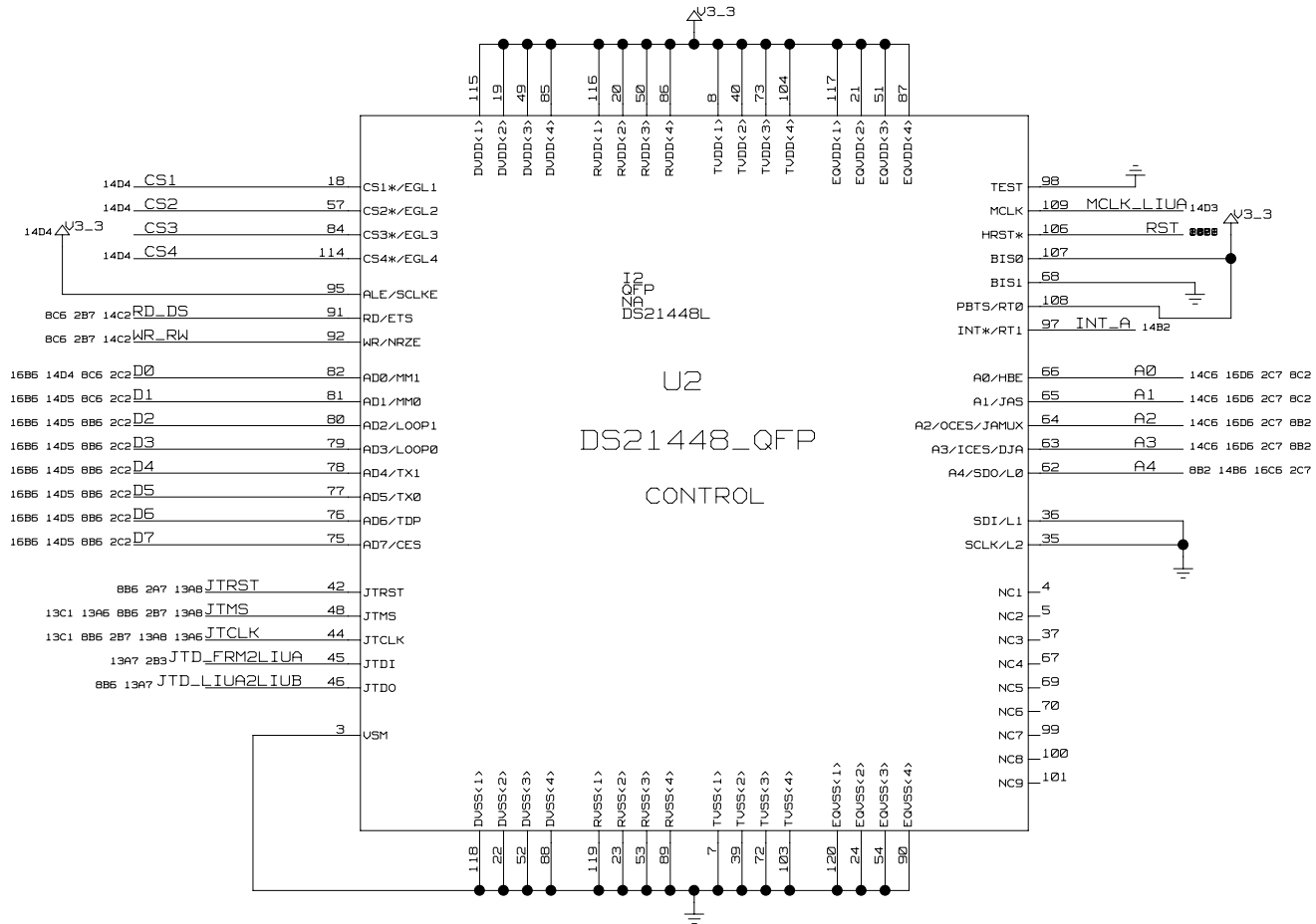


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TITLE:	DS26401 DESIGN KIT	DATE:	
	FRAMMER/LIU PORTS 3-4		
ENGINEER:	ROBERT E. SPENCER	PAGE:	4

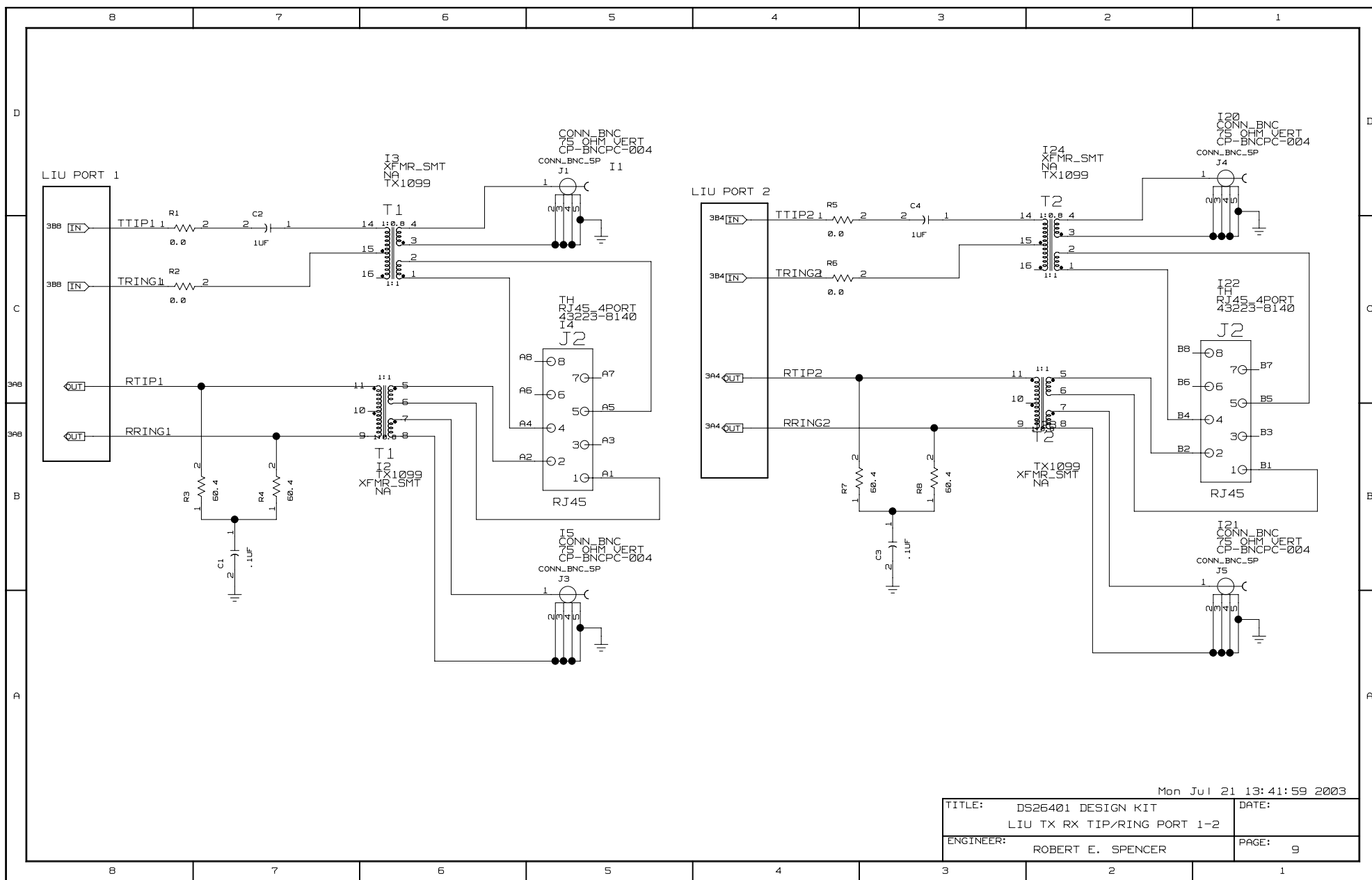




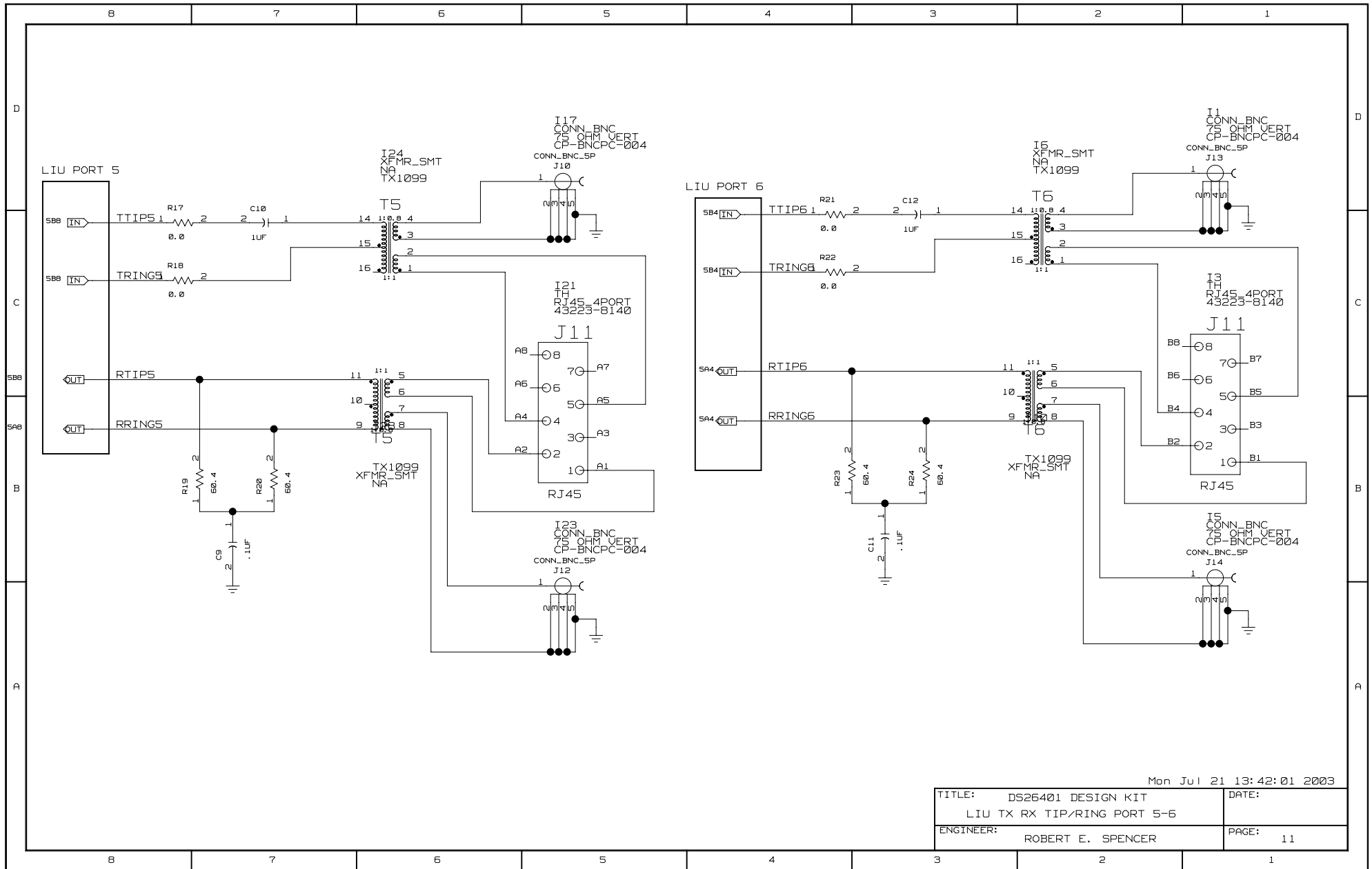


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TITLE:	DS26401 DESIGN KIT LIU CONTROL PORT 1-4	DATE:
ENGINEER:	ROBERT E. SPENCER	PAGE: 7

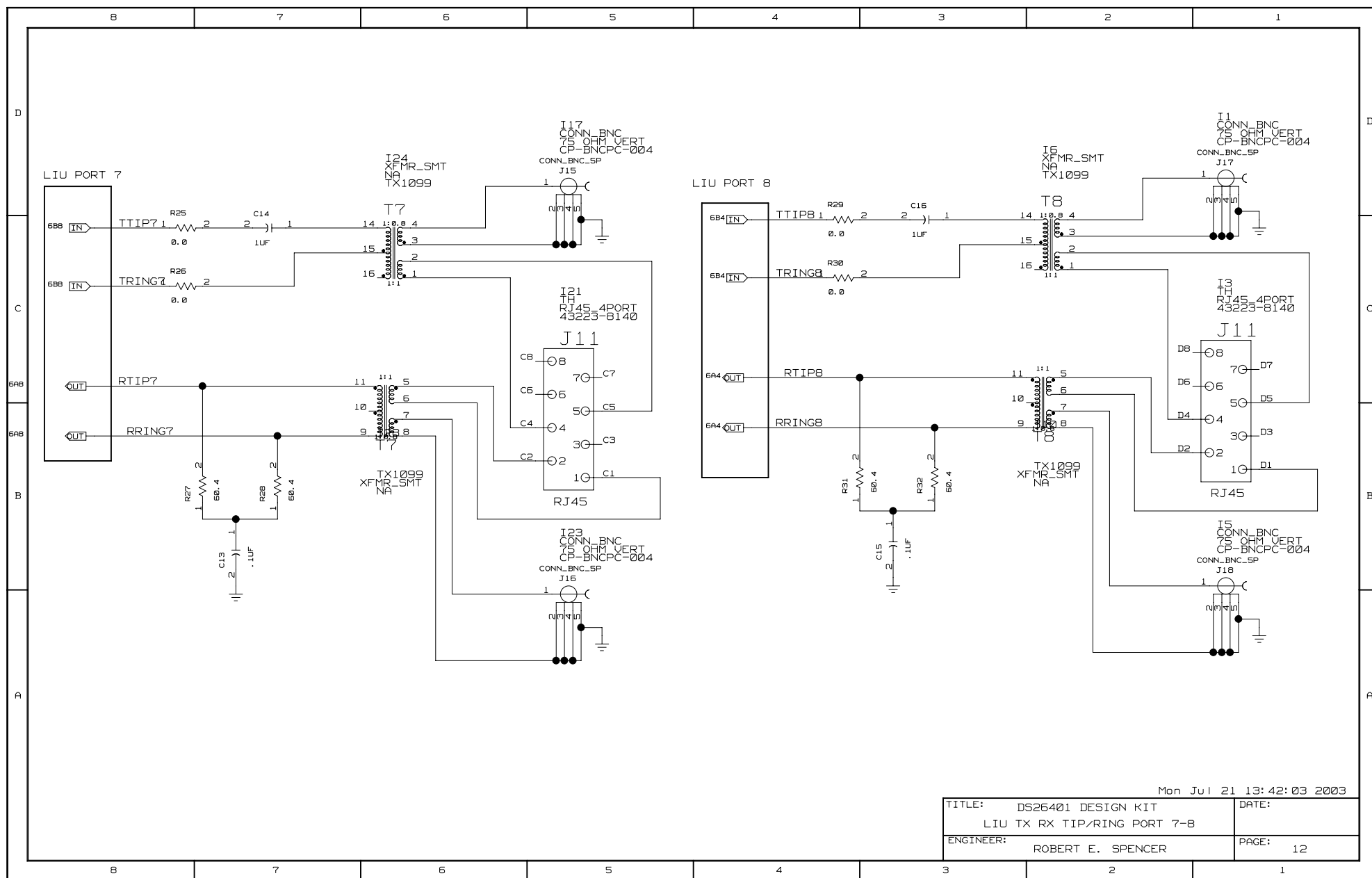


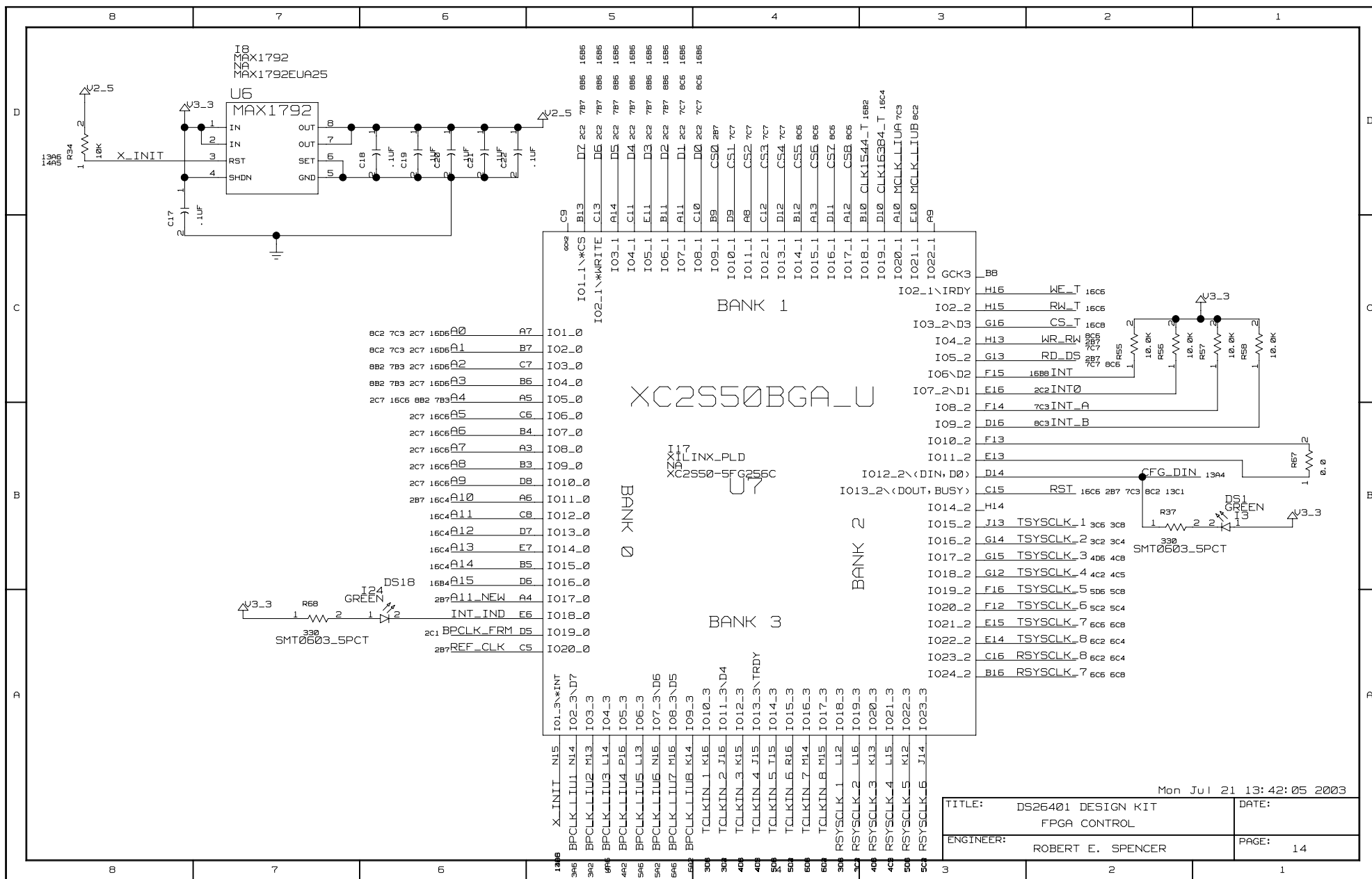
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LIU TX RX TIP/RING PORT 3-4		
ENGINEER:	ROBERT E. SPENCER	PAGE: 10

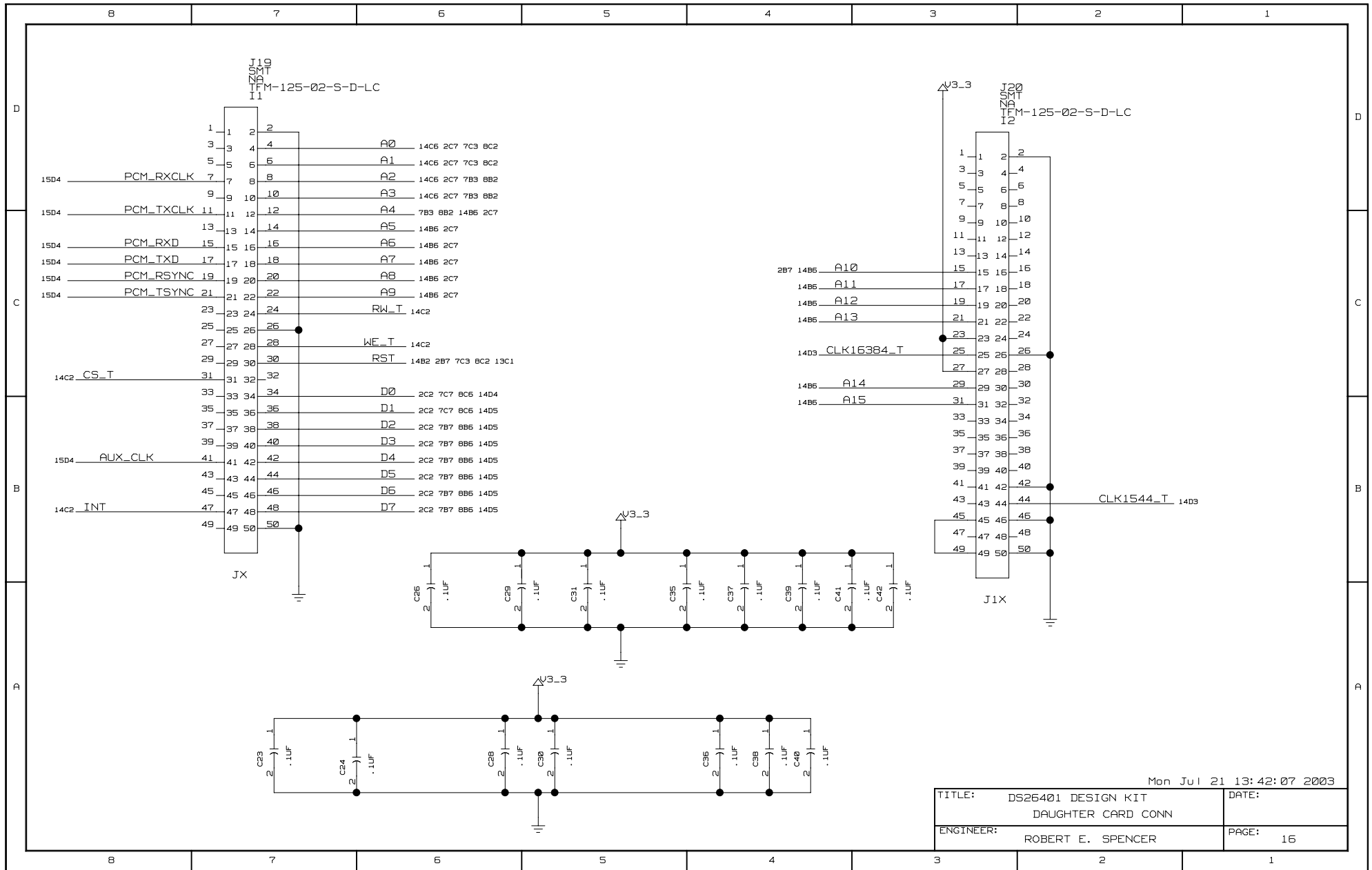


Mon Jul 21 13:42:01 2003

TITLE: DS26401 DESIGN KIT LIU TX RX TIP/RING PORT 5-6	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 11







B								7								6								5								4								3								2								1																							
D																																																																															
C																																																																															
B																																																																															
A																																																																															

8			7			6			5			4			3			2			1		
D	*** Part Cross-Reference for the entire design ***																		C				
	C1	CAP1	9B7	J21	CONN_20P	3D5	R61	RES1	4A7	B													
	C2	CAP1	9C7	J22	CONN_10P	3C5	R62	RES1	4A3														
	C3	CAP1	9B3	J23	CONN_20P	3D1	R63	RES1	5A7														
	C4	CAP1	9C3	J24	CONN_10P	3B1	R64	RES1	5A2														
	C5	CAP1	10B7	J25	CONN_20P	4D5	R65	RES1	6A7														
	C6	CAP1	10C7	J26	CONN_10P	4C6	R66	RES1	6A2														
	C7	CAP1	10B3	J27	CONN_20P	4D1	R67	RES1	14B1														
	C8	CAP1	10C3	J28	CONN_10P	4B1	R68	RES1	14A7														
	C9	CAP1	11B7	J29	CONN_20P	5D5	T1	XFMR_21N_4OUT	9B6 9C5														
C10	CAP1	11C7	J30	CONN_10P	5C5	T2	XFMR_21N_4OUT	9B2 9D2															
C	C11	CAP1	11B3	J31	CONN_20P	5D1	T3	XFMR_21N_4OUT	10B6 10C5	A													
	C12	CAP1	11C3	J32	CONN_10P	5B1	T4	XFMR_21N_4OUT	10B2 10D2														
	C13	CAP1	12B7	J33	CONN_20P	6D5	T5	XFMR_21N_4OUT	11B6 11C5														
	C14	CAP1	12C7	J34	CONN_10P	6B5	T6	XFMR_21N_4OUT	11B2 11D2														
	C15	CAP1	12B3	J35	CONN_20P	6D1	T7	XFMR_21N_4OUT	12B6 12C5														
	C16	CAP1	12C3	J36	CONN_10P	6B1	T8	XFMR_21N_4OUT	12B2 12D2														
	C17	CAP1	14C8	J37	CONN_20P	13B7	U1	DS26401_U2	2B5 3D3 3D7 4D4 4D8 5D3 5D8 6D4 6D8														
	C18	CAP1	14D6	R1	RES1	9C8	U2	DS2144B_OFF	3B4 3B8 4B4 4B8 7C5														
	C19	CAP1	14D6	R3	RES1	9B8	U3	DS2144B_OFF	5B4 5B8 6B4 6B8 8C5														
	C20	CAP1	14D6	R4	RES1	9B7	U4	XC18V02V044C_U	13A5														
B	C21	CAP1	14D6	R5	RES1	9D4	U5	MAX1792	14D7	A													
	C22	CAP1	14D6	R6	RES1	9C4	U7	XC25502BGA_U	13C4 14B4 15C5														
	C23	CAP1	16A7	R7	RES1	9B4																	
	C24	CAP1	16A7	R8	RES1	9B3																	
	C25	CAP1	16A6	R9	RES1	10C8																	
	C26	CAP1	16A6	R10	RES1	10C8																	
	C28	CAP1	16A6	R11	RES1	10B8																	
	C29	CAP1	16A6	R12	RES1	10B7																	
	C30	CAP1	16A5	R13	RES1	10D4																	
	C31	CAP1	16A5	R14	RES1	10C4																	
A	C35	CAP1	16A5	R15	RES1	10B4																	
	C36	CAP1	16A4	R16	RES1	10B3																	
	C37	CAP1	16A4	R17	RES1	11C8																	
	C38	CAP1	16A4	R18	RES1	11C8																	
	C39	CAP1	16A4	R19	RES1	11B8																	
	C40	CAP1	16A4	R20	RES1	11B7																	
	C41	CAP1	16A4	R21	RES1	11D4																	
	C42	CAP1	16A3	R22	RES1	11C4																	
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	DS2	LED	3C7	R24	RES1	11B3																	
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			DS14	LED	6C7	R36	RES1	13C1															
			DS15	LED	6C6	R37	RES1	14B2															
			DS16	LED	6C3	R38	RES1	2C2															
			DS17	LED	6C2	R39	RES1	3B7															
			DS18	LED	14B6	R40	RES1	3B6															
			J1	CONN_BNC_SP	9D5	R41	RES1	3B3															
			J2	RJ45_B	9C1 9C5 10C1 10C5	R42	RES1	3B2															
			J3	CONN_BNC_SP	9B5	R43	RES1	4B7															
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			J6	CONN_BNC_SP	10D5	R46	RES1	4B3															
			J7	CONN_BNC_SP	10B5	R47	RES1	5C7															
			J8	CONN_BNC_SP	10D1	R48	RES1	5C6															
			J9	CONN_BNC_SP	10B1	R49	RES1	5B3															
			J10	CONN_BNC_SP	11D5	R50	RES1	5B2															
			J11	RJ45_B	11C1 11C5 12C1 12C5	R51	RES1	6C7															
			J12	CONN_BNC_SP	11B5	R52	RES1	6C6															
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			J14	CONN_BNC_SP	11B1	R54	RES1	6C3															
			J15	CONN_BNC_SP	12D5	R55	RES1	14C2															
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			J17	CONN_BNC_SP	12D1	R57	RES1	14C1															
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			J19	CONN_S0P2	16D7	R59	RES1	3A6															
			J20	CONN_S0P2	16D3	R60	RES1	3A3															
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