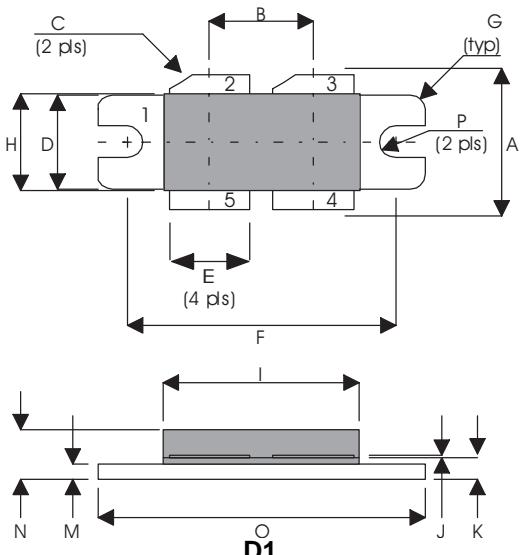


MECHANICAL DATA



PIN 1 SOURCE (COMMON)
 PIN 3 DRAIN 2
 PIN 5 GATE 1

PIN 2 DRAIN 1
 PIN 4 GATE 2

DIM	Millimetres	Tol.	Inches	Tol.
A	15.24	0.50	0.600	0.020
B	10.80	0.13	0.425	0.005
C	45°	5°	45°	5°
D	9.78	0.13	0.385	0.005
E	8.38	0.13	0.330	0.005
F	27.94	0.13	1.100	0.005
G	1.52R	0.13	0.060R	0.005
H	10.16	0.15	0.400	0.006
I	21.84	0.23	0.860	0.009
J	0.10	0.02	0.004	0.001
K	1.96	0.13	0.077	0.005
L	1.02	0.13	0.040	0.005
M	4.45	0.38	0.175	0.015
N	34.04	0.13	1.340	0.005
O	1.63R	0.13	0.064R	0.005

**IMPROVED PERFORMANCE
GOLD METALLISED
SILICON DMOS RF FET
100W – 50V – 500MHz
PUSH–PULL**

FEATURES

- SUITABLE FOR BROAD BAND APPLICATIONS
- SIMPLE BIAS CIRCUITS
- ULTRA-LOW THERMAL RESISTANCE
- BeO FREE
- LOW Crss
- HIGH GAIN – 15 dB MINIMUM

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS
from 1 MHz to 500 MHz

P_D	Power Dissipation	500W (290W -A Version)
BV_{DSS}	Drain – Source Breakdown Voltage *	125V
BV_{GSS}	Gate – Source Breakdown Voltage *	$\pm 20V$
$I_{D(sat)}$	Drain Current *	9A
T_{stg}	Storage Temperature	-65 to 150°C
T_j	Maximum Operating Junction Temperature	200°C

* Per Side

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ELECTRICAL CHARACTERISTICS ($T_{case} = 25^\circ C$ unless otherwise stated)

Parameter	Test Conditions		Min.	Typ.	Max.	Unit
PER SIDE						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$	$I_D = 100mA$	125		V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 50V$	$V_{GS} = 0$		3	mA
I_{GSS}	Gate Leakage Current	$V_{GS} = 20V$	$V_{DS} = 0$		1	μA
$V_{GS(th)}$	Gate Threshold Voltage*	$I_D = 10mA$	$V_{DS} = V_{GS}$	1	7	V
g_{fs}	Forward Transconductance*	$V_{DS} = 10V$	$I_D = 3A$	2.4		S
TOTAL DEVICE						
G_{PS}	Common Source Power Gain	$P_O = 100W$ $V_{DS} = 50V$ $f = 500MHz$	$I_{DQ} = 1.2A$	15		dB
η	Drain Efficiency			65		%
VSWR	Load Mismatch Tolerance			20:1		—
PER SIDE						
C_{iss}	Input Capacitance	$V_{DS} = 50V$	$V_{GS} = -5V$	$f = 1MHz$	100	pF
C_{oss}	Output Capacitance	$V_{DS} = 50V$	$V_{GS} = 0$	$f = 1MHz$	45	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 50V$	$V_{GS} = 0$	$f = 1MHz$	1.5	pF

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle $\leq 2\%$

THERMAL DATA

$R_{THj-case}$	Thermal Resistance Junction – Case	Max. 0.35°C / W 0.6°C / W -A Version
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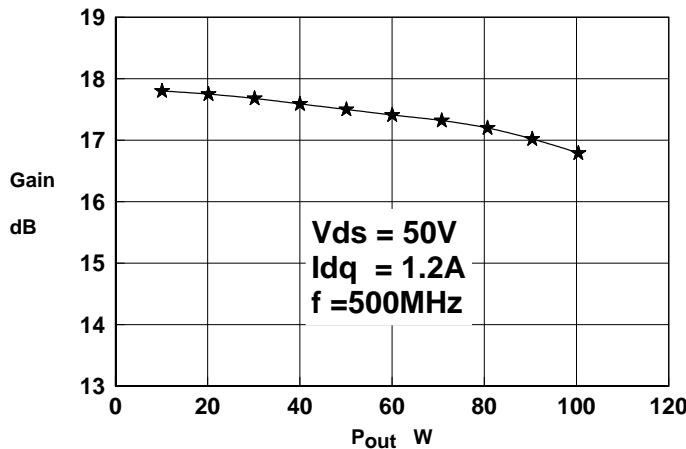


Figure 1 - Gain vs. Power Output.

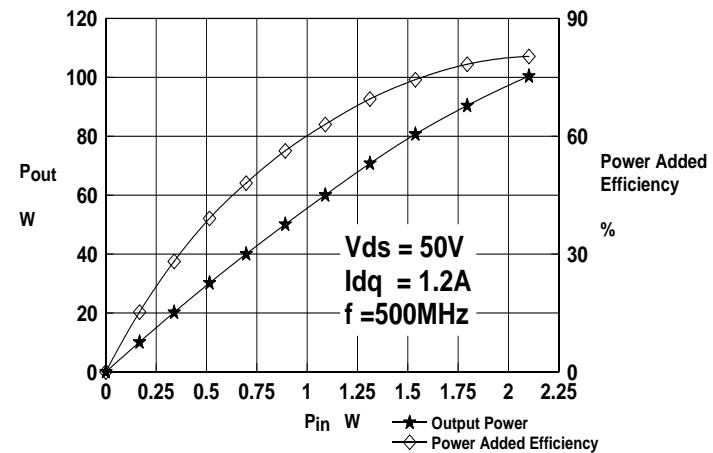


Figure 2 - Power Output & Efficiency vs. Power Input.

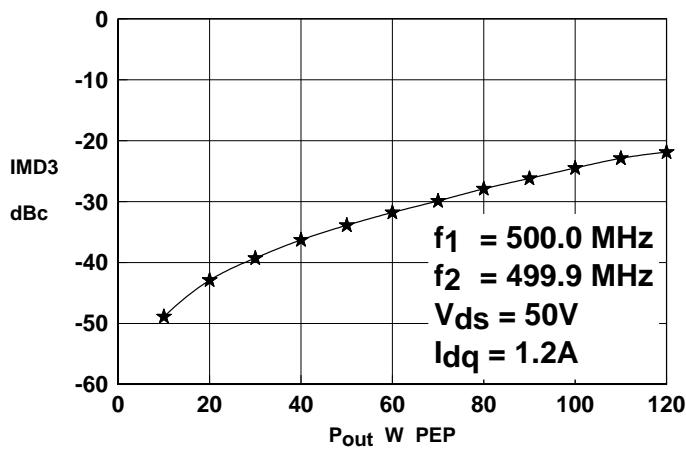


Figure 3 - IMD vs. Output Power.

DMD5012 OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z_S Ω	Z_L Ω
500	$1.6 + j2.3$	$3.5 + j2.1$

N.B. Impedances measured terminal to terminal

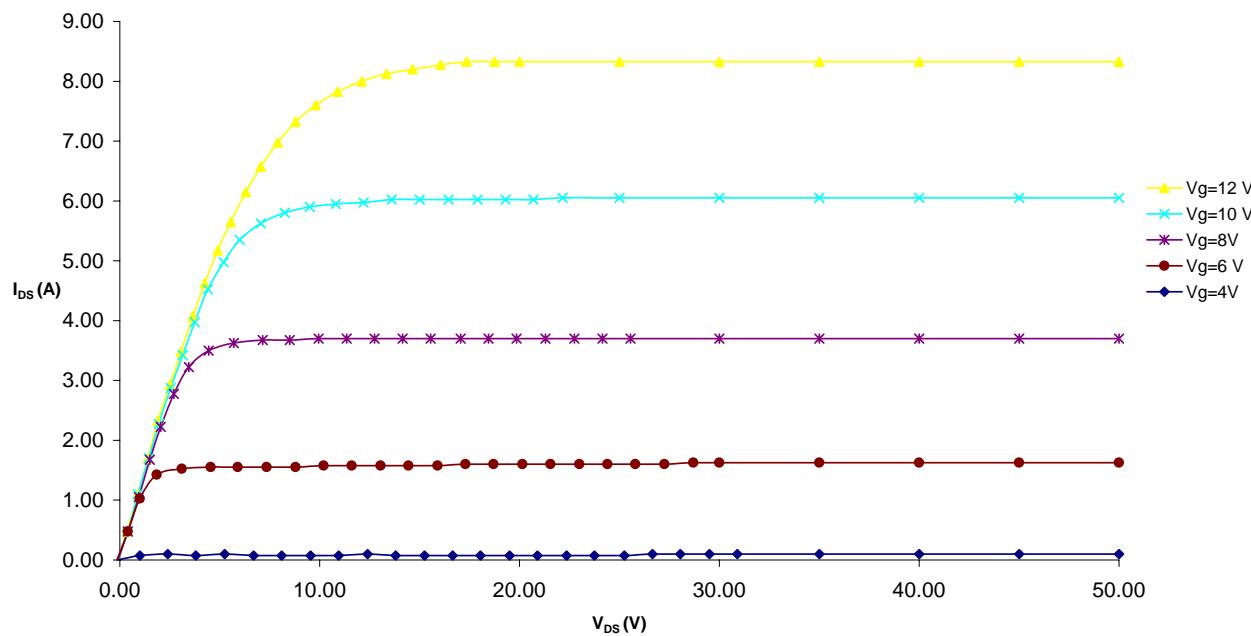


Figure 4 – Typical IV Characteristics.

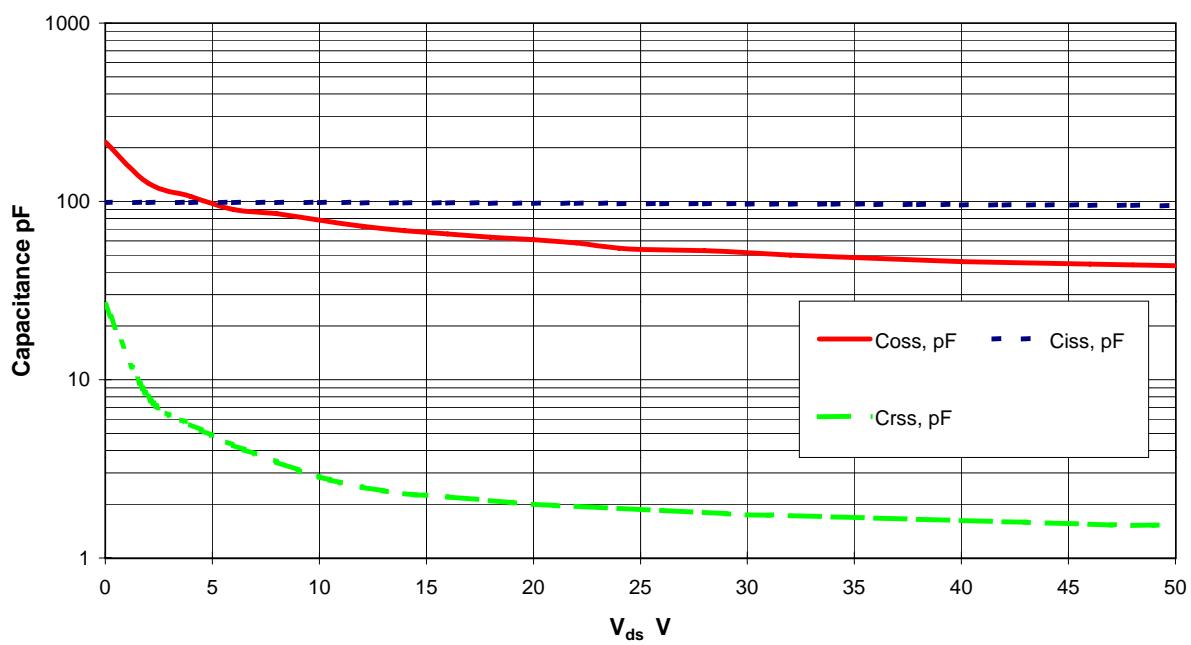


Figure 5 – Typical CV Characteristics.

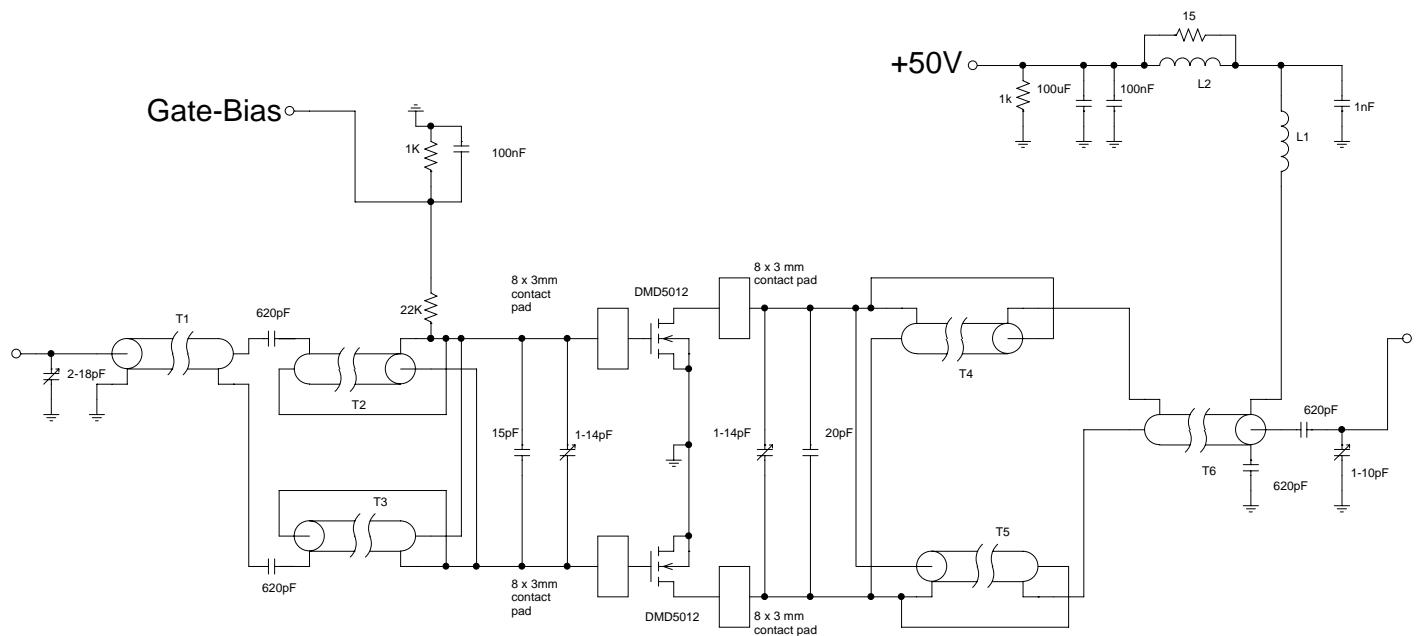
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DMD5012 500MHz TEST FIXTURE

T1,6	65mm	50 Ohm UT85 semi-rigid coax
T2,3,4,5	75mm	15 Ohm UT85-15 semi-rigid coax
L1	6 turns	21 swg enamelled copper wire, 3mm i.d.
L2	8.5 turns	19 swg enamelled copper wire on Fair-Rite FT82-43 core

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