



# 28V, 100mA, Low-Quiescent-Current LDO with Reset and Power-Fail Input/Output

## General Description

The MAX5091 high-voltage linear regulator is designed to operate from a +5V to +28V input voltage, and withstands up to 40V transients. The device consumes only 45µA of quiescent current at 100µA output current. The MAX5091 delivers up to 100mA of output current with low 50mV maximum dropout voltage. The MAX5091 provides an active-low open-drain microprocessor RESET output. The reset timeout period is programmable and can be set with an external capacitor. The MAX5091 includes an uncommitted comparator for input voltage monitoring/power-fail indication. The device is available with a fixed +5V (MAX5091A) or +3.3V (MAX5091B) output. The MAX5091 is short-circuit protected and includes thermal shutdown.

The MAX5091 operates over the -40°C to +125°C automotive temperature range and is available in 8-pin, thermally enhanced TDFN and SO-EP packages.

## Applications

Automotive  
Industrial

Home Security/Safety  
Telecom/Networking

## Features

- ◆ +5V to +28V Wide Operating Input Voltage Range
- ◆ Withstands 40V Input Voltage Transients
- ◆ Guaranteed 100mA Output Current
- ◆ 45µA Typical Quiescent Current at 100µA Output Current
- ◆ Preset +5V (MAX5091A) or +3.3V (MAX5091B) Output Voltage
- ◆ Stable with Only 10µF Output Capacitance
- ◆ RESET Output with Adjustable Timeout Period
- ◆ Uncommitted Comparator for Voltage Monitoring/Power-Fail Indication
- ◆ Output Overload and Short-Circuit Protection
- ◆ Thermal Shutdown
- ◆ Available in 8-Pin TDFN (1.95W at T<sub>A</sub> = +70°C) and 8-Pin SO (1.5W at T<sub>A</sub> = +70°C)
- ◆ Operates Over -40°C to +125°C Automotive Temperature Range

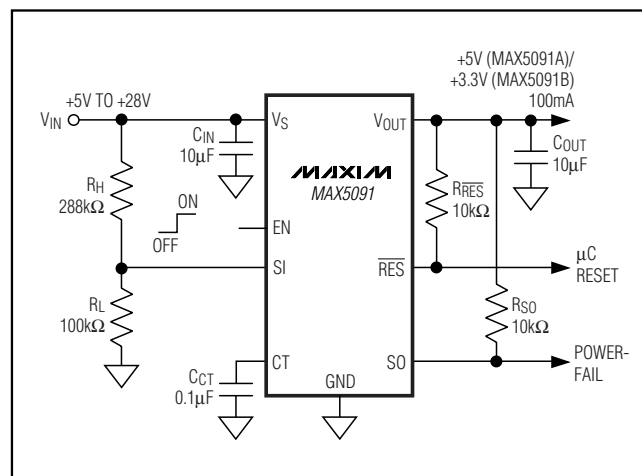
## Ordering Information

| PART          | PIN-PACKAGE | PRESET V <sub>OUT</sub> (V) | PKG CODE | TOP MARK |
|---------------|-------------|-----------------------------|----------|----------|
| MAX5091AATA+T | 8 TDFN-8    | 5                           | T833-2   | +APB     |
| MAX5091AASA+  | 8 SO-EP*    | 5                           | S8E-14   | —        |
| MAX5091BATA+T | 8 TDFN-8    | 3.3                         | T833-2   | +APC     |
| MAX5091BASA+  | 8 SO-EP*    | 3.3                         | S8E-14   | —        |

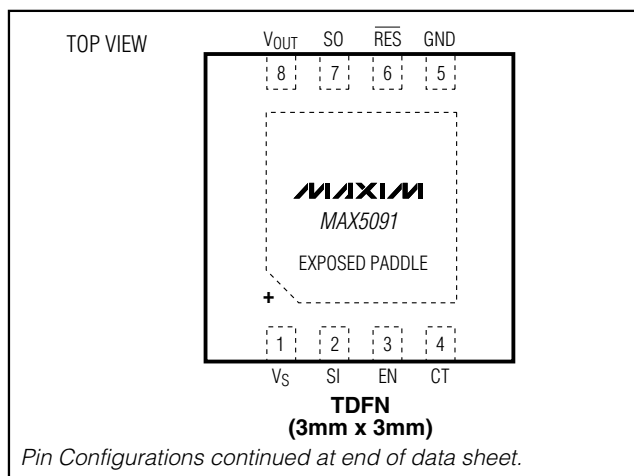
**Note:** All devices specified for -40°C to +125°C operating temperature range.

+Denotes lead-free package. \*EP = Exposed paddle.

## Typical Application Circuit



## Pin Configurations



# 28V, 100mA, Low-Quiescent-Current LDO with Reset and Power-Fail Input/Output

## ABSOLUTE MAXIMUM RATINGS

|                                                       |                                                     |
|-------------------------------------------------------|-----------------------------------------------------|
| V <sub>S</sub> to GND                                 | .....-0.3V to +28V                                  |
| V <sub>S</sub> to GND (t ≤ 1s)                        | .....-0.3V to +40V                                  |
| V <sub>OUT</sub> to GND                               | .....-0.3V to +20V                                  |
| V <sub>S</sub> to OUT                                 | .....-0.3V to +28V                                  |
| RES, SO to GND                                        | .....-0.3V to +20V                                  |
| RES, SO Output Sink Current                           | .....5mA                                            |
| V <sub>OUT</sub> Short Circuit (V <sub>S</sub> ≤ 16V) | .....Continuous                                     |
| EN, SI to GND                                         | .....-0.3V to +12V                                  |
| CT to GND                                             | .....-0.3V to the lower of V <sub>OUT</sub> or +12V |

|                                                       |                      |
|-------------------------------------------------------|----------------------|
| Continuous Power Dissipation (T <sub>A</sub> = +70°C) |                      |
| 8-Pin SO-EP (derate 19.2mW/°C above +70°C)            | .....1538mW*         |
| Thermal Resistance (θ <sub>JA</sub> )                 | .....52°C/W          |
| Thermal Resistance (θ <sub>JC</sub> )                 | .....6°C/W           |
| 8-Pin TDFN-EP (derate 24.4mW/°C above +70°C)          | .....1951mW**        |
| Thermal Resistance (θ <sub>JA</sub> )                 | .....41°C/W          |
| Thermal Resistance (θ <sub>JC</sub> )                 | .....8.3°C/W         |
| Operating Junction Temperature Range                  | .....-40°C to +125°C |
| Maximum Junction Temperature                          | .....+150°C          |
| Storage Temperature Range                             | .....-60°C to +150°C |
| Lead Temperature (soldering, 10s)                     | .....+300°C          |

\*As per JEDEC51 Standard (single-layer board).

\*\*As per JEDEC51 Standard (multilayer board).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS (MAX5091A)

(V<sub>S</sub> = +14V, V<sub>OUT</sub> = 5V, EN unconnected, T<sub>A</sub> = T<sub>J</sub> = -40°C to +125°C, C<sub>IN</sub> = 10μF, C<sub>OUT</sub> = 10μF, unless otherwise noted. Typical specifications are at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                                     | SYMBOL                | CONDITIONS                                                                   | MIN                      | TYP  | MAX  | UNITS |
|---------------------------------------------------------------|-----------------------|------------------------------------------------------------------------------|--------------------------|------|------|-------|
| Output Voltage                                                | V <sub>OUT</sub>      | T <sub>A</sub> = +25°C, I <sub>OUT</sub> = 1mA                               | 4.95                     | 5    | 5.05 | V     |
|                                                               |                       | 5.6V ≤ V <sub>S</sub> ≤ 28V, I <sub>OUT</sub> = 1mA to 50mA (Note 2)         | 4.90                     | 5    | 5.10 |       |
|                                                               |                       | 5.6V ≤ V <sub>S</sub> ≤ 40V, t ≤ 1s, I <sub>OUT</sub> = 1mA to 30mA (Note 2) | 4.9                      | 5    | 5.1  |       |
|                                                               |                       | V <sub>S</sub> = +8V, I <sub>OUT</sub> = 1mA to 100mA                        | 4.9                      | 5    | 5.1  |       |
| Dropout Voltage                                               | V <sub>DP</sub>       | V <sub>S</sub> = +4.75V                                                      | I <sub>OUT</sub> = 10mA  | 0.1  | 0.25 | V     |
|                                                               |                       |                                                                              | I <sub>OUT</sub> = 50mA  | 0.2  | 0.4  |       |
|                                                               |                       |                                                                              | I <sub>OUT</sub> = 100mA | 0.3  | 0.5  |       |
| V <sub>S</sub> to V <sub>OUT</sub> Difference in Undervoltage | V <sub>IO</sub>       | V <sub>S</sub> = +4V, I <sub>OUT</sub> = 35mA                                |                          |      | 0.4  | V     |
| Line Regulation                                               | V <sub>OL</sub>       | +5.5V ≤ V <sub>S</sub> ≤ +28V, I <sub>OUT</sub> = 1mA                        |                          | 0.6  | 5    | mV    |
| Load Regulation                                               | V <sub>OLO</sub>      | 1mA ≤ I <sub>OUT</sub> ≤ 100mA                                               |                          | 17   | 50   | mV    |
| Current Limit                                                 | I <sub>LIM</sub>      |                                                                              | 160                      | 260  | 400  | mA    |
| Quiescent Current                                             | I <sub>Q</sub>        | I <sub>OUT</sub> = 100μA                                                     |                          | 46   | 100  | μA    |
|                                                               |                       | I <sub>OUT</sub> = 300μA                                                     |                          | 45   | 100  |       |
|                                                               |                       | I <sub>OUT</sub> = 100mA                                                     |                          | 4.5  | 10   | mA    |
| Shutdown Supply Current                                       | I <sub>SHDN</sub>     | V <sub>EN</sub> ≤ +0.4V                                                      |                          | 17   | 30   | μA    |
| Thermal-Shutdown Temperature                                  | T <sub>J(SHDN)</sub>  | Temperature rising                                                           |                          | +165 |      | °C    |
| Thermal-Shutdown Hysteresis                                   | ΔT <sub>J(SHDN)</sub> |                                                                              |                          | 20   |      | °C    |

# 28V, 100mA, Low-Quiescent-Current LDO with Reset and Power-Fail Input/Output

## ELECTRICAL CHARACTERISTICS (MAX5091A) (continued)

( $V_S = +14V$ ,  $V_{OUT} = 5V$ , EN unconnected,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ ,  $C_{IN} = 10\mu F$ ,  $C_{OUT} = 10\mu F$ , unless otherwise noted. Typical specifications are at  $T_A = +25^\circ C$ .) (Note 1)

| PARAMETER                                    | SYMBOL            | CONDITIONS                                                                               | MIN  | TYP  | MAX  | UNITS             |
|----------------------------------------------|-------------------|------------------------------------------------------------------------------------------|------|------|------|-------------------|
| RESET                                        |                   |                                                                                          |      |      |      |                   |
| Reset Threshold Voltage                      | V <sub>RT</sub>   | V <sub>OUT</sub> falling                                                                 | 85   | 90   | 94.5 | %V <sub>OUT</sub> |
| Reset Threshold Hysteresis                   | V <sub>RTH</sub>  |                                                                                          | 30   | 65   | 100  | mV                |
| Reset Pulse Delay                            | t <sub>RD</sub>   | C <sub>CT</sub> = 100nF, t <sub>R</sub> ≥ 100μs                                          | 55   | 110  | 180  | ms                |
| $\overline{RES}$ Output Low Voltage          | V <sub>RL</sub>   | V <sub>S</sub> ≥ +1.5V, R $\overline{RES}$ = 10kΩ to V <sub>OUT</sub>                    |      |      | 0.4  | V                 |
| $\overline{RES}$ Output High Leakage Current | I <sub>RH</sub>   | V $\overline{RES}$ = 5V                                                                  |      |      | 1.0  | μA                |
| Delay Comparator Threshold                   | V <sub>CTTH</sub> | V <sub>CT</sub> rising                                                                   | 1.9  | 2.1  | 2.4  | V                 |
| Delay Comparator Threshold Hysteresis        |                   |                                                                                          |      | 100  |      | mV                |
| SENSE                                        |                   |                                                                                          |      |      |      |                   |
| Sense Threshold                              | V <sub>ST</sub>   | V <sub>SI</sub> falling                                                                  | 1.10 | 1.16 | 1.24 | V                 |
| Sense Threshold Hysteresis                   |                   |                                                                                          | 50   | 100  | 150  | mV                |
| Sense Output Low Voltage                     | V <sub>SL</sub>   | V <sub>SI</sub> ≤ 1.10V, V <sub>S</sub> ≥ 4V, R <sub>SO</sub> = 10kΩ to V <sub>OUT</sub> |      |      | 0.4  | V                 |
| Sense Output Leakage Current                 | I <sub>SH</sub>   | V <sub>SO</sub> = 5V, V <sub>SI</sub> ≥ 1.5V                                             |      |      | 1    | μA                |
| Sense Input Current                          | I <sub>SI</sub>   | V <sub>SI</sub> = 3.3V                                                                   | -1   |      | +1   | μA                |
| ENABLE                                       |                   |                                                                                          |      |      |      |                   |
| Enable Voltage                               | V <sub>EN</sub>   | EN = high, regulator on                                                                  | 2.4  |      |      | V                 |
|                                              |                   | EN = low, regulator off                                                                  | 0.4  |      |      |                   |
| Enable Internal Pullup Current               | I <sub>EN</sub>   | EN is internally pulled up to 3.6V (max)                                                 |      |      | 3    | μA                |

MAX5091

# 28V, 100mA, Low-Quiescent-Current LDO with Reset and Power-Fail Input/Output

## ELECTRICAL CHARACTERISTICS (MAX5091B)

( $V_S = +14V$ ,  $V_{OUT} = 3.3V$ , EN unconnected,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ ,  $C_{IN} = 10\mu F$ ,  $C_{OUT} = 10\mu F$ , unless otherwise noted. Typical specifications are at  $T_A = +25^\circ C$ .) (Note 1)

| PARAMETER                                     | SYMBOL               | CONDITIONS                                                             | MIN   | TYP  | MAX   | UNITS       |
|-----------------------------------------------|----------------------|------------------------------------------------------------------------|-------|------|-------|-------------|
| Output Voltage                                | $V_{OUT}$            | $T_A = +25^\circ C$ , $I_{OUT} = 1mA$                                  | 3.267 | 3.3  | 3.333 | V           |
|                                               |                      | $5V \leq V_S \leq 28V$ , $I_{OUT} = 1mA$ to $50mA$ (Note 2)            | 3.234 | 3.3  | 3.366 |             |
|                                               |                      | $5V \leq V_S \leq 40V$ , $t < 1s$ , $I_{OUT} = 1mA$ to $30mA$ (Note 2) | 3.234 | 3.3  | 3.366 |             |
|                                               |                      | $V_S = +8V$ , $I_{OUT} = 1mA$ to $100mA$                               | 3.234 | 3.3  | 3.366 |             |
| $V_S$ to $V_{OUT}$ Difference in Undervoltage | $V_{IO}$             | $V_S = 3.5V$ , $I_{OUT} = 35mA$                                        |       | 0.2  | 0.4   | V           |
| Line Regulation                               | $V_{OL}$             | $5V \leq V_S \leq 28V$ , $I_{OUT} = 1mA$                               |       | 0.6  | 5     | mV          |
| Load Regulation                               | $V_{OLO}$            | $1mA \leq I_{OUT} \leq 100mA$                                          |       | 11   | 40    | mV          |
| Current Limit                                 | $I_{LIM}$            |                                                                        | 160   | 260  | 400   | mA          |
| Quiescent Current                             | $I_Q$                | $I_{OUT} = 100\mu A$                                                   |       | 45   | 100   | $\mu A$     |
|                                               |                      | $I_{OUT} = 300\mu A$                                                   |       | 45   | 100   |             |
|                                               |                      | $I_{OUT} = 100mA$                                                      |       | 4.4  | 10    | mA          |
| Shutdown Supply Current                       | $I_{SHDN}$           | $V_{EN} \leq 0.4V$                                                     |       | 17   | 30    | $\mu A$     |
| Thermal-Shutdown Temperature                  | $T_{J(SHDN)}$        | Temperature rising                                                     |       | +165 |       | $^\circ C$  |
| Thermal-Shutdown Hysteresis                   | $\Delta T_{J(SHDN)}$ |                                                                        |       | 20   |       | $^\circ C$  |
| <b>RESET CIRCUIT</b>                          |                      |                                                                        |       |      |       |             |
| Reset Threshold Voltage                       | $V_{RT}$             | $V_{OUT}$ falling                                                      | 85    | 90   | 94.5  | $\%V_{OUT}$ |
| Reset Threshold Hysteresis                    | $V_{RTH}$            |                                                                        | 20    | 45   | 80    | mV          |
| Reset Pulse Delay                             | $t_{RD}$             | $C_{CT} = 100nF$ , $t_R \geq 100\mu s$                                 | 55    | 105  | 180   | ms          |
| $\overline{RES}$ Output-Low Voltage           | $V_{RL}$             | $V_S \geq 1.5V$ , $R_{\overline{RES}} = 4k\Omega$ to $V_{OUT}$         |       |      | 0.4   | V           |
| $\overline{RES}$ Output-High Leakage Current  | $I_{RH}$             | $V_{\overline{RES}} = 3.3V$                                            |       |      | 1.0   | $\mu A$     |
| Delay Comparator Threshold                    | $V_{CTTH}$           | $V_{CT}$ rising                                                        | 1.9   | 2.1  | 2.4   | V           |
| Delay Comparator Threshold Hysteresis         |                      |                                                                        |       | 100  |       | mV          |

# 28V, 100mA, Low-Quiescent-Current LDO with Reset and Power-Fail Input/Output

## ELECTRICAL CHARACTERISTICS (MAX5091B) (continued)

( $V_S = +14V$ ,  $V_{OUT} = 3.3V$ , EN unconnected,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ ,  $C_{IN} = 10\mu F$ ,  $C_{OUT} = 10\mu F$ , unless otherwise noted. Typical specifications are at  $T_A = +25^\circ C$ .) (Note 1)

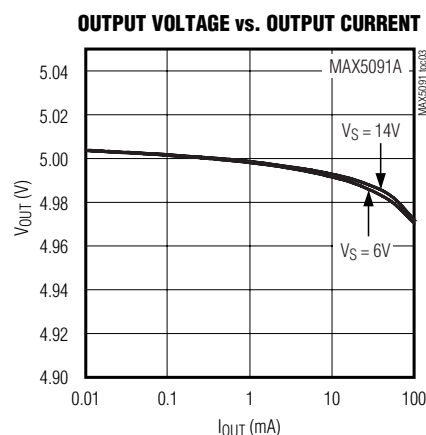
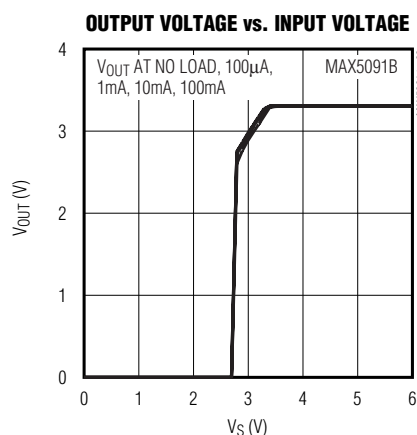
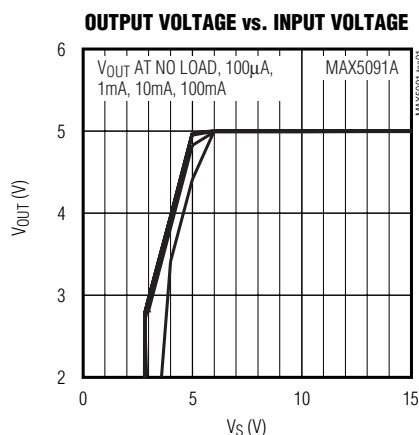
| PARAMETER                      | SYMBOL   | CONDITIONS                                                              | MIN  | TYP  | MAX  | UNITS   |
|--------------------------------|----------|-------------------------------------------------------------------------|------|------|------|---------|
| <b>SENSE</b>                   |          |                                                                         |      |      |      |         |
| Sense Threshold                | $V_{ST}$ | $V_{SI}$ falling                                                        | 1.09 | 1.15 | 1.23 | V       |
| Sense Threshold Hysteresis     |          |                                                                         | 50   | 100  | 150  | mV      |
| Sense Output-Low Voltage       | $V_{SL}$ | $V_{SI} \leq 1.09V$ , $V_S \geq 4V$ , $R_{SO} = 10k\Omega$ to $V_{OUT}$ |      |      | 0.4  | V       |
| Sense Output Leakage Current   | $I_{SH}$ | $V_{SO} = 3.3V$ , $V_{SI} \geq 1.5V$                                    |      |      | 1    | $\mu A$ |
| Sense Input Current            | $I_{SI}$ | $V_{SI} = 3.3V$                                                         | -1   |      | +1   | $\mu A$ |
| <b>ENABLE</b>                  |          |                                                                         |      |      |      |         |
| Enable Voltage                 | $V_{EN}$ | EN = high, regulator on                                                 | 2.4  |      |      | V       |
|                                |          | EN = low, regulator off                                                 |      |      | 0.4  |         |
| Enable Internal Pullup Current | $I_{EN}$ | EN is internally pulled up to 3.6V (max)                                |      |      | 3    | $\mu A$ |

**Note 1:** Limits at  $T_A = -40^\circ C$  are guaranteed by design and not production tested.

**Note 2:** Maximum output current is limited by the power dissipation capability of the package.

## Typical Operating Characteristics

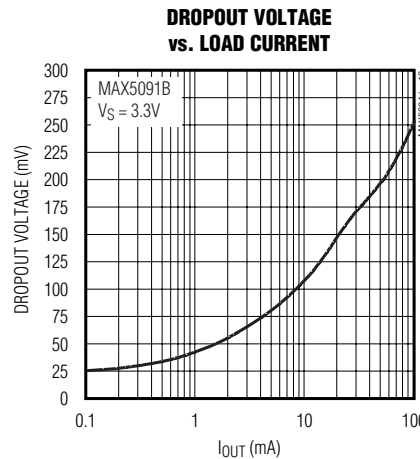
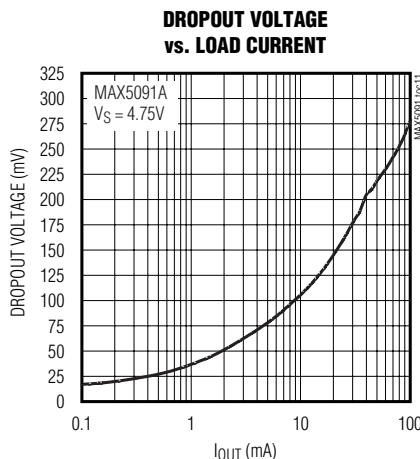
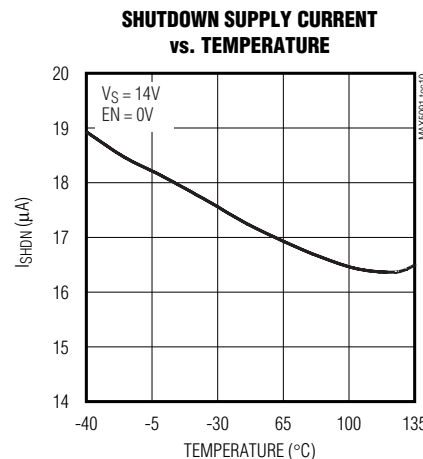
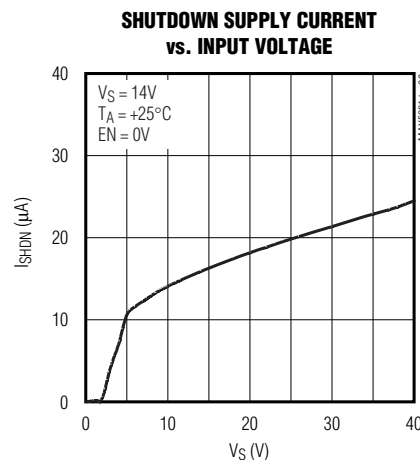
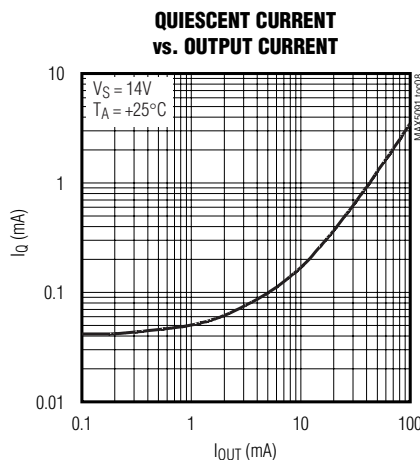
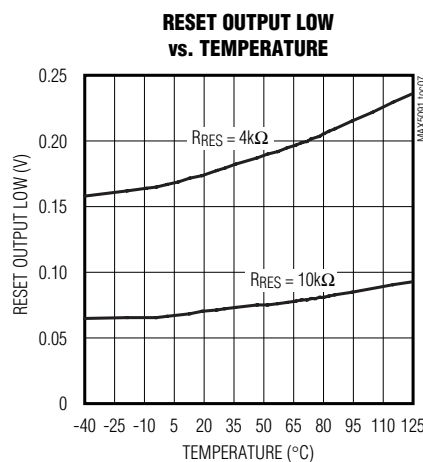
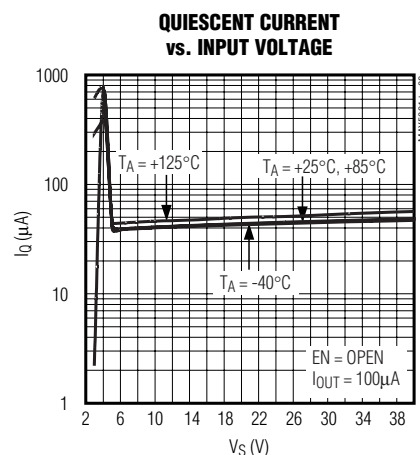
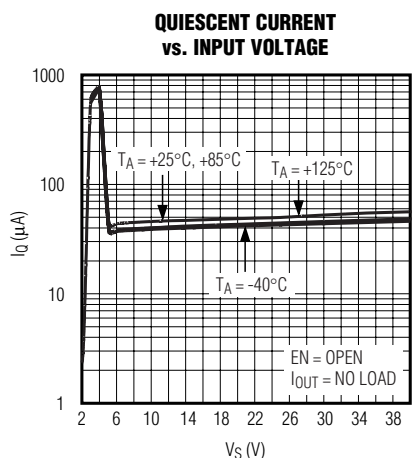
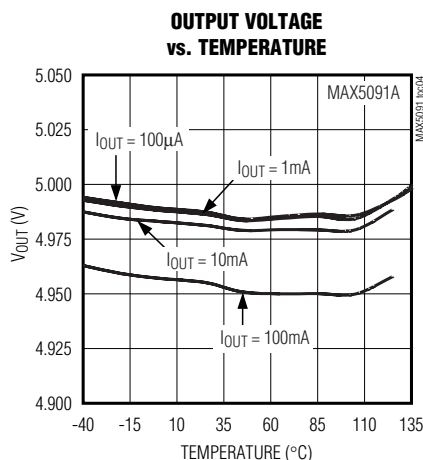
(Typical Application Circuit,  $V_S = +14V$ ,  $C_{IN} = 10\mu F$ ,  $C_{OUT} = 10\mu F$ ,  $V_{SI} = 0V$ ,  $V_{EN} = +2.4V$ ,  $V_{OUT} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# 28V, 100mA, Low-Quiescent-Current LDO with Reset and Power-Fail Input/Output

## Typical Operating Characteristics (continued)

(Typical Application Circuit,  $V_S = +14V$ ,  $C_{IN} = 10\mu F$ ,  $C_{OUT} = 10\mu F$ ,  $V_{SI} = 0V$ ,  $V_{EN} = +2.4V$ ,  $V_{OUT} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



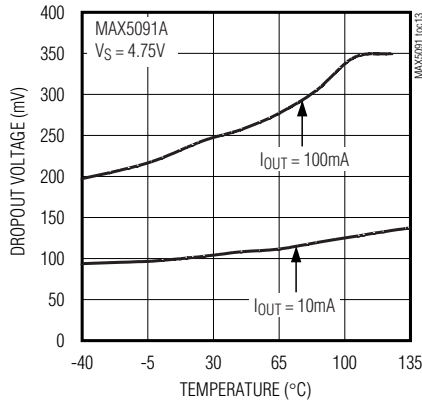
# 28V, 100mA, Low-Quiescent-Current LDO with Reset and Power-Fail Input/Output

MAX5091

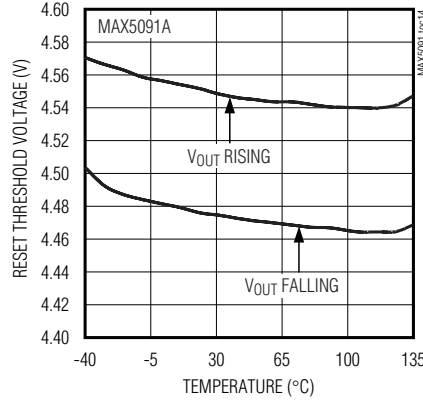
## Typical Operating Characteristics (continued)

(Typical Application Circuit,  $V_S = +14V$ ,  $C_{IN} = 10\mu F$ ,  $C_{OUT} = 10\mu F$ ,  $V_{SI} = 0V$ ,  $V_{EN} = +2.4V$ ,  $V_{OUT} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

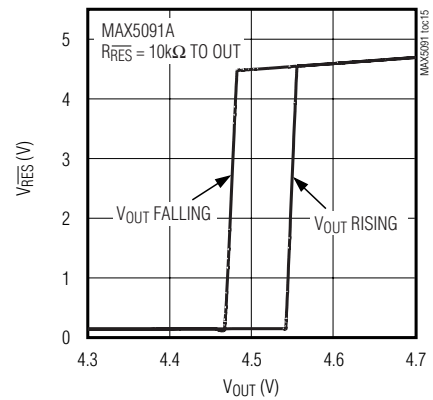
**DROPOUT VOLTAGE vs. TEMPERATURE**



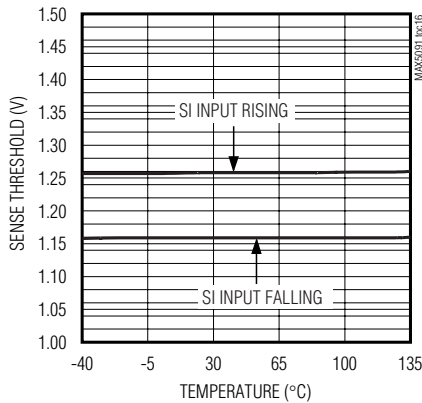
**RESET THRESHOLD vs. TEMPERATURE**



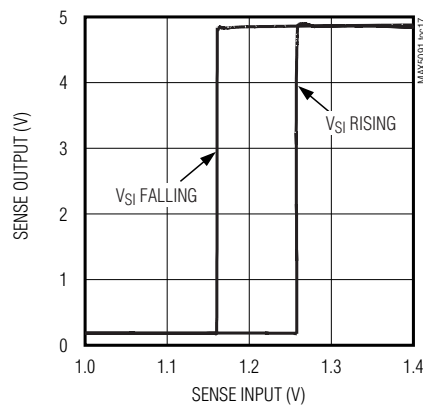
**RESET VOLTAGE vs. OUTPUT VOLTAGE**



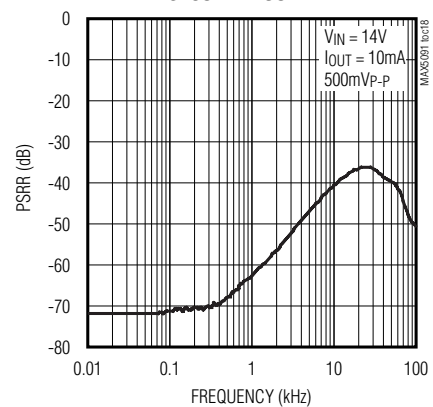
**SENSE THRESHOLD vs. TEMPERATURE**



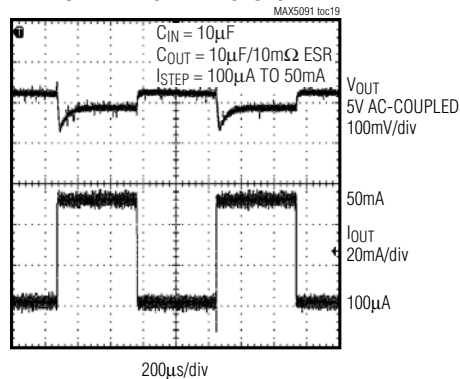
**SENSE OUTPUT vs. SENSE INPUT**



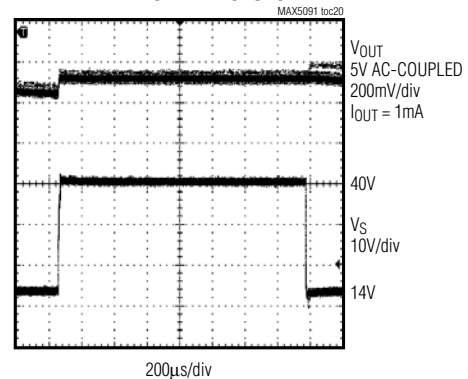
**POWER-SUPPLY REJECTION RATIO vs. SUPPLY CURRENT**



**LOAD-TRANSIENT RESPONSE**



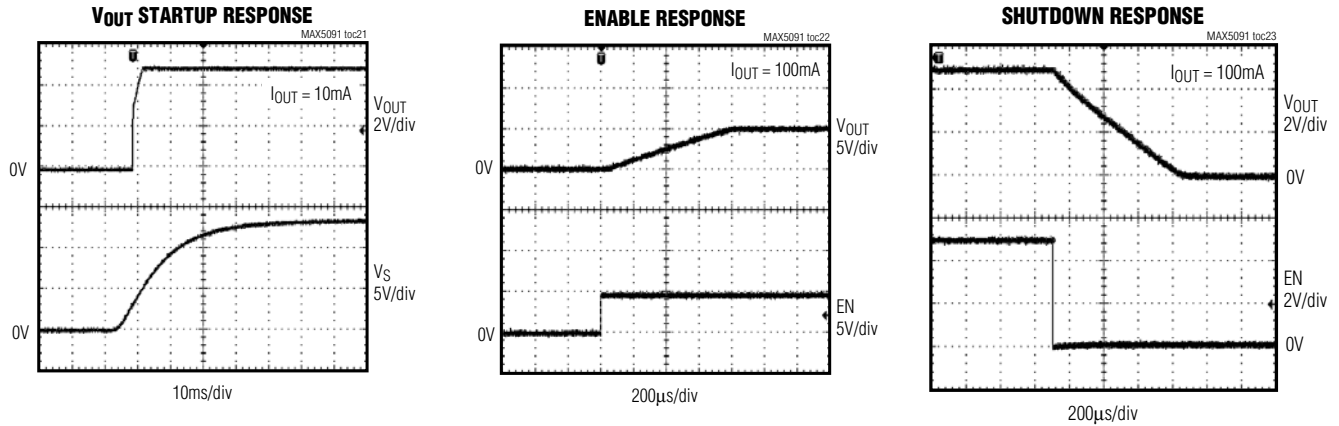
**LINE-TRANSIENT RESPONSE**



# 28V, 100mA, Low-Quiescent-Current LDO with Reset and Power-Fail Input/Output

## Typical Operating Characteristics (continued)

(Typical Application Circuit,  $V_S = +14V$ ,  $C_{IN} = 10\mu F$ ,  $C_{OUT} = 10\mu F$ ,  $V_{SI} = 0V$ ,  $V_{EN} = +2.4V$ ,  $V_{OUT} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



## Pin Description

| PIN | NAME             | FUNCTION                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | $V_S$            | Regulator Input. Operating supply range is from +5V to +28V and withstands 40V transients. Bypass $V_S$ to GND with a $10\mu F$ capacitor.                                                                                                                                                                                      |
| 2   | SI               | Voltage Sense/Power-Fail Comparator Input. SI is the noninverting input of an uncommitted comparator. SO asserts low if $V_{SI}$ drops below the reference level, $V_{ST}$ .                                                                                                                                                    |
| 3   | EN               | Enable Input. Leave unconnected (or pull EN high) to turn on the regulator. Pull EN low to place the device in shutdown mode. EN is internally pulled up to 3.6V.                                                                                                                                                               |
| 4   | CT               | Reset Timeout Delay Capacitor Connection. Connect a capacitor from CT to GND to program the reset timeout period/reset pulse delay. During regulation, CT is pulled up to $V_{OUT}$ . CT is pulled low during reset, when EN is low, or when in thermal shutdown.                                                               |
| 5   | GND              | Ground. Bypass the input and output capacitors to the GND plane. Solder to large pads or the circuit-board ground plane to maximize thermal dissipation.                                                                                                                                                                        |
| 6   | $\overline{RES}$ | Active-Low Reset Output. Pull up externally to $V_{OUT}$ . Open-drain $\overline{RES}$ goes low when $V_{OUT}$ is below the reset threshold. Once output voltage is in regulation, $\overline{RES}$ goes high after the programmed reset timeout period is over. $\overline{RES}$ is low when EN is low or in thermal shutdown. |
| 7   | SO               | Voltage Sense/Power-Fail Comparator Output. Pull up externally to $V_{OUT}$ . Open-drain SO asserts low when $V_{SI}$ drops below the reference level, $V_{ST}$ . SO also asserts low when EN is low or in thermal shutdown.                                                                                                    |
| 8   | $V_{OUT}$        | Regulator Output. Fixed at +5V (MAX5091A) or +3.3V (MAX5091B). Bypass with a $10\mu F$ ceramic capacitor to GND.                                                                                                                                                                                                                |
| EP  | EP               | Exposed Paddle. EP is internally connected to GND. Connect EP to GND to provide a low thermal-resistance path from the IC junction to the PC board. Do not use as the only electrical connection to GND.                                                                                                                        |

# 28V, 100mA, Low-Quiescent-Current LDO with Reset and Power-Fail Input/Output

MAX5091

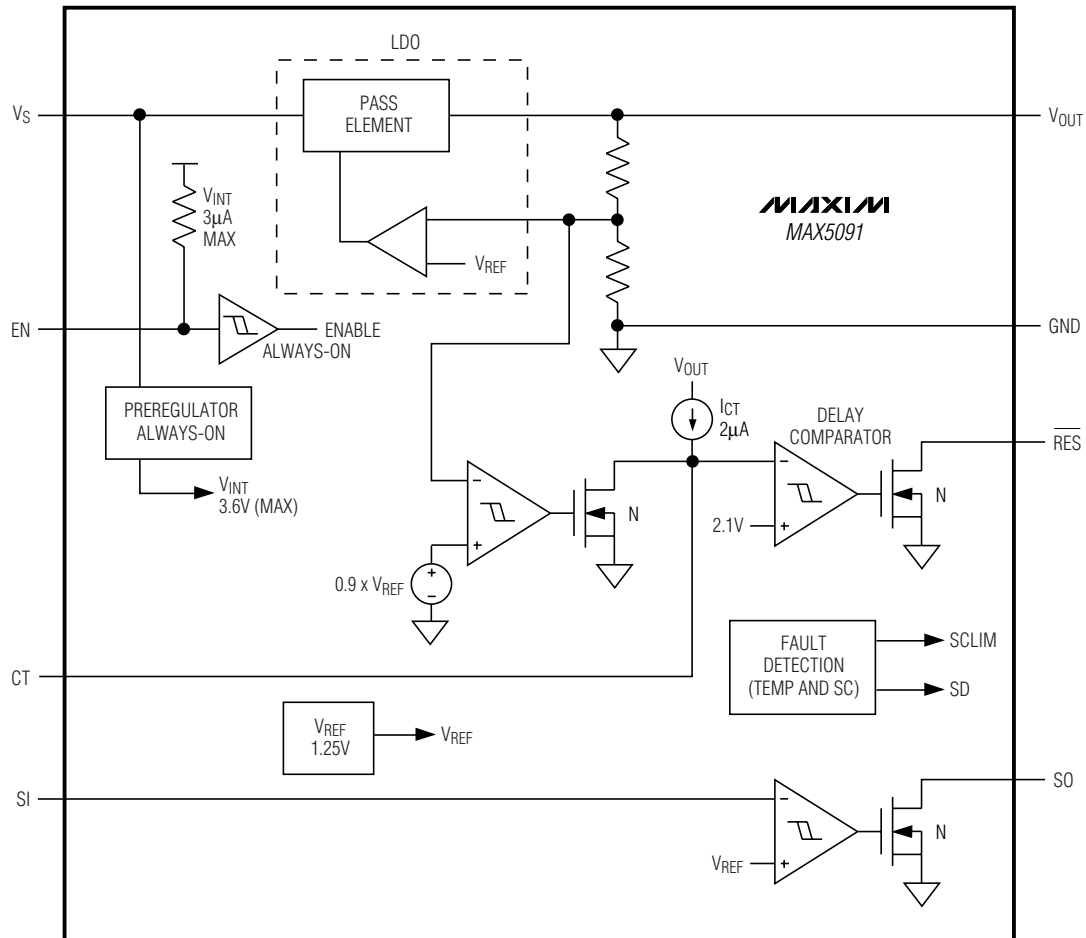


Figure 1. Functional Diagram

# 28V, 100mA, Low-Quiescent-Current LDO with Reset and Power-Fail Input/Output

## Detailed Description

### Regulator

The MAX5091 high-voltage, LDO regulator operates from +5V to +28V input voltage. The device withstands up to 40V transients, providing protection against temporary overvoltage conditions like load dump. The MAX5091 incorporates internal feedback resistors for factory-preset voltages of either +5V (MAX5091A) or +3.3V (MAX5091B). The regulator is capable of driving up to 100mA of load current and features a typical current limit of 260mA. The regulator uses a pnp pass element and provides low 0.5V dropout while delivering 100mA load current. The output of the regulator follows closely to the input during turn-on. See the Output Voltage vs. Input Voltage graph in the *Typical Operating Characteristics*. This makes the usable input voltage range for 3.3V and 5V output down to 3.7V and 5.5V, respectively. The MAX5091 is designed to operate with very low quiescent current during always-on operation when not in dropout. The regulator is stable with a wide variety of capacitors including low-ESR ceramic 10μF (0603 case size). The load-transient response curves depict the stability of the LDO when using different capacitance and ESR ranges. See the *Capacitor Selection and Regulator Stability* section in the *Applications Information*.

### Reset Output ( $\overline{\text{RES}}$ )

The MAX5091 integrates a power-on-reset circuit.  $\overline{\text{RES}}$  is an open-drain output that requires a pullup resistor to  $V_{\text{OUT}}$ . The open-drain MOSFET can sink up to 825μA current while keeping the  $\overline{\text{RES}}$  voltage below 0.4V. The internal reset circuit monitors the regulator output voltage and  $\overline{\text{RES}}$  asserts an active-low output when the regulator output falls below a reset threshold of typically  $0.9 \times V_{\text{OUT}}$ . The  $\overline{\text{RES}}$  output remains low when  $V_{\text{OUT}}$  is below the reset threshold, and remains low for the duration of the reset timeout period ( $t_{\text{RD}}$ ). The reset timeout period is programmable and can be set with an external capacitor connected from CT to ground. The duration of the delay as a function of CT is:

$$t_{\text{RD}} = \frac{C_{\text{CT}} \times V_{\text{CCTH}}}{I_{\text{CT}}} + (35 \times 10^{-6})$$

where  $V_{\text{CCTH}} = 2.1\text{V}$  and  $I_{\text{CT}} = 2 \times 10^{-6}\text{A}$ .

The default reset timeout period is 35μs when no capacitor is connected from CT to ground.

### SI/SO Comparator

The MAX5091 includes an uncommitted comparator for monitoring the input voltage or for detecting power-fail conditions. The input SI is the noninverting input of the comparator. The open-drain output SO asserts low when voltage at the input SI drops below the threshold voltage,  $V_{\text{ST}}$  (see Figure 1). The sense comparator typically has a hysteresis of 100mV. Use the following equation to calculate the resistor-divider for programming the trip voltage ( $V_{\text{TRIP}}$ ) during power-fail. See the *Typical Application Circuit*.

$$V_{\text{TRIP}} = \frac{(V_{\text{ST}} \times R_{\text{H}})}{R_{\text{L}}} + V_{\text{ST}}$$

where  $V_{\text{ST}} = 1.16\text{V}$  (typ). Choose  $R_{\text{L}}$  between 100kΩ to 300kΩ.

### Enable Input

The enable (EN) is a TTL-compatible logic input. Logic low at EN turns off the regulator and reduces the current consumption to 17μA (typ). It is internally pulled up to a logic-high voltage (3.6V max) by an internal resistor. Thus, the MAX5091 is enabled by default when  $V_{\text{S}}$  is applied and EN is left unconnected. The regulator, reset supervisor circuit, and the sense comparator can be manually shut down by pulling EN low. For shutdown operation, the pulldown network must be capable of sinking 3μA max, since the internal pullup resistor sets the maximum pullup current at 3μA. The external pulldown device should not leak more than 1μA current when it is in the off-state.

### Current Limit

The MAX5091 features a current limiter that monitors the output current and controls the pass transistor's gate voltage, limiting the output current to typically 260mA. The output can be continuously shorted to ground without damaging the device at  $V_{\text{S}} \leq 16\text{V}$ . Note that the output short-circuit current may increase the power dissipation significantly and raise the junction temperature to its thermal-shutdown threshold. In such a case, the MAX5091 is temporarily turned off.

### Thermal Shutdown

When the junction temperature exceeds  $T_{\text{J}} = +165^{\circ}\text{C}$  (typ), an internal thermal sensor signals the shutdown logic to turn off the pass transistor and allow the IC to cool. The thermal sensor turns the pass transistor on again after the IC's junction temperature cools by  $+20^{\circ}\text{C}$  (typ), resulting in a cycled output during continuous thermal-overload conditions. Thermal shutdown protects the MAX5091 in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature of  $T_{\text{J}} = +150^{\circ}\text{C}$ .

# 28V, 100mA, Low-Quiescent-Current LDO with Reset and Power-Fail Input/Output

## Applications Information

### Available Output Current Calculation

The MAX5091 high-voltage regulator provides up to 100mA of output current. The input voltage extends to +28V. Package power dissipation limits the amount of output current available for a given input/output voltage and ambient temperature. Figure 2 depicts the maximum power dissipation curve for the 8-pin SO-EP package. The graph assumes that the exposed metal back of the MAX5091 package is soldered to copper on a single layer PCB according to the JEDEC51 standard.

Use Figure 2 to determine the allowable package dissipation for a given ambient temperature. Alternately, use the following formula to calculate the allowable package dissipation:

$$P_D = \begin{cases} 1.538\text{W} & \text{For } T_A \leq +70^\circ\text{C} \\ 1.538 - 0.01923(T_A - 70^\circ\text{C}) & \text{For } +70^\circ\text{C} < T_A \leq +125^\circ\text{C} \end{cases}$$

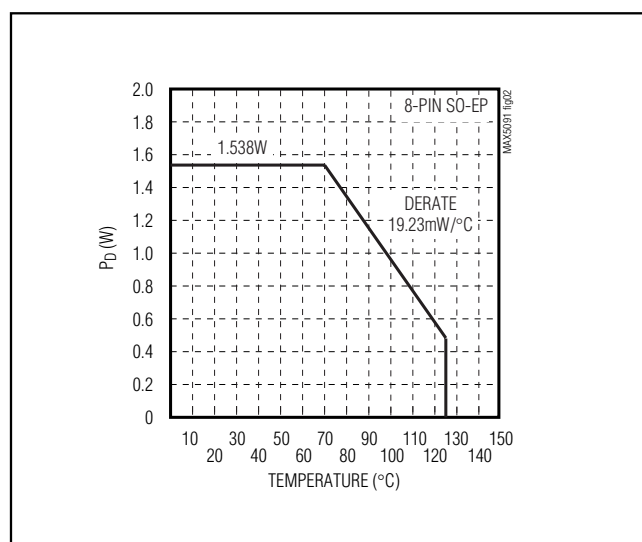


Figure 2. 8-Pin SO-EP Maximum Power Dissipation vs. Temperature

After determining the allowable package dissipation, calculate the maximum output current using the following formula:

$$I_{OUT(MAX)} \equiv \frac{P_D}{V_S - V_{OUT}}$$

The above equations do not include the power dissipation from self-heating due to the IC ground current.

The junction-to-ambient thermal impedance depends on the area of the copper plane, its thickness, and the number of copper layers on PCB. For the higher power dissipation requirement, use multiple-layered PCBs with 2oz copper and a large copper area.

### Capacitor Selection and Regulator Stability

For stable operation over the full temperature range and with load currents up to 100mA, use a 10μF output capacitor with a low ESR. Table 1 shows a list of recommended output capacitor ESR for various load conditions.

Table 1. Recommended Output Capacitor ESR

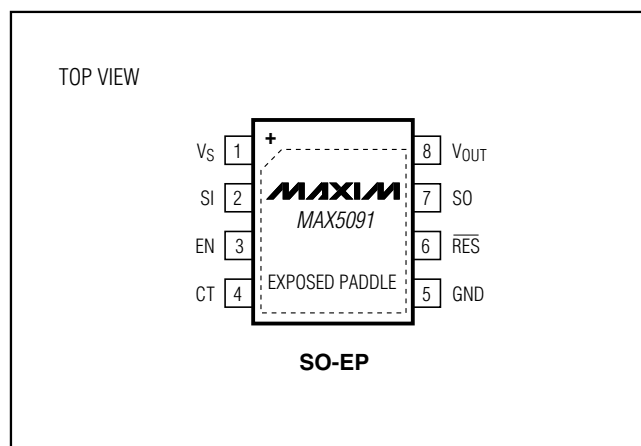
| RECOMMENDED C <sub>OUT</sub> ESR |                           |                         |
|----------------------------------|---------------------------|-------------------------|
| I <sub>OUT</sub>                 | V <sub>OUT</sub> = 3.3V   | V <sub>OUT</sub> = 5.0V |
| I <sub>OUT</sub> ≤ 10mA          | C <sub>ESR</sub> < 0.66Ω  | C <sub>ESR</sub> < 1Ω   |
| I <sub>OUT</sub> ≤ 50mA          | C <sub>ESR</sub> < 0.132Ω | C <sub>ESR</sub> < 0.2Ω |
| I <sub>OUT</sub> ≤ 100mA         | C <sub>ESR</sub> < 66mΩ   | C <sub>ESR</sub> < 0.1Ω |

# 28V, 100mA, Low-Quiescent-Current LDO with Reset and Power-Fail Input/Output

## Pin Configurations (continued)

## Chip Information

PROCESS: BiCMOS



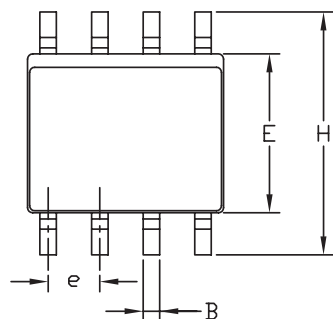
# 28V, 100mA, Low-Quiescent-Current LDO with Reset and Power-Fail Input/Output

## Package Information

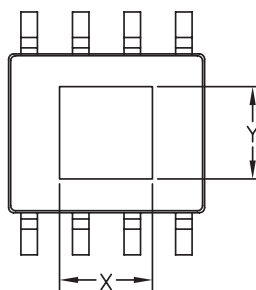
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX5091

8L, SOIC EXP. PADS



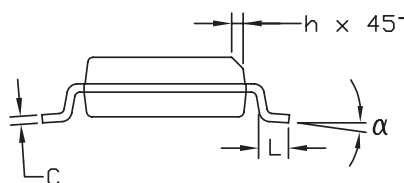
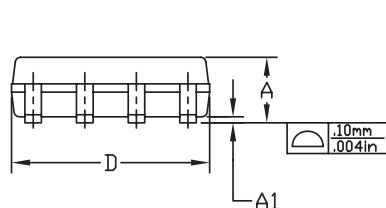
TOP VIEW



BOTTOM VIEW

| DIM | INCHES |       | MILLIMETERS |      |
|-----|--------|-------|-------------|------|
|     | MIN    | MAX   | MIN         | MAX  |
| A   | 0.056  | 0.066 | 1.43        | 1.68 |
| A1  | 0.000  | 0.004 | 0.00        | 0.10 |
| B   | 0.014  | 0.019 | 0.35        | 0.49 |
| C   | 0.007  | 0.010 | 0.19        | 0.25 |
| D   | 0.189  | 0.196 | 4.80        | 4.98 |
| e   | 0.050  | BSC   | 1.27        | BSC  |
| E   | 0.150  | 0.157 | 3.81        | 3.99 |
| H   | 0.230  | 0.244 | 5.81        | 6.20 |
| h   | 0.010  | 0.016 | 0.25        | 0.41 |
| L   | 0.016  | 0.035 | 0.41        | 0.89 |
| α   | 0°     | 8°    | 0°          | 8°   |

| PKG.   | X (mm) |       | Y (mm) |       |
|--------|--------|-------|--------|-------|
|        | MIN    | MAX   | MIN    | MAX   |
| S8E-12 | 2.184  | 2.388 | 2.184  | 2.388 |
| S8E-14 | 2.997  | 3.200 | 2.311  | 2.515 |



### NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 EXCEPT DIMENSION A1.
5. DIMENSIONS X AND Y DEFINE EXPOSED PAD METAL AREA.

|                                                                                                                      |                                 |                                                                                       |     |
|----------------------------------------------------------------------------------------------------------------------|---------------------------------|---------------------------------------------------------------------------------------|-----|
|  <b>DALLAS</b><br>SEMICONDUCTOR |                                 |  |     |
| PROPRIETARY INFORMATION                                                                                              |                                 |                                                                                       |     |
| TITLE: PACKAGE OUTLINE<br>8L SOIC, .150" EXPOSED PAD                                                                 |                                 |                                                                                       |     |
| APPROVAL                                                                                                             | DOCUMENT CONTROL NO.<br>21-0111 | REV.<br>C                                                                             | 1/1 |

# MAX5091

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



# 28V, 100mA, Low-Quiescent-Current LDO with Reset and Power-Fail Input/Output

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

| COMMON DIMENSIONS |           |      |
|-------------------|-----------|------|
| SYMBOL            | MIN.      | MAX. |
| A                 | 0.70      | 0.80 |
| D                 | 2.90      | 3.10 |
| E                 | 2.90      | 3.10 |
| A1                | 0.00      | 0.05 |
| L                 | 0.20      | 0.40 |
| k                 | 0.25 MIN. |      |
| A2                | 0.20 REF. |      |

| PACKAGE VARIATIONS |    |           |           |          |                |           |               |  |
|--------------------|----|-----------|-----------|----------|----------------|-----------|---------------|--|
| PKG. CODE          | N  | D2        | E2        | e        | JEDEC SPEC     | b         | [(N/2)-1] x e |  |
| T633-1             | 6  | 1.50±0.10 | 2.30±0.10 | 0.95 BSC | MO229 / WEEA   | 0.40±0.05 | 1.90 REF      |  |
| T633-2             | 6  | 1.50±0.10 | 2.30±0.10 | 0.95 BSC | MO229 / WEEA   | 0.40±0.05 | 1.90 REF      |  |
| T833-1             | 8  | 1.50±0.10 | 2.30±0.10 | 0.65 BSC | MO229 / WEEC   | 0.30±0.05 | 1.95 REF      |  |
| T833-2             | 8  | 1.50±0.10 | 2.30±0.10 | 0.65 BSC | MO229 / WEEC   | 0.30±0.05 | 1.95 REF      |  |
| T833-3             | 8  | 1.50±0.10 | 2.30±0.10 | 0.65 BSC | MO229 / WEEC   | 0.30±0.05 | 1.95 REF      |  |
| T1033-1            | 10 | 1.50±0.10 | 2.30±0.10 | 0.50 BSC | MO229 / WEED-3 | 0.25±0.05 | 2.00 REF      |  |
| T1033-2            | 10 | 1.50±0.10 | 2.30±0.10 | 0.50 BSC | MO229 / WEED-3 | 0.25±0.05 | 2.00 REF      |  |
| T1433-1            | 14 | 1.70±0.10 | 2.30±0.10 | 0.40 BSC | ----           | 0.20±0.05 | 2.40 REF      |  |
| T1433-2            | 14 | 1.70±0.10 | 2.30±0.10 | 0.40 BSC | ----           | 0.20±0.05 | 2.40 REF      |  |

### NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

 MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

|                                                                                       |                                        |                      |
|---------------------------------------------------------------------------------------|----------------------------------------|----------------------|
|  |                                        |                      |
| <b>TITLE:</b> PACKAGE OUTLINE, 6,8,10 & 14L,<br>TDFN, EXPOSED PAD, 3x3x0.80 mm        |                                        |                      |
| <b>APPROVAL</b>                                                                       | <b>DOCUMENT CONTROL NO.</b><br>21-0137 | <b>REV.</b><br>H 2/2 |

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 15