

Automotive-grade N-channel 250 V, 0.14 Ω , 17 A low gate charge STripFET™ II Power MOSFET in D²PAK and DPAK packages

Datasheet - production data

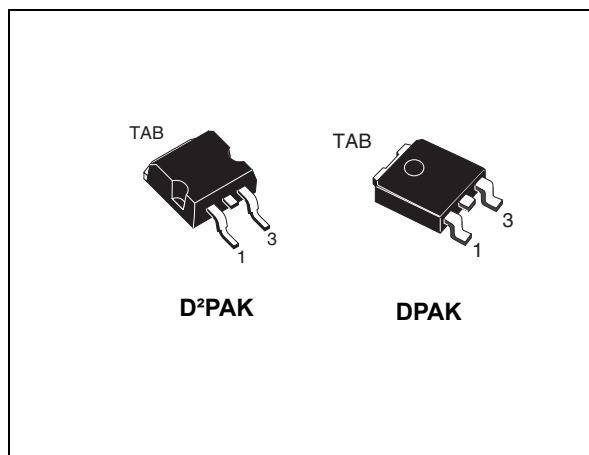
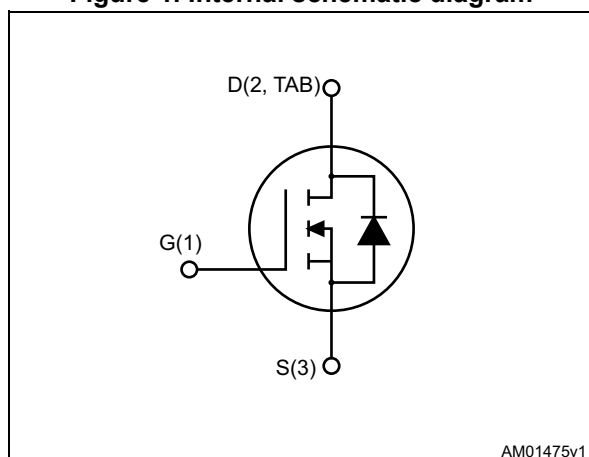


Figure 1. Internal schematic diagram



Features

Type	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STB18NF25	250 V	0.165 Ω	17 A	110 W
STD18NF25	250 V	0.165 Ω	17 A	110 W

- Designed for automotive applications and AEC-Q101 qualified
- Low gate charge
- 100% avalanche tested
- Exceptional dv/dt capability

Application

- Switching applications

Description

These Power MOSFETs have been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the devices suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Table 1. Device summary

Order code	Marking	Package	Packing
STB18NF25	18NF25	D ² PAK	Tape and reel
STD18NF25	18NF25	DPAK	Tape and reel

Contents

1 **Electrical ratings** 3

2 **Electrical characteristics** 4

 2.1 Electrical characteristics (curves) 6

3 **Test circuits** 9

4 **Package information** 10

 4.1 D²PAK (TO-263) package information 10

 4.2 DPAK (TO-252) package information 13

 4.3 Packing information 16

5 **Revision history** 19



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	250	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	17	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	12	A
$I_{DM}^{(1)}$	Drain current (pulsed)	68	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	10	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 17\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq 80\%V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK	DPAK	
$R_{thj-case}$	Thermal resistance junction-case max	1.36		$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	30	50	$^{\circ}\text{C}/\text{W}$

1. When mounted on 1inch² FR-4, 2 Oz copper board.

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	17	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	170	mJ

2 Electrical characteristics

($T_{CASE}=25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	250			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 250\text{ V},$			1	μA
		$V_{GS} = 0$ $V_{DS} = 250\text{ V}, T_C = 125\text{ }^{\circ}\text{C}$			10	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0, V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 8.5\text{ A}$		0.14	0.165	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}, I_D = 8.5\text{ A}$	-	14	-	S
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	1000	-	pF
C_{oss}	Output capacitance			178		pF
C_{rss}	Reverse transfer capacitance			28		pF
$C_{o(tr)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }200\text{ V}, V_{GS} = 0$	-	106	-	pF
$C_{o(er)}$	Equivalent capacitance energy related		-	79	-	pF
Q_g	Total gate charge	$V_{DD} = 200\text{ V}, I_D = 17\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 17)	-	29.5	-	nC
Q_{gs}	Gate-source charge			4.8		nC
Q_{gd}	Gate-drain charge			15.6		nC
R_G	Gate input resistance	$f = 1\text{ MHz}$ gate DC bias = 0 test signal level = 20 mV open drain	-	2	-	Ω

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 125\text{ V}$, $I_D = 8.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16)	-	8.8	-	ns
t_r	Rise time			17.2		ns
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 125\text{ V}$, $I_D = 8.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16)	-	21	-	ns
t_f	Fall time			8.8		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 50\text{ V}$ (see Figure 18)	-	157		ns
Q_{rr}	Reverse recovery charge			0.91		μC
I_{RRM}	Reverse recovery current			11.6		A
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 50\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 18)	-	196		ns
Q_{rr}	Reverse recovery charge			1.34		μC
I_{RRM}	Reverse recovery current			13.7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

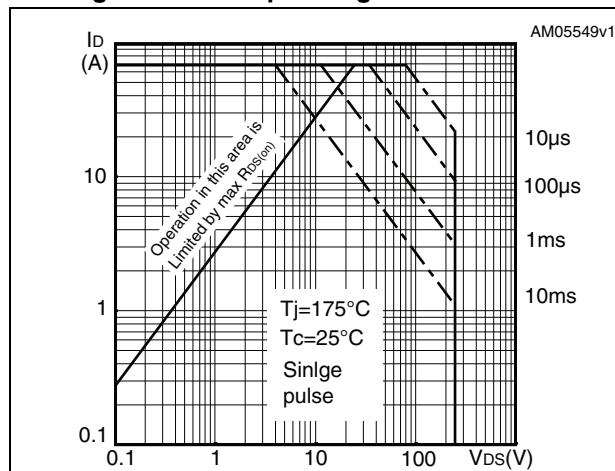
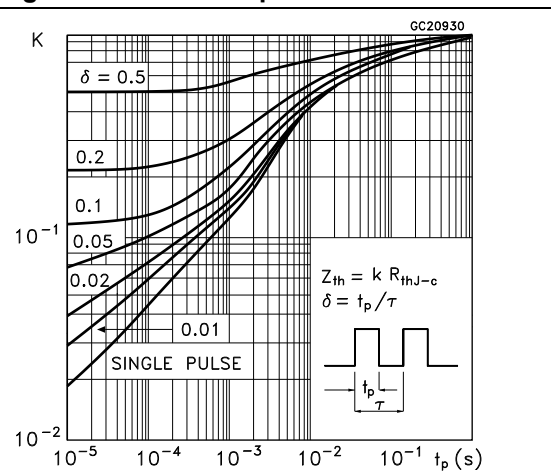
Figure 2. Safe operating area for D²PAKFigure 3. Thermal impedance for D²PAK

Figure 4. Safe operating area for DPAK

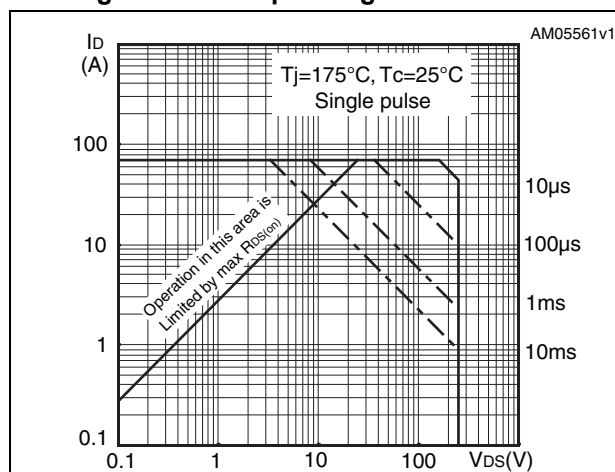


Figure 5. Thermal impedance for DPAK

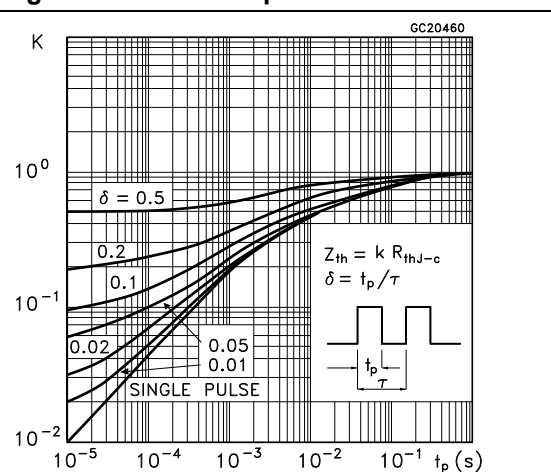


Figure 6. Output characteristics

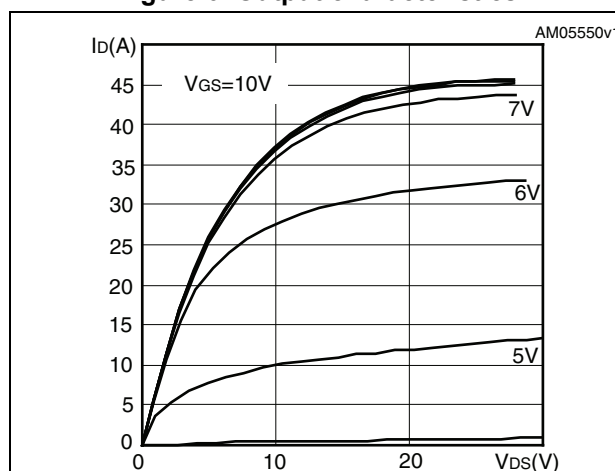


Figure 7. Transfer characteristics

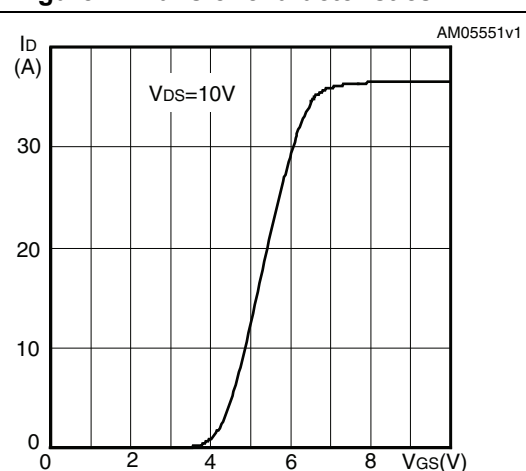


Figure 8. Gate charge vs gate-source voltage

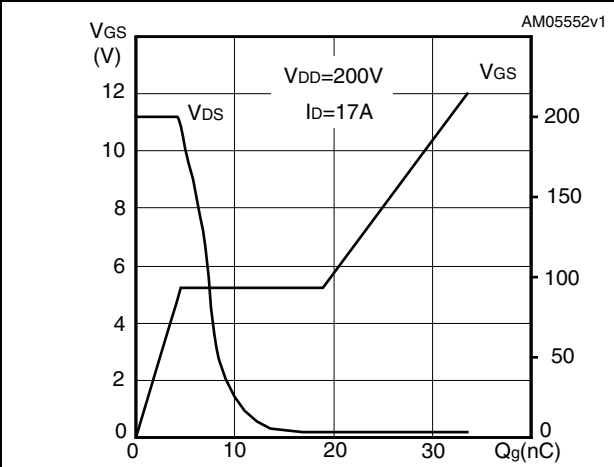


Figure 9. Static drain-source on-resistance

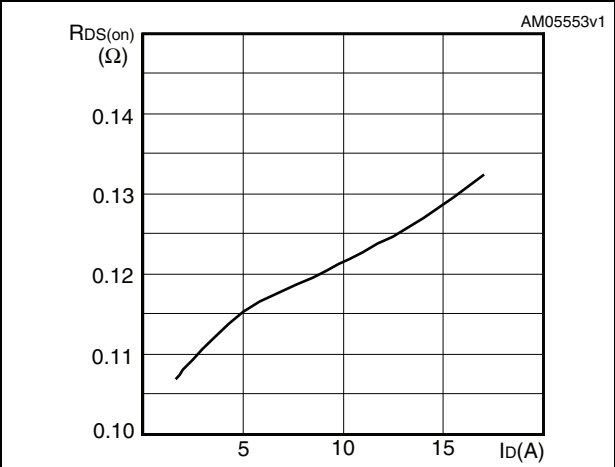


Figure 10. Output capacitance stored energy

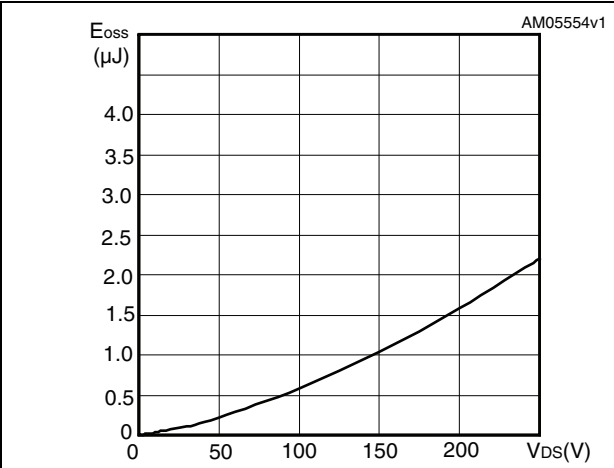


Figure 11. Capacitance variations

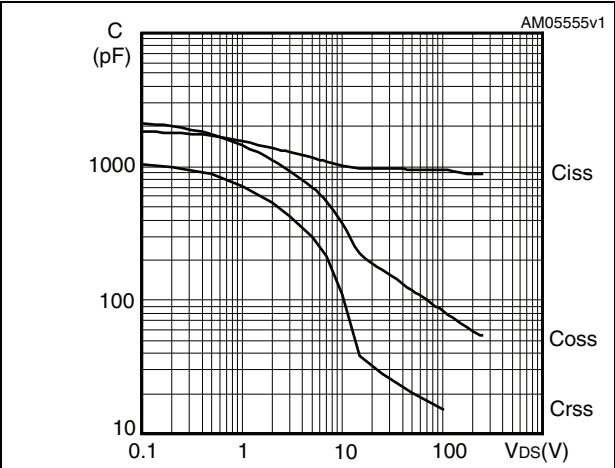


Figure 12. Normalized gate threshold voltage vs temperature

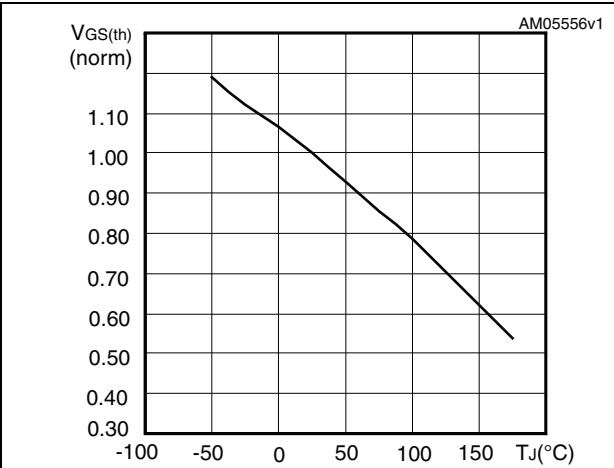


Figure 13. Normalized on resistance vs temperature

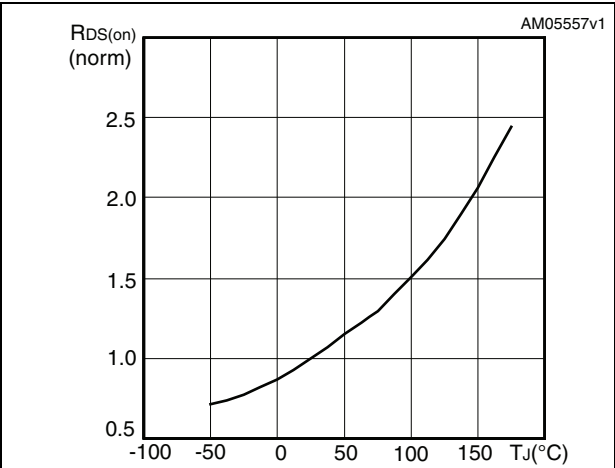


Figure 14. Source-drain diode forward characteristics

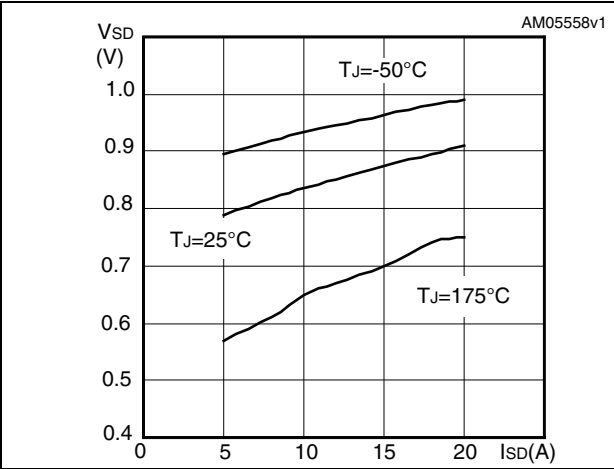
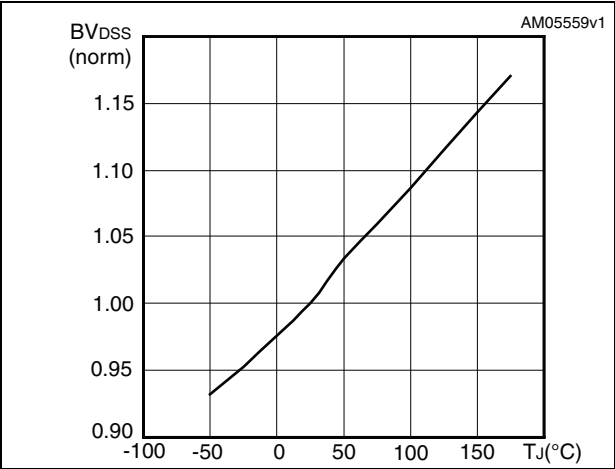


Figure 15. Normalized $B_{V_{DS}}$ vs temperature



3 Test circuits

Figure 16. Switching times test circuit for resistive load

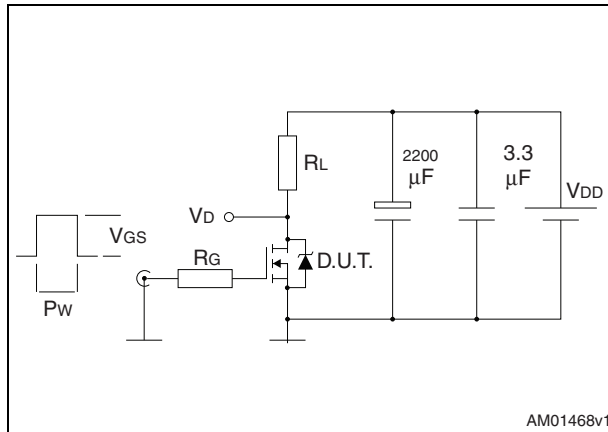


Figure 17. Gate charge test circuit

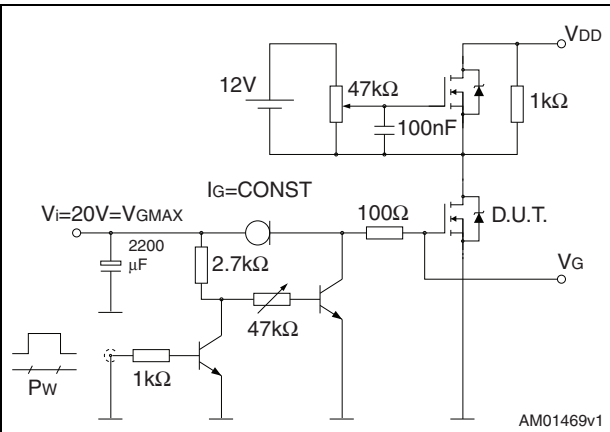


Figure 18. Test circuit for inductive load switching and diode recovery times

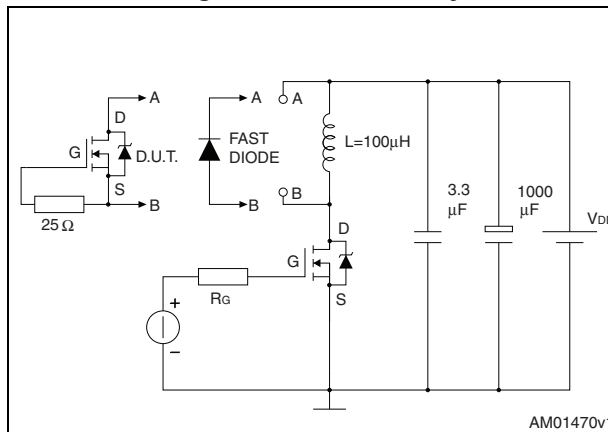


Figure 19. Unclamped inductive load test circuit

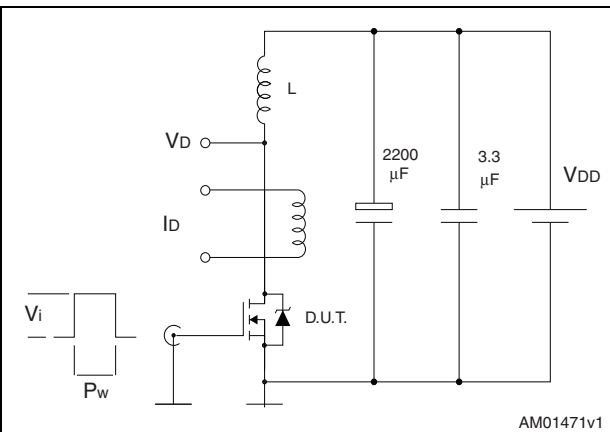


Figure 20. Unclamped inductive waveform

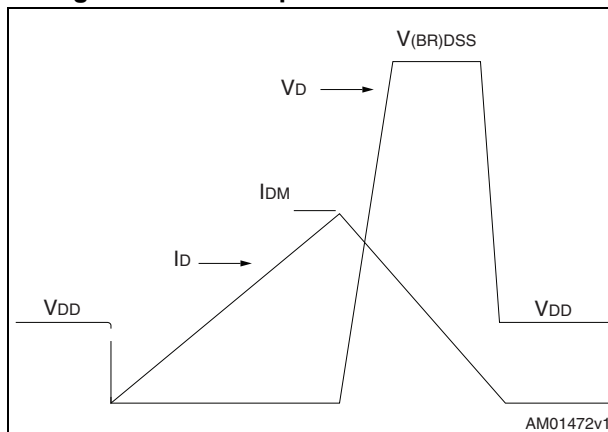
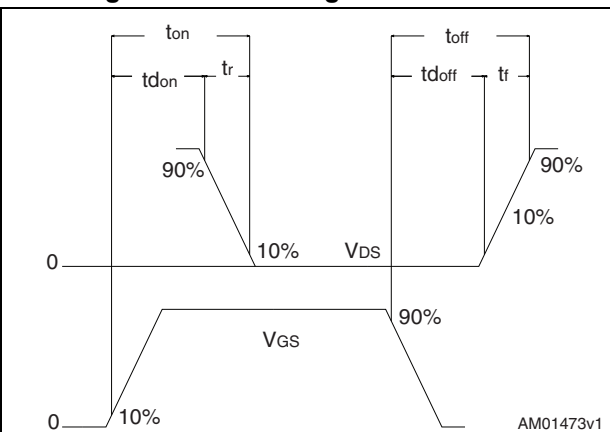


Figure 21. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) package information

Figure 22. D²PAK (TO-263) type A package outline

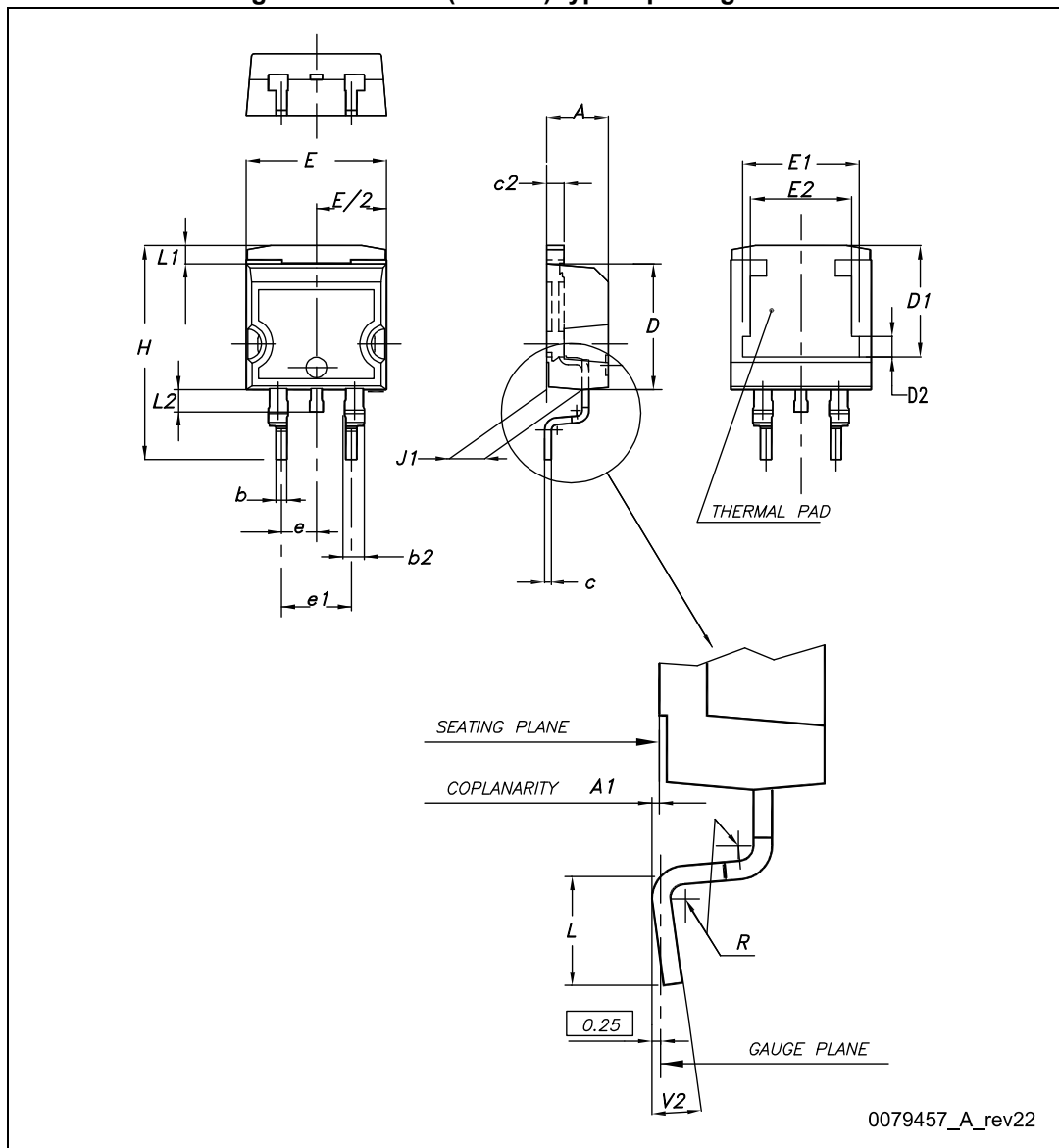
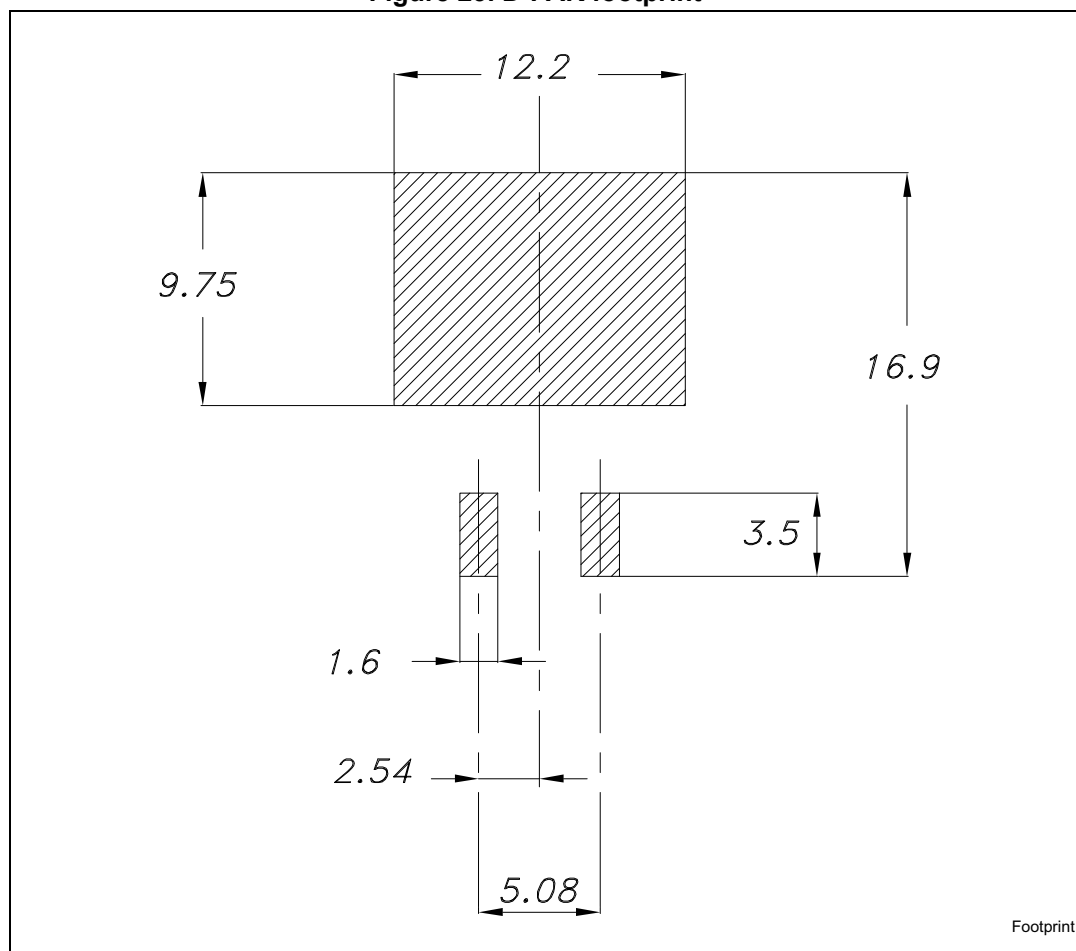


Table 9. D²PAK (TO-263) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D²PAK footprint^(a)

a. All dimensions are in millimeters

4.2 DPAK (TO-252) package information

Figure 24. DPAK (TO-252) type A package outline

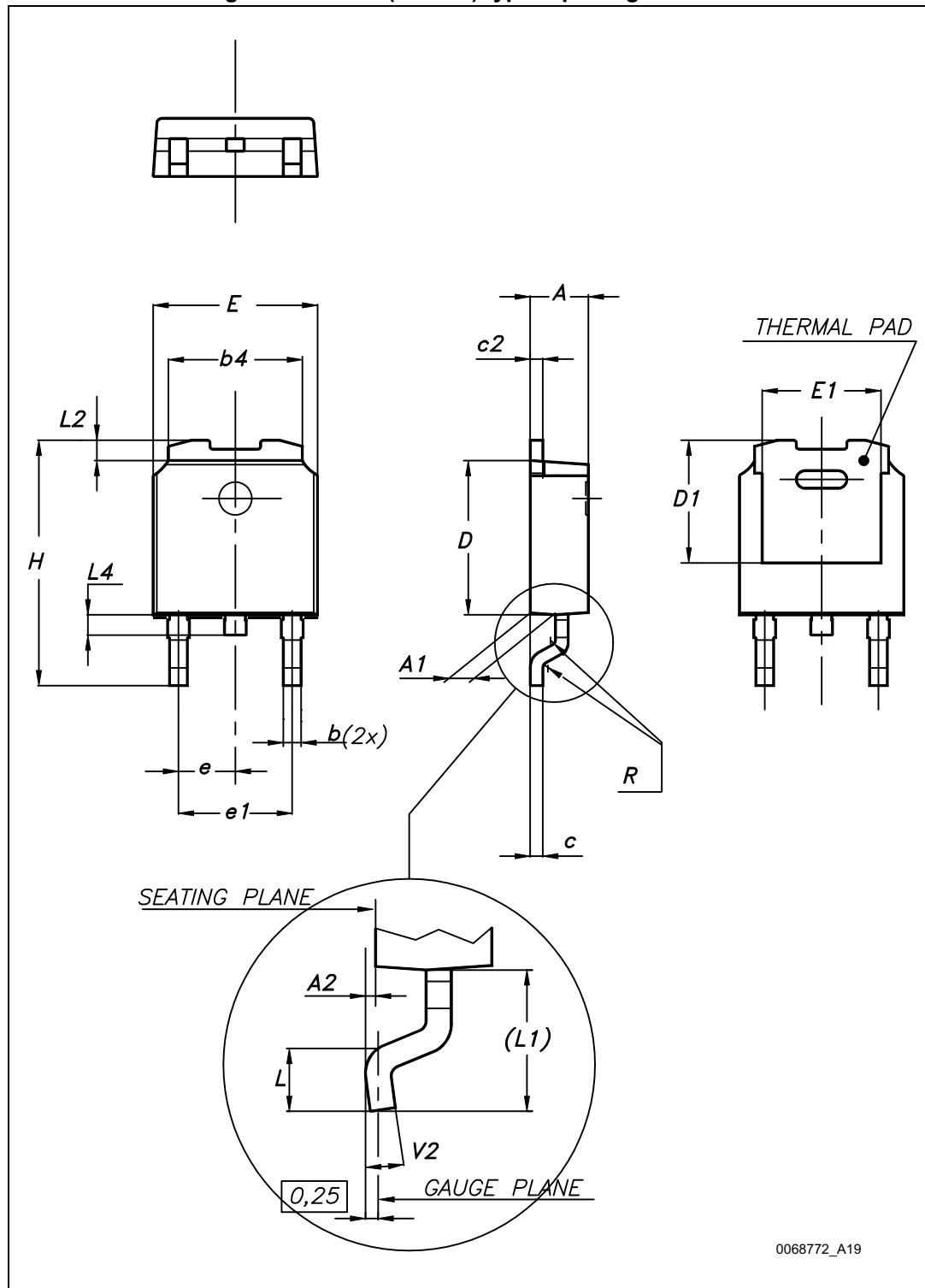
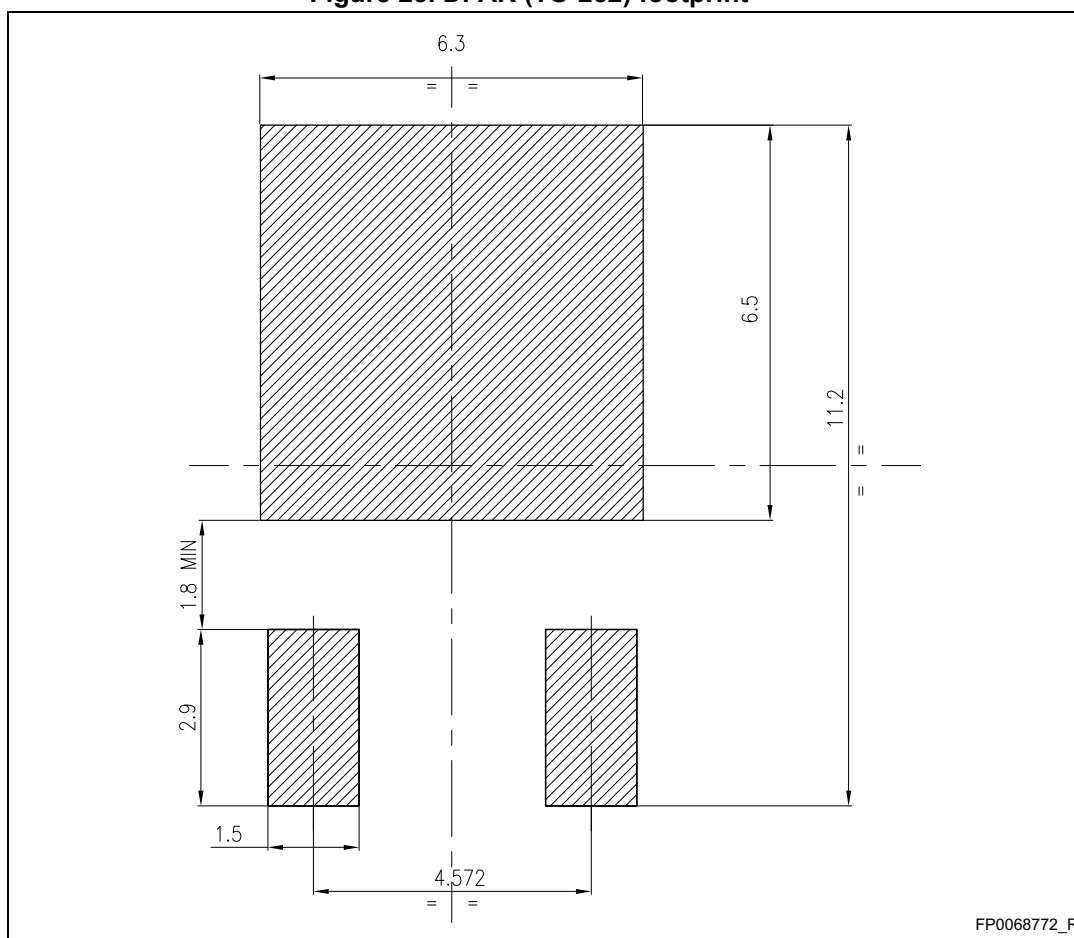


Table 10. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) footprint (b)



b. All dimensions are in millimeters

4.3 Packing information

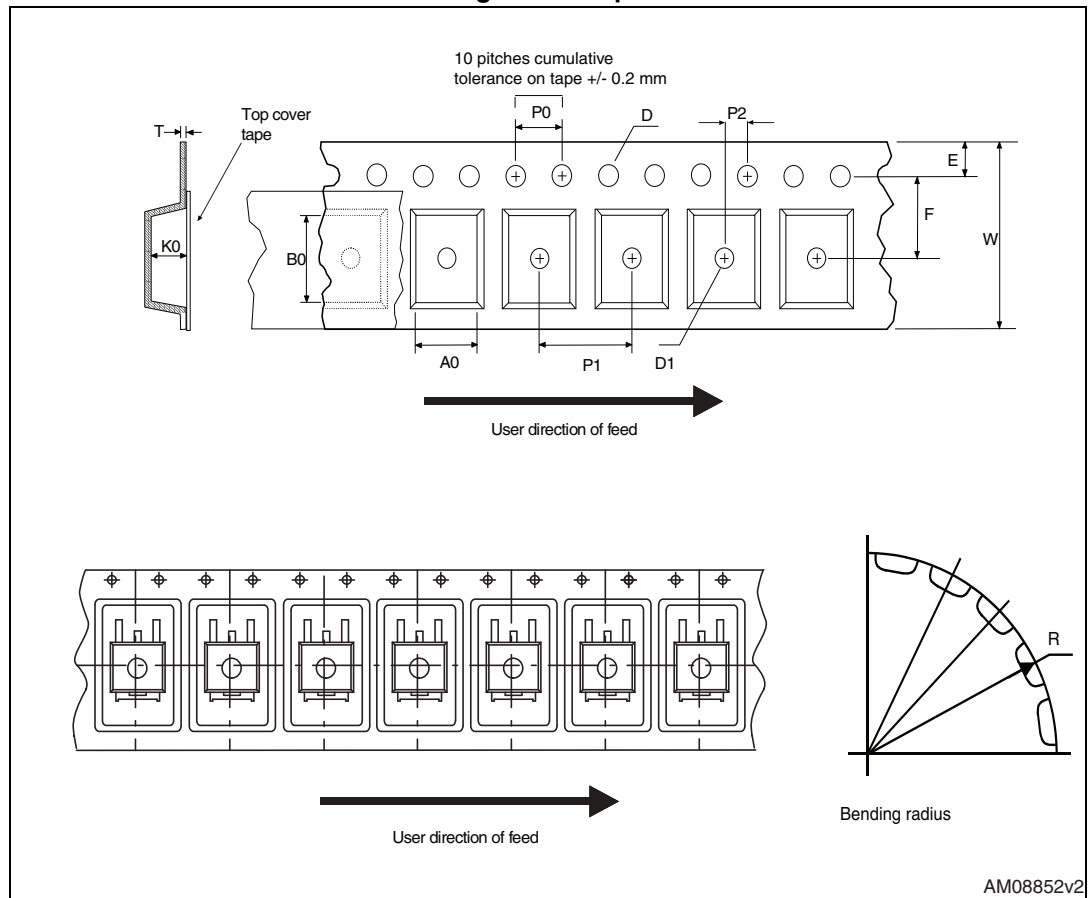
Figure 26. Tape

Figure 27. Reel

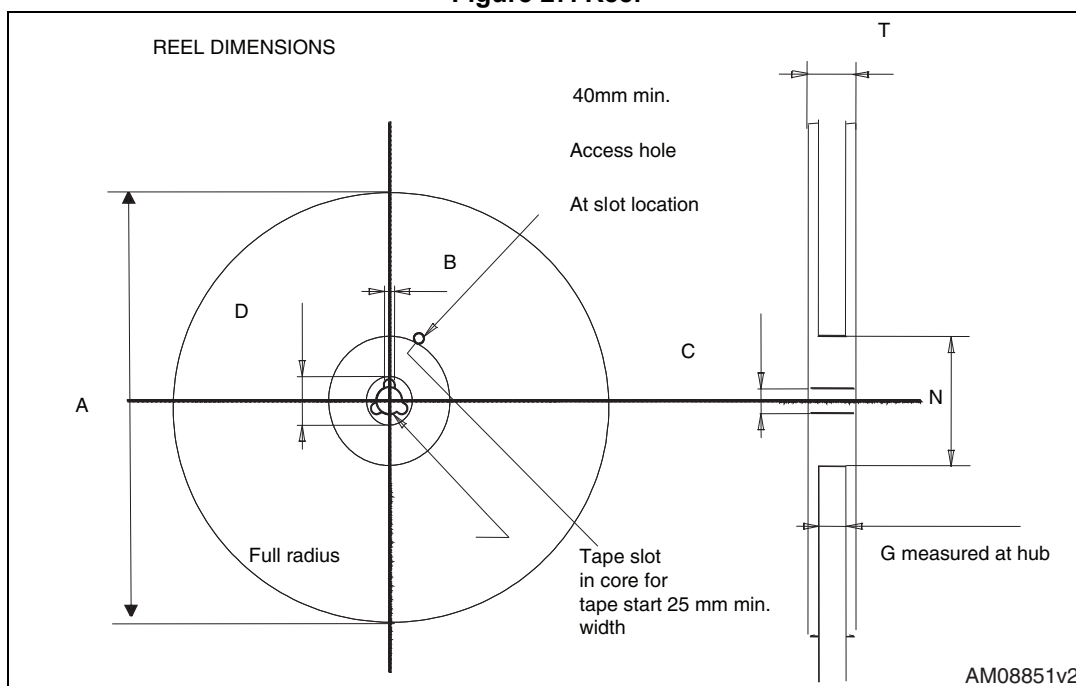


Table 11. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 13. Document revision history

Date	Revision	Changes
16-Nov-2009	1	First release
19-Feb-2010	2	V _{DS} value in Table 8 has been corrected.
26-Apr-2012	3	Updated E _{AS} in Table 4: Avalanche data , Section 4: Package information and Section 4.3: Packing information . Minor text changes.
10-Sep-2015	4	Updated 4.2: DPAK (TO-252) package information Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved