

OPAx355 200-MHz CMOS Operational Amplifiers With Shutdown

1 Features

- Unity-Gain Bandwidth: 450 MHz
- Wide Bandwidth: 200 MHz GBW
- Low Noise: 5.8 nV/ $\sqrt{\text{Hz}}$
- Excellent Video Performance
 - Differential Gain: 0.02%
 - Differential Phase: 0.05°
 - 0.1-dB Gain Flatness: 75 MHz
- Input Range Includes Ground
- Rail-to-Rail Output (within 100 mV)
- Low Input Bias Current: 3 pA
- Low Shutdown Current: 3.4 μA
- Enable and Disable Time: 100 ns and 30 ns
- Thermal Shutdown
- Single-Supply Operating Range: 2.5 V to 5.5 V
- MicroSIZE Packages

2 Applications

- Video Processing
- Ultrasound
- Optical Networking, Tunable Lasers
- Photodiode Transimpedance Amplifiers
- Active Filters
- High-Speed Integrators
- Analog-to-Digital Converter (ADC) Input Buffers
- Digital-to-Analog Converter (DAC) Output Amplifiers
- Barcode Scanners
- Communications

3 Description

The OPA355 series of high-speed, voltage-feedback CMOS operational amplifiers are designed for video and other applications requiring wide bandwidth. The OPA355 series is unity-gain stable and can drive large output currents. In addition, the OPAx355 series has a digital shutdown (enable) function. This feature provides power saving during idle periods and places the output in a high-impedance state to support output multiplexing. The differential gain is 0.02% and the differential phase is 0.05°. The quiescent current is 8.3 mA per channel.

The OPAx355 series is optimized for operation on single supply or dual supplies as low as 2.5 V (± 1.25 V) and up to 5.5 V (± 2.75 V). The common-mode input range for the OPAx355 series extends 100 mV below ground and up to 1.5 V from V+. The output swing is within 100 mV of the rails, supporting wide dynamic range.

The OPAx355 series is available in single (SOT-23-6 and SO-8), dual (VSSOP-10), and triple (TSSOP-14 and SO-14) versions. Multichannel versions feature completely independent circuitry for lowest crosstalk and freedom from interaction. All packages are specified from -40°C to $+125^{\circ}\text{C}$.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|--------------------------|
| OPA355 | SOIC (8) | 4.90 mm \times 3.91 mm |
| | SOT-23 (6) | 2.90 mm \times 1.60 mm |
| OPA2355 | VSSOP (10) | 3.00 mm \times 3.00 mm |
| OPA3355 | SOIC (14) | 8.65 mm \times 3.91 mm |
| | TSSOP (14) | 5.00 mm \times 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

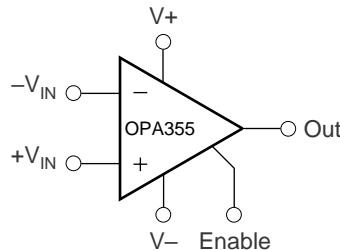


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4 Revision History

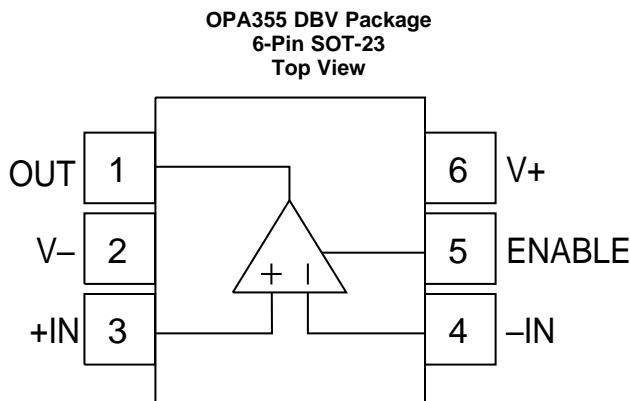
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision D (January 2004) to Revision E | Page |
|---|------|
| • Updated data sheet to latest TIS documentation and translation standards | 1 |
| • Changed pin type typo from MSOP to VSSOP in <i>Description</i> section | 1 |
| • Added <i>Device Information</i> table | 1 |
| • Deleted the <i>Absolute Maximum Ratings</i> table note: Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less. | 7 |
| • Added <i>ESD Ratings</i> table | 7 |
| • Added <i>Recommended Operating Conditions</i> table | 7 |
| • Added <i>Thermal Information</i> tables | 8 |
| • Changed pin type typo from MSOP to VSSOP in <i>Electrical Characteristics</i> section | 10 |
| • Deleted the test conditions statement from <i>Typical Characteristics</i> graphs and moved the conditions to tablenotes below the graphs | 11 |
| • Added <i>Detailed Description</i> section | 16 |
| • Added <i>Functional Block Diagram</i> graphic | 16 |
| • Deleted <i>Input and ESD Protection</i> section | 16 |
| • Added <i>Application and Implementation</i> section | 18 |
| • Deleted <i>Internal ESD Protection</i> application | 18 |
| • Added <i>Power Supply Recommendations</i> section | 25 |
| • Added <i>Layout Guidelines</i> section | 25 |

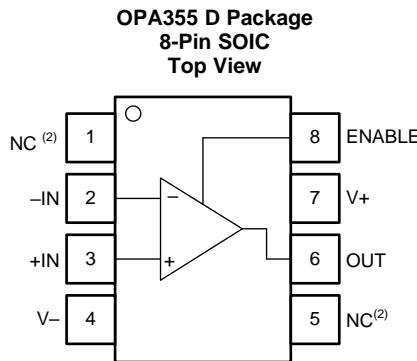
5 Device Comparison Table

| OPAx355 RELATED PRODUCTS | FEATURES |
|--------------------------|---|
| OPA356 | 200-MHz, Rail-to-Rail Output, CMOS, No Shutdown |
| OPAx350 | 38-MHz, Rail-to-Rail Input and Output, CMOS |
| OPAx631 | 75-MHz, Rail-to-Rail Output |
| OPAx634 | 150-MHz, Rail-to-Rail Output |
| THS412x | Differential Input and Output, 3.3-V Supply |

6 Pin Configuration and Functions



(1) Pin 1 of the SOT-23-6 is determined by orienting the package marking as indicated in the diagram.

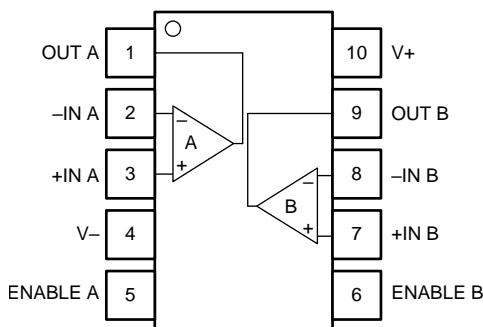


(1) Pin 1 of the SOT-23-6 is determined by orienting the package marking as indicated in the diagram.
 (2) NC - no internal connection

Pin Functions: OPA355

| PIN | | | I/O | DESCRIPTION |
|--------|--------|------|-----|---|
| NAME | SOT-23 | SOIC | | |
| ENABLE | 5 | 8 | — | Amplifier power down. Low = disabled, high = normal operation (pin must be driven) |
| IN+ | 3 | 3 | I | Noninverting input pin |
| IN- | 4 | 2 | I | Inverting input pin |
| NC | — | 1,5 | — | Do not connect. |
| OUT | 1 | 6 | O | Output pin |
| V+ | 6 | 7 | — | Positive power supply |
| V- | 2 | 4 | — | Negative power supply |

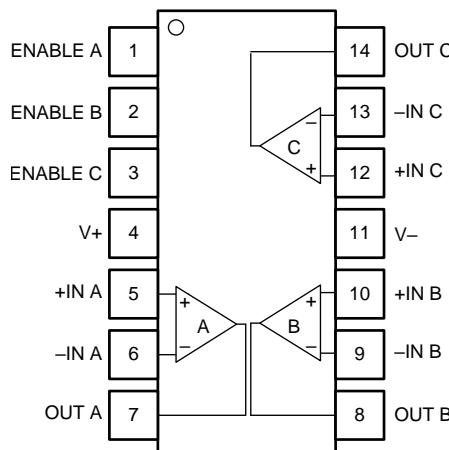
**OPA2355 DGS Package
10-Pin VSSOP
Top View**



Pin Functions: OPA2355

| PIN | | I/O | DESCRIPTION |
|----------|-----|-----|--|
| NAME | NO. | | |
| ENABLE A | 5 | — | Amplifier power down, channel A. Low = disabled, high = normal operation (pin must be driven) |
| ENABLE B | 6 | — | Amplifier power down, channel B. Low = disabled, high = normal operation (pin must be driven) |
| +IN A | 3 | I | Noninverting input pin, channel A |
| +IN B | 7 | I | Noninverting input pin, channel B |
| -IN A | 2 | I | Inverting input pin, channel A |
| -IN B | 8 | I | Inverting input pin, channel B |
| OUT A | 1 | O | Output pin, channel A |
| OUT B | 9 | O | Output pin, channel B |
| V+ | 10 | — | Positive power supply |
| V- | 4 | — | Negative power supply |

OPA3355 D and PW Packages
14-Pin SOIC, TSSOP
Top View



Pin Functions: OPA3355

| PIN | | I/O | DESCRIPTION |
|----------|-----|-----|--|
| NAME | NO. | | |
| ENABLE A | 1 | — | Amplifier power down, channel A. Low = disabled, high = normal operation (pin must be driven) |
| ENABLE B | 2 | — | Amplifier power down, channel B. Low = disabled, high = normal operation (pin must be driven) |
| ENABLE C | 3 | — | Amplifier power down, channel C. Low = disabled, high = normal operation (pin must be driven) |
| +IN A | 5 | I | Noninverting input pin, channel A |
| +IN B | 10 | I | Noninverting input pin, channel B |
| +IN C | 12 | I | Noninverting input pin, channel C |
| -IN A | 6 | I | Inverting input pin, channel A |
| -IN B | 9 | I | Inverting input pin, channel B |
| -IN C | 13 | I | Inverting input pin, channel C |
| OUT A | 7 | O | Output, channel A |
| OUT B | 8 | O | Output channel B |
| OUT C | 14 | O | Output, channel C |
| V+ | 4 | — | Positive power supply |
| V- | 11 | — | Negative power supply |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|---|------------|------------|------------|------|
| Supply voltage | V+ to V- | | 7.5 | V |
| Signal input terminals | Voltage | (V-) – 0.5 | (V+) + 0.5 | V |
| | Current | 10 | | mA |
| Output short circuit ⁽²⁾ | Continuous | | | |
| Operating temperature | | -55 | 150 | °C |
| Junction temperature | | | 160 | °C |
| Lead temperature (soldering, 10 seconds) | | | 300 | °C |
| Storage temperature range, T _{stg} | | -65 | 150 | °C |

(1) Stresses above *Absolute Maximum Ratings* may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|--|-------|------|
| V _(ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±250 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|-------------------------------------|-----|-----|-----|------|
| V _S Total supply voltage | 2.7 | | 5.5 | V |
| T _A Ambient temperature | -40 | 25 | 125 | °C |

7.4 Thermal Information: OPA355

| THERMAL METRIC ⁽¹⁾ | OPA355 | | UNIT |
|--|----------|--------------|------|
| | D (SOIC) | DBV (SOT-23) | |
| | 8 PINS | 6 PINS | |
| R _{θJA} Junction-to-ambient thermal resistance | 136.3 | 166.1 | °C/W |
| R _{θJC(top)} Junction-to-case (top) thermal resistance | 76.7 | 104.3 | °C/W |
| R _{θJB} Junction-to-board thermal resistance | 79.8 | 38.7 | °C/W |
| Ψ _{JT} Junction-to-top characterization parameter | 26.3 | 23.4 | °C/W |
| Ψ _{JB} Junction-to-board characterization parameter | 79 | 38.5 | °C/W |
| R _{θJC(bot)} Junction-to-case (bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Thermal Information: OPA2355

| THERMAL METRIC ⁽¹⁾ | OPA2355 | | UNIT |
|--|-------------|---------|------|
| | DGS (VSSOP) | 10 PINS | |
| | 10 PINS | 10 PINS | |
| R _{θJA} Junction-to-ambient thermal resistance | 171.1 | — | °C/W |
| R _{θJC(top)} Junction-to-case (top) thermal resistance | 58 | — | °C/W |
| R _{θJB} Junction-to-board thermal resistance | 92.9 | — | °C/W |
| Ψ _{JT} Junction-to-top characterization parameter | 6.7 | — | °C/W |
| Ψ _{JB} Junction-to-board characterization parameter | 91.2 | — | °C/W |
| R _{θJC(bot)} Junction-to-case (bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.6 Thermal Information: OPA3355

| THERMAL METRIC ⁽¹⁾ | OPA3355 | | UNIT |
|--|----------|------------|------|
| | D (SOIC) | PW (TSSOP) | |
| | 14 PINS | 14 PINS | |
| R _{θJA} Junction-to-ambient thermal resistance | 85.3 | 113.3 | °C/W |
| R _{θJC(top)} Junction-to-case (top) thermal resistance | 41.4 | 38 | °C/W |
| R _{θJB} Junction-to-board thermal resistance | 41.5 | 58.1 | °C/W |
| Ψ _{JT} Junction-to-top characterization parameter | 8.3 | 2.8 | °C/W |
| Ψ _{JB} Junction-to-board characterization parameter | 41.2 | 57.3 | °C/W |
| R _{θJC(bot)} Junction-to-case (bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.7 Electrical Characteristics: $V_S = 2.7 \text{ V to } 5.5 \text{ V}$ (Single-Supply)

at $T_A = 25^\circ\text{C}$, $R_F = 604 \Omega$, $R_L = 150 \Omega$, and connected to $V_S / 2$, (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------|---|--|-------------------------|--------------|------------------------------|
| OFFSET VOLTAGE | | | | | |
| V_{OS} | $V_S = 5 \text{ V}$ | | ± 2 | ± 9 | mV |
| | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | | ± 15 | |
| dV_{OS}/dT | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | ± 7 | | $\mu\text{V}/^\circ\text{C}$ |
| Input offset voltage vs power supply | | | ± 80 | ± 350 | $\mu\text{V}/\text{V}$ |
| INPUT BIAS CURRENT | | | | | |
| I_B | | | 3 | ± 50 | pA |
| I_{OS} | Input offset current | | ± 1 | ± 50 | pA |
| NOISE | | | | | |
| Input noise voltage density | $f = 1 \text{ MHz}$ | | 5.8 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| Current noise density | $f = 1 \text{ MHz}$ | | 50 | | $\text{fA}/\sqrt{\text{Hz}}$ |
| INPUT VOLTAGE RANGE | | | | | |
| V_{CM} | Common-mode voltage range | | $(V-) - 0.1$ | $(V+) - 1.5$ | V |
| CMRR | $V_S = 5.5 \text{ V}, -0.1 \text{ V} < V_{CM} < 4 \text{ V}$ | 66 | 80 | | dB |
| | $V_S = 5.5 \text{ V}, -0.1 \text{ V} < V_{CM} < 4 \text{ V}$ $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | 66 | | | dB |
| INPUT IMPEDANCE | | | | | |
| Differential | | | $10^{13} \parallel 1.5$ | | $\Omega \parallel \text{pF}$ |
| Common-mode | | | $10^{13} \parallel 1.5$ | | $\Omega \parallel \text{pF}$ |
| OPEN-LOOP GAIN | | | | | |
| Open-loop gain | $V_S = 5 \text{ V}, 0.3 \text{ V} < V_O < 4.7 \text{ V}$ | 84 | 92 | | dB |
| | OPA355: $V_S = 5 \text{ V}, 0.3 \text{ V} < V_O < 4.7 \text{ V}$ $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | 80 | | | dB |
| | OPA2355, OPA3355: $V_S = 5 \text{ V}, 0.4 \text{ V} < V_O < 4.6 \text{ V}$ | 80 | | | dB |
| FREQUENCY RESPONSE | | | | | |
| $f_{-3\text{dB}}$ | $G = 1, V_O = 100 \text{ mVp-p}, R_F = 0 \Omega$ | | 450 | | MHz |
| | $G = 2, V_O = 100 \text{ mVp-p}, R_L = 50 \Omega$ | | 100 | | MHz |
| | $G = 2, V_O = 100 \text{ mVp-p}, R_L = 150 \Omega$ | | 170 | | MHz |
| | $G = 2, V_O = 100 \text{ mVp-p}, R_L = 1 \text{ k}\Omega$ | | 200 | | MHz |
| GBW | $G = 10, R_L = 1 \text{ k}\Omega$ | | 200 | | MHz |
| $f_{0.1\text{dB}}$ | Bandwidth for 0.1-dB gain flatness | $G = 2, V_O = 100 \text{ mVp-p}, R_F = 560 \Omega$ | 75 | | MHz |
| SR | Slew rate | $V_S = 5 \text{ V}, G = 2, 4\text{-V output step}$ | 300 / -360 | | $\text{V}/\mu\text{s}$ |
| | Rise and fall time | $G = 2, V_O = 200 \text{ Vp-p}, 10\% \text{ to } 90\%$ | 2.4 | | ns |
| | | $G = 2, V_O = 2 \text{ Vp-p}, 10\% \text{ to } 90\%$ | 8 | | ns |
| Settling time | 0.1%: $V_S = 5 \text{ V}, G = 2, 2\text{-V output step}$ | | 30 | | ns |
| | 0.01%: $V_S = 5 \text{ V}, G = 2, 2\text{-V output step}$ | | 120 | | ns |
| Overload recovery time | $V_{IN} \times \text{gain} = V_S$ | | 8 | | ns |
| HARMONIC DISTORTION | | | | | |
| Second harmonic | $G = 2, f = 1 \text{ MHz}, V_O = 2 \text{ Vp-p}, R_L = 200 \Omega$ | | -81 | | dBc |
| Third harmonic | $G = 2, f = 1 \text{ MHz}, V_O = 2 \text{ Vp-p}, R_L = 200 \Omega$ | | -93 | | dBc |
| Differential gain error | NTSC, $R_L = 150 \Omega$ | | 0.02 | | % |

Electrical Characteristics: $V_S = 2.7 \text{ V to } 5.5 \text{ V}$ (Single-Supply) (continued)

at $T_A = 25^\circ\text{C}$, $R_F = 604 \Omega$, $R_L = 150 \Omega$, and connected to $V_S / 2$, (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|--|------------|-----|------|
| Differential phase error | NTSC, $R_L = 150 \Omega$ | | 0.05 | | ° |
| Channel-to-channel crosstalk | OPA2355: $f = 5 \text{ MHz}$ | | -90 | | dB |
| | OPA3355: $f = 5 \text{ MHz}$ | | -70 | | dB |
| OUTPUT | | | | | |
| Voltage output swing from rail | $V_S = 5 \text{ V}$, $R_L = 150 \Omega$, $A_{OL} > 84 \text{ dB}$ | | 0.2 | 0.3 | V |
| | $V_S = 5 \text{ V}$, $R_L = 1 \text{ k}\Omega$ | | 0.1 | | V |
| I_O | Continuous output current ⁽¹⁾ | | ±60 | | mA |
| | Peak output current ⁽¹⁾ | $V_S = 5 \text{ V}$ | ±100 | | mA |
| Closed-loop output impedance ⁽¹⁾ | $V_S = 3 \text{ V}$ | | ±80 | | mA |
| | $f < 100 \text{ kHz}$ | | 0.02 | | Ω |
| POWER SUPPLY | | | | | |
| V_S | Specified voltage range | | 2.7 | 5.5 | V |
| | Operating voltage range | | 2.5 to 5.5 | | V |
| I_Q | Quiescent current (per amplifier) | $V_S = 5 \text{ V}$, enabled, $I_O = 0$ | 8.3 | 11 | mA |
| | | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | 14 | mA |
| SHUTDOWN | | | | | |
| Disabled (logic-LOW threshold) | | | | 0.8 | V |
| Enabled (logic-HIGH threshold) | | | 2 | | V |
| Enable time | | | 100 | | ns |
| Disable time | | | 30 | | ns |
| Shutdown current (per amplifier) | $V_S = 5 \text{ V}$, disabled | | 3.4 | 6 | μA |
| THERMAL SHUTDOWN | | | | | |
| Junction temperature | Shutdown | | 160 | | °C |
| | Reset from shutdown | | 140 | | |
| TEMPERATURE RANGE | | | | | |
| Specified range | | -40 | 125 | | °C |
| Operating range | | -55 | 150 | | °C |
| Storage range | | -65 | 150 | | °C |
| θ_{JA} | SOT-23-6, VSSOP-10 | | 150 | | °C/W |
| | SO-8 | | 125 | | °C/W |
| | SO-14, TSSOP-14 | | 100 | | °C/W |

(1) See [Output Voltage Swing vs Output Current](#).

7.8 Typical Characteristics

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $G = 2$, $R_F = 604\text{ }\Omega$, and $R_L = 150\text{ }\Omega$ connected to $V_S / 2$, (unless otherwise noted)

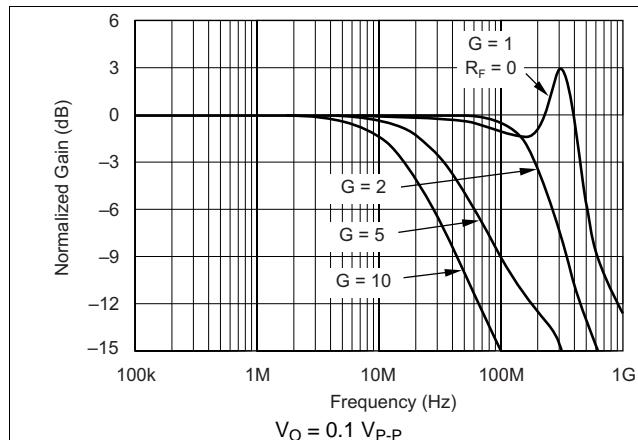


Figure 1. Noninverting Small-Signal Frequency Response

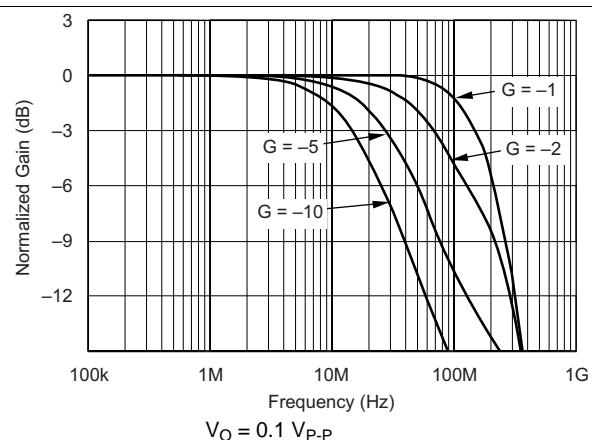


Figure 2. Inverting Small-Signal Frequency Response

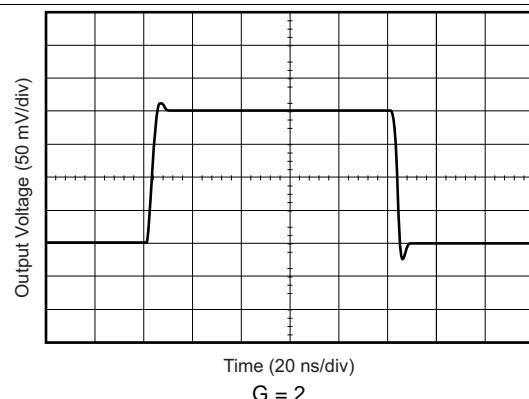


Figure 3. Noninverting Small-Signal Step Response

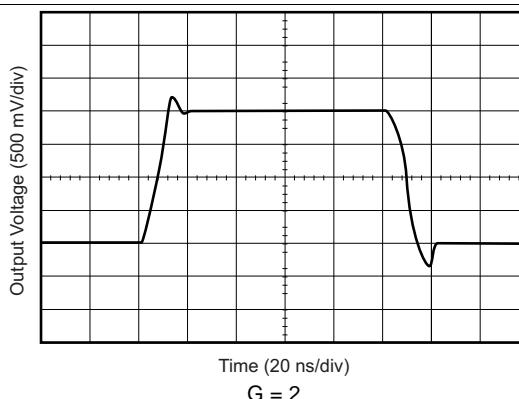


Figure 4. Noninverting Large-Signal Step Response

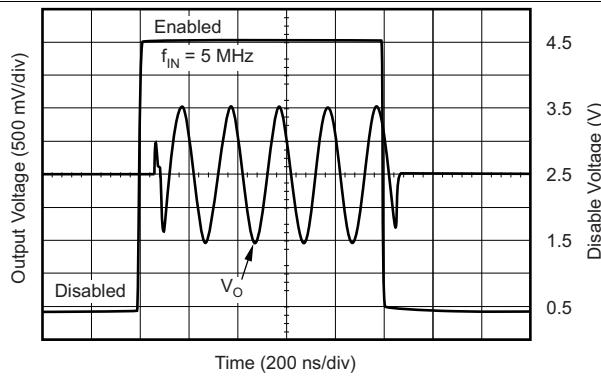


Figure 5. Large-Signal Disable and Enable Response

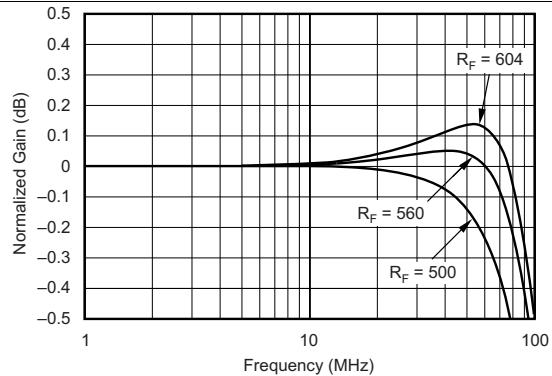


Figure 6. 0.1-dB Gain Flatness for Various RF Values

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $G = 2$, $R_F = 604\ \Omega$, and $R_L = 150\ \Omega$ connected to $V_S / 2$, (unless otherwise noted)

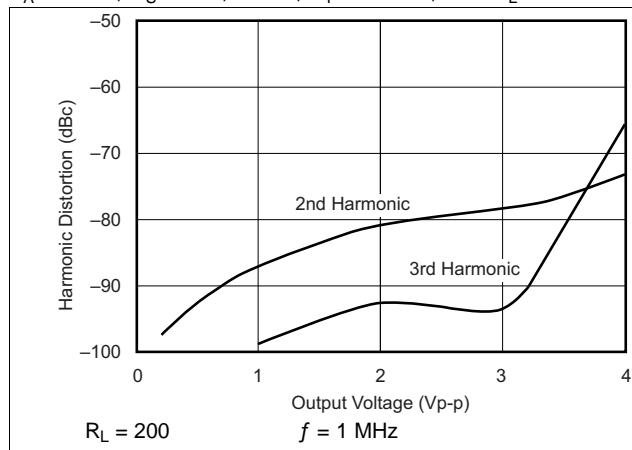


Figure 7. Harmonic Distortion vs Output Voltage

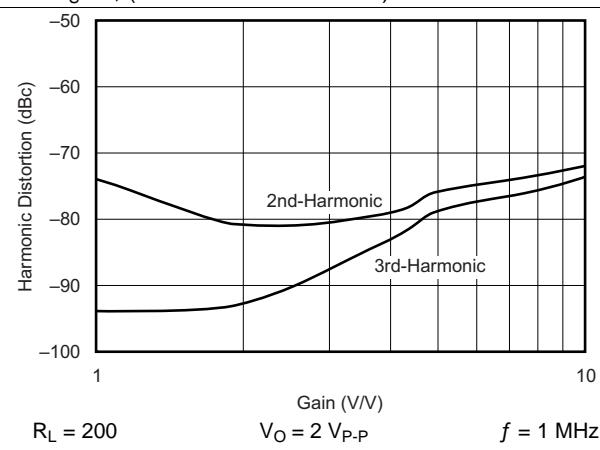


Figure 8. Harmonic Distortion vs Noninverting Gain

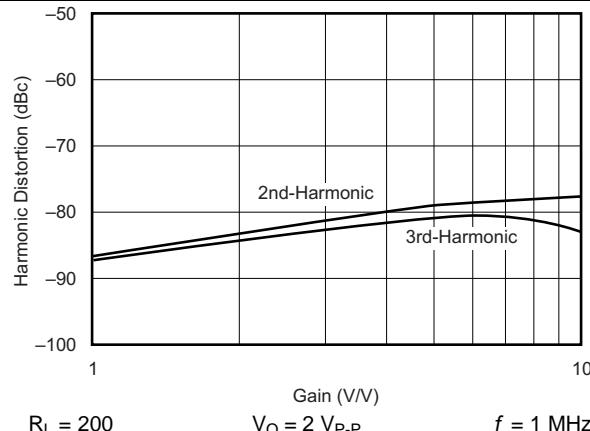


Figure 9. Harmonic Distortion vs Inverting Gain

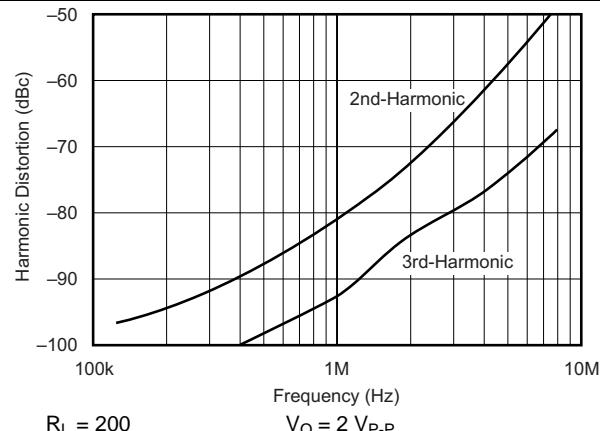


Figure 10. Harmonic Distortion vs Frequency

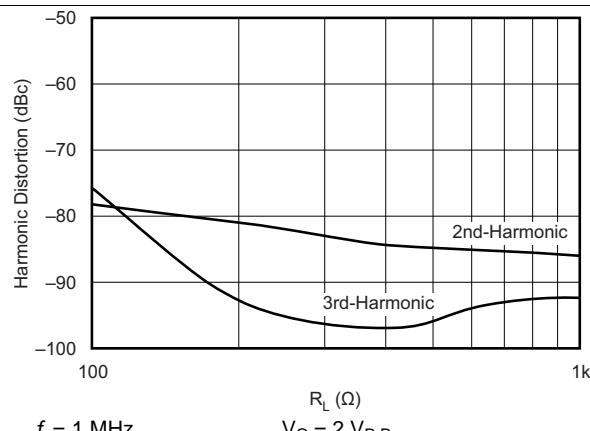


Figure 11. Harmonic Distortion vs Load Resistance

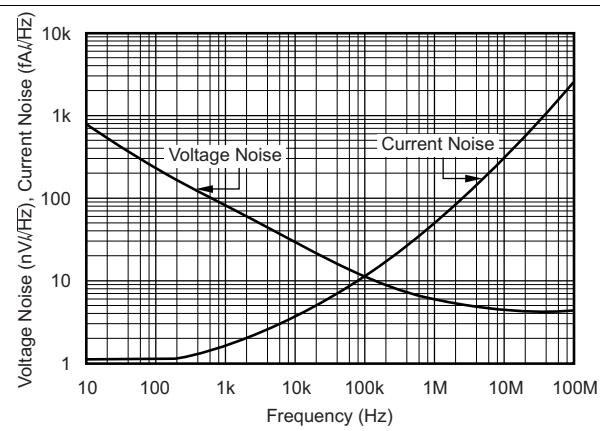


Figure 12. Input Voltage and Current Noise Spectral Density vs Frequency

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5 \text{ V}$, $G = 2$, $R_F = 604 \Omega$, and $R_L = 150 \Omega$ connected to $V_S / 2$, (unless otherwise noted)

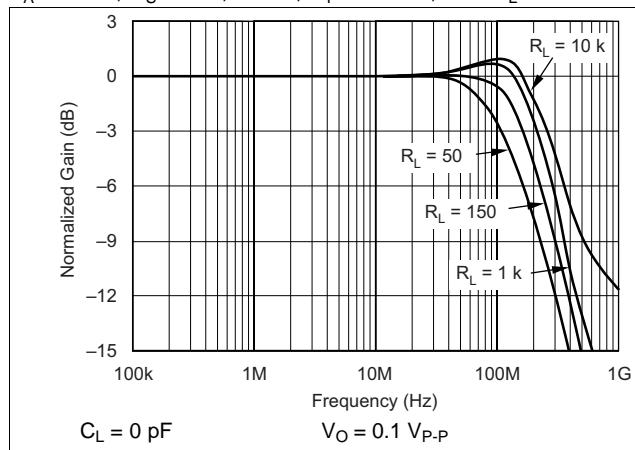


Figure 13. Frequency Response for Various R_L Values

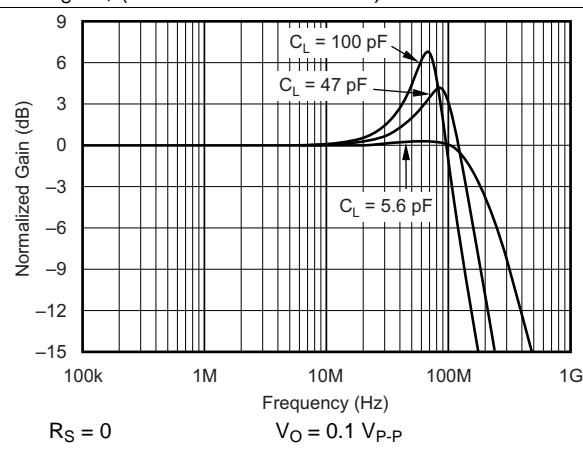


Figure 14. Frequency Response for Various C_L Values

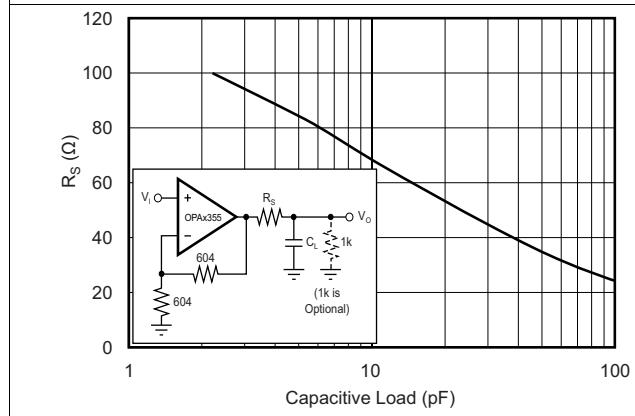


Figure 15. Recommended R_S Values vs Capacitive Load

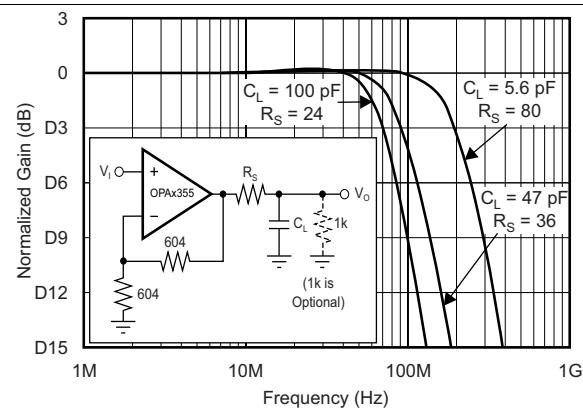


Figure 16. Frequency Response vs Capacitive Load

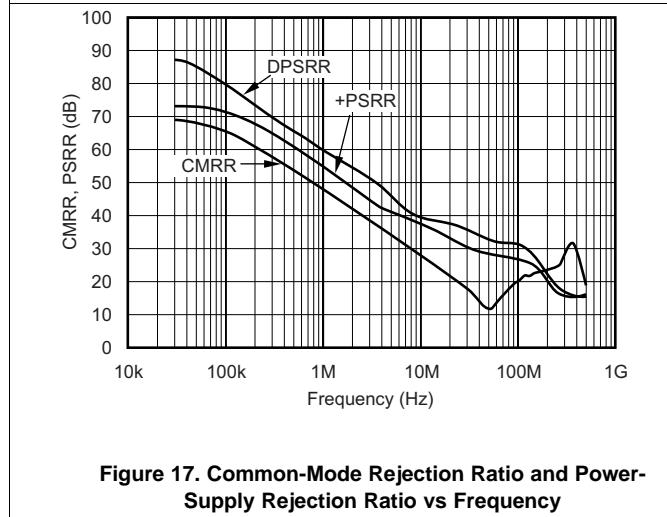


Figure 17. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

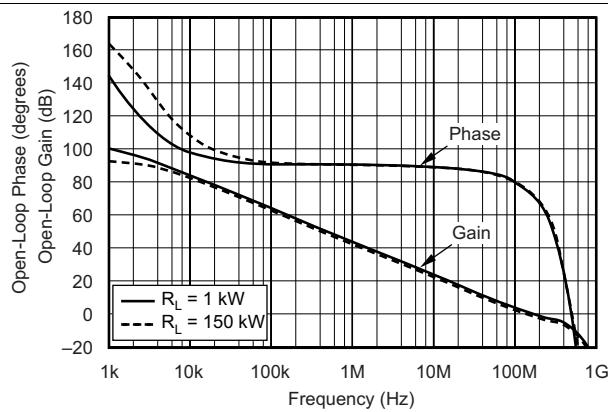


Figure 18. Open-Loop Gain and Phase

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $G = 2$, $R_F = 604\text{ }\Omega$, and $R_L = 150\text{ }\Omega$ connected to $V_S / 2$, (unless otherwise noted)

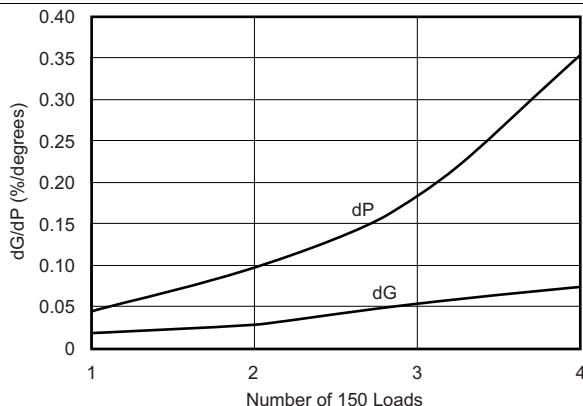


Figure 19. Composite Video Differential Gain and Phase

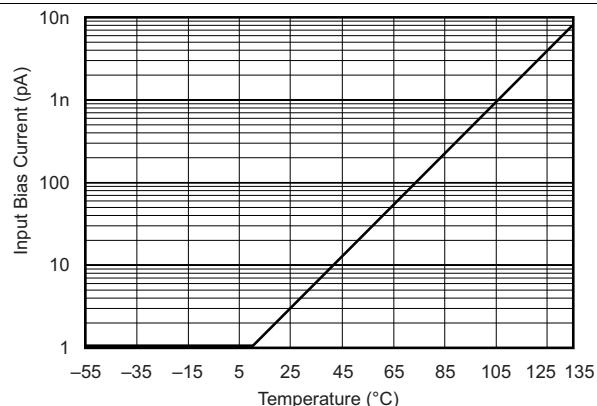
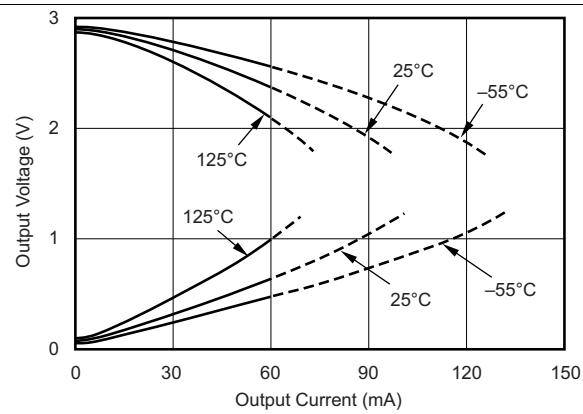


Figure 20. Input Bias Current vs Temperature



Continuous currents above 60 mA are not recommended
 $V_S = 3\text{ V}$

Figure 21. Output Voltage Swing vs Output Current

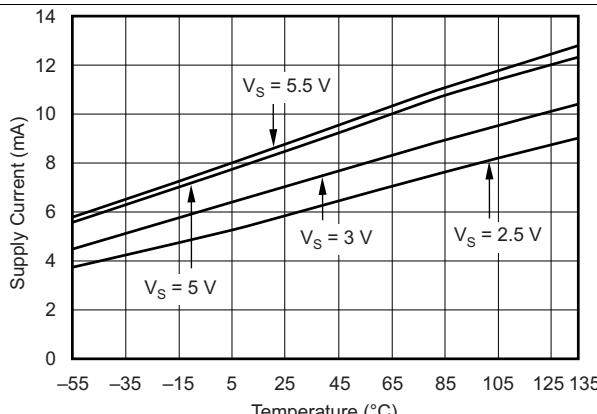
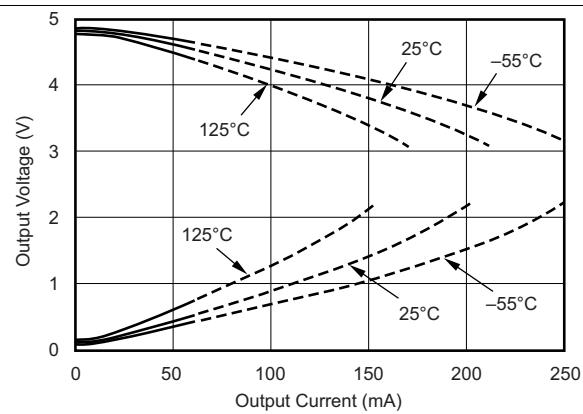


Figure 22. Supply Current vs Temperature



Continuous currents above 60 mA are not recommended
 $V_S = 5\text{ V}$

Figure 23. Output Voltage Swing vs Output Current

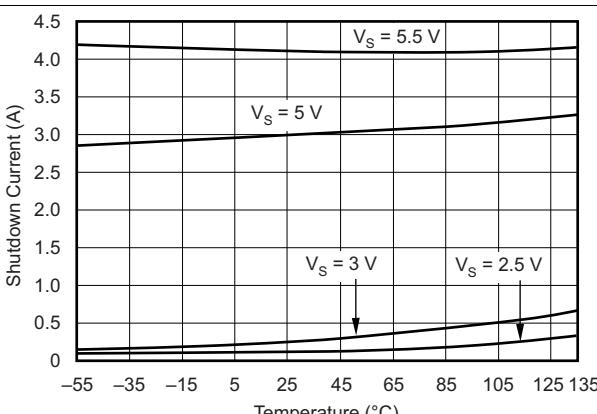


Figure 24. Shutdown Current vs Temperature

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $G = 2$, $R_F = 604\ \Omega$, and $R_L = 150\ \Omega$ connected to $V_S / 2$, (unless otherwise noted)

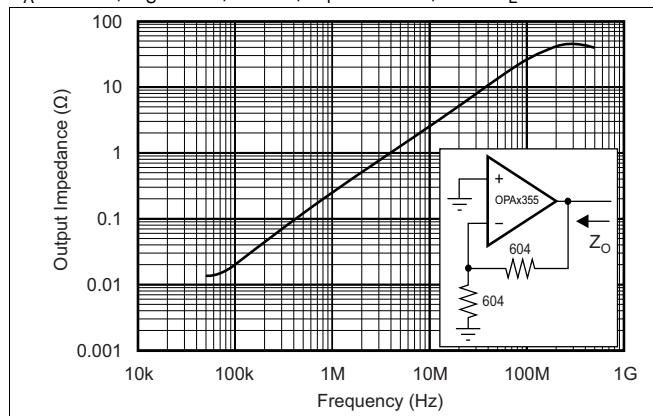
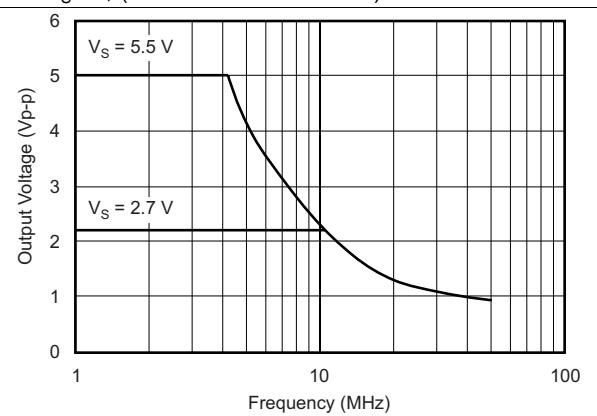


Figure 25. Closed-Loop Output Impedance vs Frequency



Maximum output voltage without slew-rate induced distortion

Figure 26. Maximum Output Voltage vs Frequency

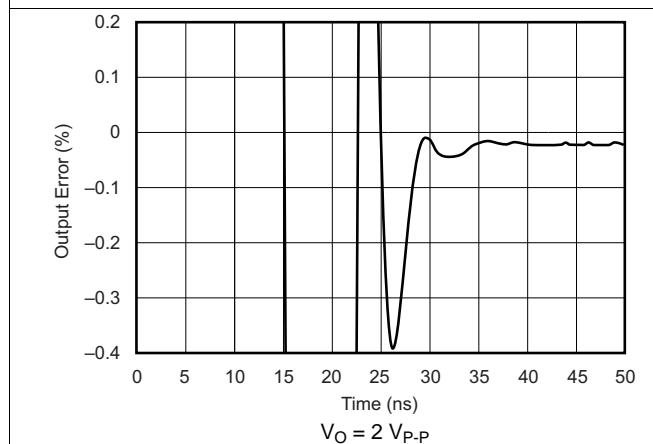


Figure 27. Output Settling Time to 0.1%

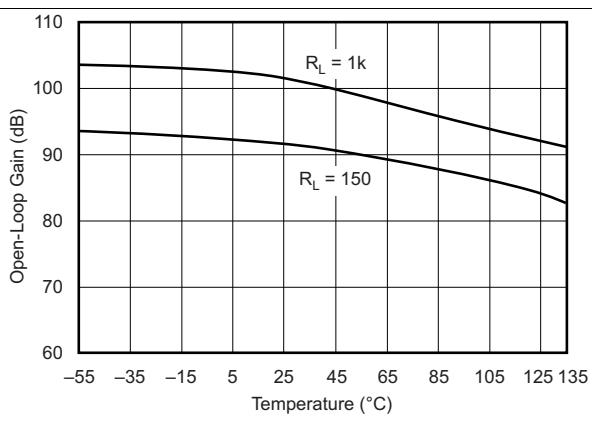


Figure 28. Open-Loop Gain vs Temperature

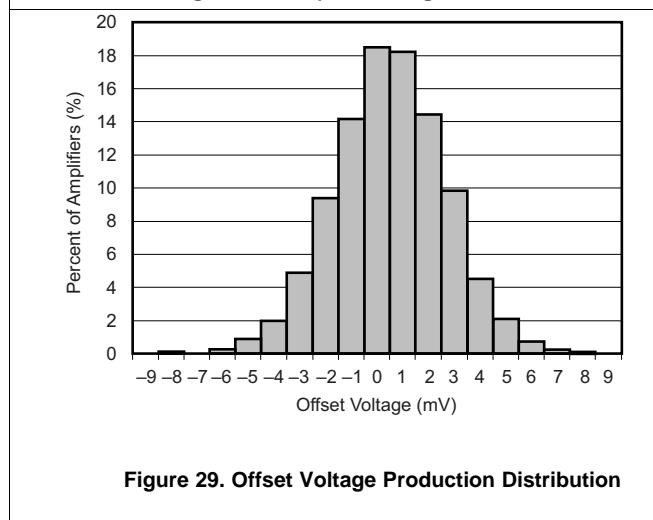


Figure 29. Offset Voltage Production Distribution

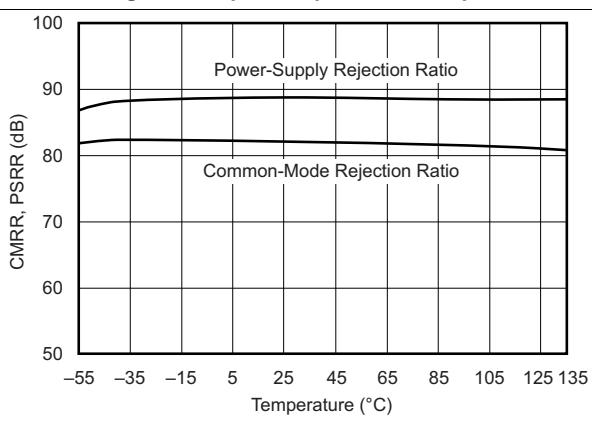


Figure 30. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

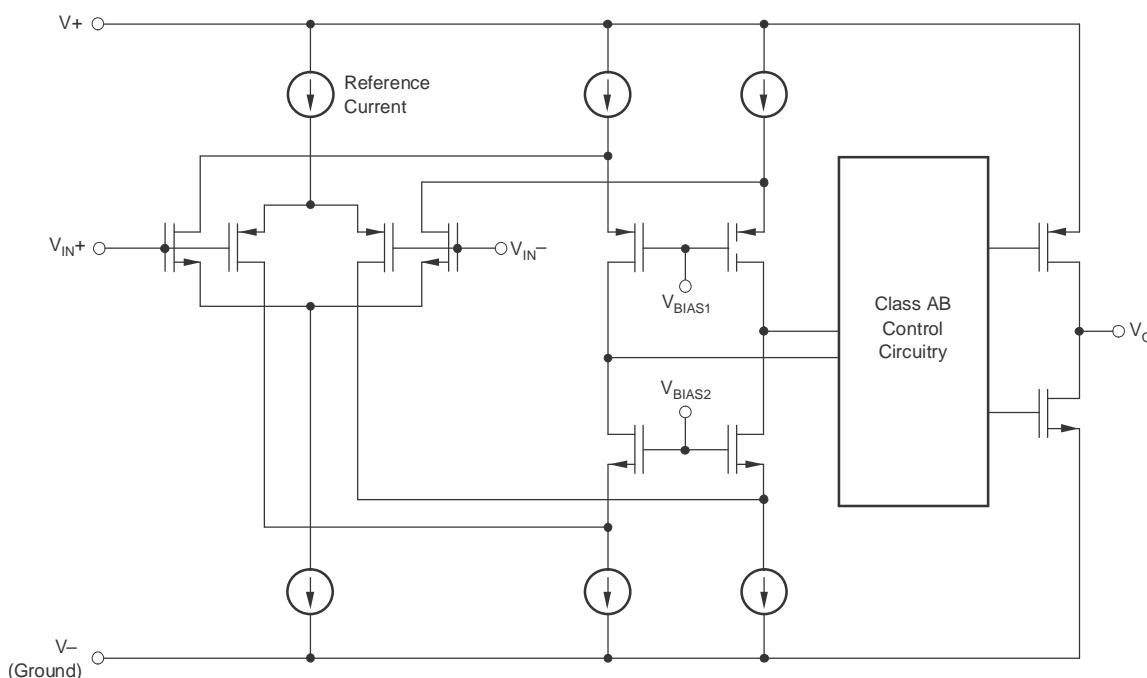
8 Detailed Description

8.1 Overview

The OPA355 series is a CMOS, high-speed, voltage-feedback, operational amplifier designed for video and other general-purpose applications. The series is available as a single, dual, or triple op amp. The family features a 200-MHz gain bandwidth and 360 V/ μ s slew rate, but the series is unity-gain stable and can operate as a 1 V/V voltage follower.

The input common-mode range includes ground, allowing the OPAX355 family to be used in virtually any single-supply application up to a supply voltage of 5.5 V.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The OPAX355 family is specified over a power-supply range of 2.7 V to 5.5 V (± 1.35 to ± 2.75 V). However, the supply voltage ranges from 2.5 to 5.5 V (± 1.25 to ± 2.75 V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary significantly over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

8.3.2 Enable Function

The OPAX355 series is enabled by applying a TTL high-voltage level to the enable pin. Conversely, a TTL low-voltage level disables the amplifier, which reduces the supply current from 8.3 mA to 3.4 μ A per amplifier. This pin voltage is referenced to a single-supply ground. When using a split-supply, such as ± 2.5 V, the enable and disable voltage levels are referenced to V-. For portable battery-operated applications, this feature greatly reduces the average current and as a result, extends battery life.

The enable input is modeled as a CMOS input gate with a 100-k Ω pullup resistor to V+. The enable pin assumes a logic high and the amplifier turns on if the enable pin is left open.

Feature Description (continued)

The enable time is 100 ns and the disable time is 30 ns, which allows the OPAX355 series to operate as a *gated* amplifier, or to have the output multiplexed onto a common output bus. When disabled, the output assumes a high-impedance state.

8.3.3 Output Drive

The output stage supplies a high short-circuit current (typically over 200 mA). Therefore, an on-chip thermal shutdown circuit is provided to protect the OPAX355 series from dangerously-high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below 140°C.

NOTE

Running a continuous DC current in excess of ± 60 mA is not recommended. See the *Output Voltage Swing vs Output Current* graphs ([Figure 21](#) and [Figure 22](#)) in the [Typical Characteristics](#) section.

8.4 Device Functional Modes

The OPAX355 family is powered on when the supply is connected. The series operates as a single supply operational amplifier or dual supply amplifier depending on the application. The series is used with asymmetrical supplies as long as the differential voltage (V₋ to V₊) is at least 1.8 V and no greater than 5.5 V (example: V₋ set to -3.5 V and V₊ set to 1.5 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAX355 series is a CMOS, high-speed, voltage-feedback, operational amplifier (op amp) designed for general-purpose applications.

The amplifiers feature a 200-MHz gain bandwidth and 300-V/ μ s slew rate, but the devices are unity-gain stable and operate as a 1-V/V voltage follower.

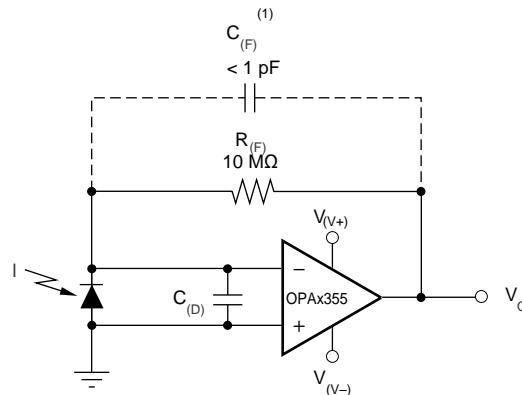
The input common-mode voltage range of the series includes ground, which allows the OPAX355 to be used in virtually any single-supply application up to a supply voltage of 5.5 V.

9.2 Typical Applications

9.2.1 Transimpedance Amplifier

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPAX355 series a preferred wideband photodiode transimpedance amplifier family. Low voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequencies.

The key elements to a transimpedance design, as shown in [Figure 31](#), are the expected diode capacitance ($C_{(D)}$), which must include the parasitic input common-mode and differential-mode input capacitance (4 pF + 5 pF), the desired transimpedance gain ($R_{(FB)}$), and the gain-bandwidth (GBW) for the OPAX355 family (20 MHz). With these three variables set, the feedback capacitor value ($C_{(FB)}$) controls the frequency response. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$, which is 0.2 pF for a typical surface-mount resistor.



(1) $C_{(FB)}$ is optional to prevent gain peaking. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$.

Figure 31. Dual-Supply Transimpedance Amplifier

9.2.1.1 Design Requirements

| PARAMETER | VALUE |
|---------------------------|--------|
| Supply voltage $V_{(V+)}$ | 2.5 V |
| Supply voltage $V_{(V-)}$ | -2.5 V |

9.2.1.2 Detailed Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, set the feedback pole to:

$$\frac{1}{2 \times \pi \times R_{(FB)} \times C_{(FB)}} = \sqrt{\frac{GBW}{4 \times \pi \times R_{(FB)} \times C_{(D)}}} \quad (1)$$

Use [Equation 2](#) to calculate the bandwidth.

$$f_{(-3 \text{ dB})} = \sqrt{\frac{GBW}{2 \times \pi \times R_{(FB)} \times C_{(D)}}} \quad (2)$$

For other transimpedance bandwidths, consider the high-speed CMOS [OPA380](#) (90-MHz GBW), [OPA354](#) (100-MHz GBW), [OPA300](#) (180-MHz GBW), [OPA355](#) (200-MHz GBW), or [OPA656](#) and [OPA657](#) (400-MHz GBW).

For single-supply applications, the $+INx$ input is biased with a positive DC voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail. [Figure 32](#) shows this configuration. This bias voltage appears across the photodiode, providing a reverse bias for faster operation.

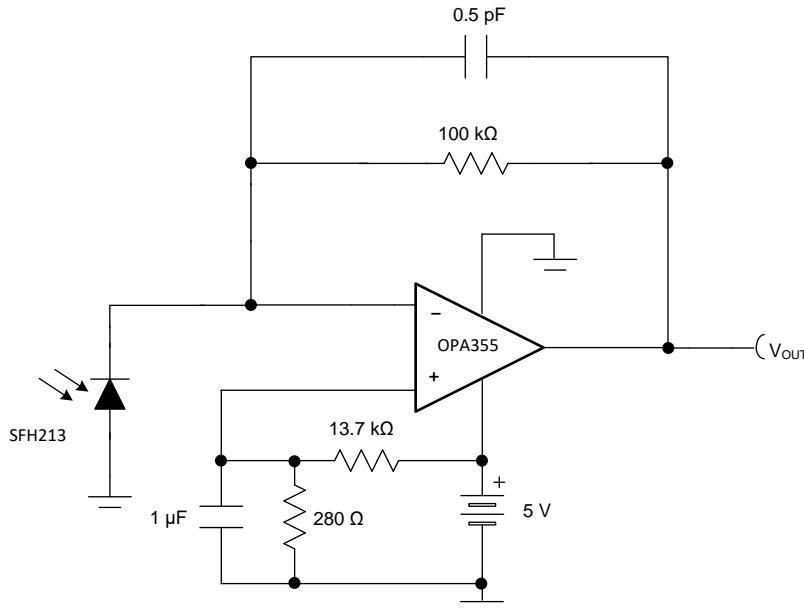


Figure 32. Single-Supply Transimpedance Amplifier

For additional information, see [Compensate Transimpedance Amplifiers Intuitively](#).

9.2.1.2.1 Optimizing The Transimpedance Circuit

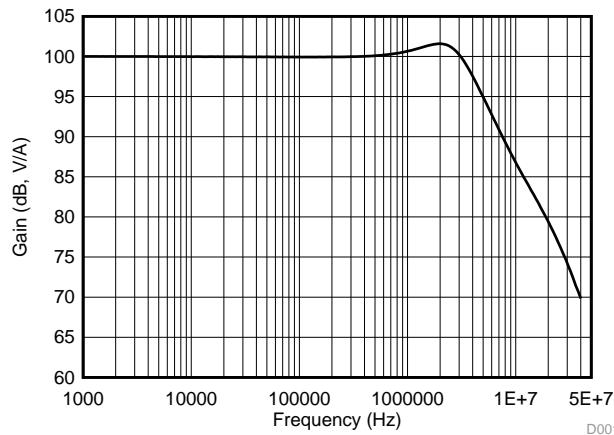
To achieve the best performance, select components according to the following guidelines:

1. For lowest noise, select $R_{(FB)}$ to create the total required gain. Using a lower value for $R_{(FB)}$ and adding gain after the transimpedance amplifier generally results in poorer noise performance. $R_{(FB)}$ produces noise that increases with the square root of $R_{(FB)}$, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to amplify (increasing amplification at high frequencies). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Only use the required circuit bandwidth. Use a capacitor across the $R_{(FB)}$ to limit bandwidth, even if a capacitor is not required for stability.
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. Control leakage by using a circuit board guard trace that encircles the summing junction and

drives at the same voltage.

For additional information, see [Noise Analysis of FET Transimpedance Amplifiers](#) and [Noise Analysis for High-Speed Op Amps](#).

9.2.1.3 Application Curve



–3 dB bandwidth is 4.56 MHz

Figure 33. AC Transfer Function

9.2.2 High-Impedance Sensor Interface

Many sensors have high source impedances that may range up to $10\text{ M}\Omega$, or even higher. The output signal of sensors often must be amplified or otherwise conditioned by an amplifier. The input bias current of this amplifier loads the sensor output and causes a voltage drop across the source resistance, [Figure 34](#) shows ($V_{(+INx)} = V_S - I_{(BIAS)} \times R_{(S)}$.) The last term ($I_{(BIAS)} \times R_{(S)}$) shows the voltage drop across $R_{(S)}$. To prevent errors introduced to the system as a result of this voltage, use an op amp with low input bias current with high-impedance sensors. This low current keeps the $I_{(BIAS)} \times R_{(S)}$ error contribution less than the input voltage noise of the amplifier so that input voltage noise is not the dominant noise factor. The OPAX355 op amps feature low input bias current (typically 200 fA), and as a result, a preferred choice for these applications.

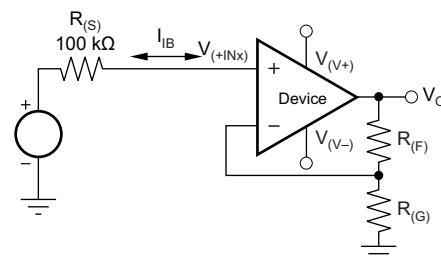
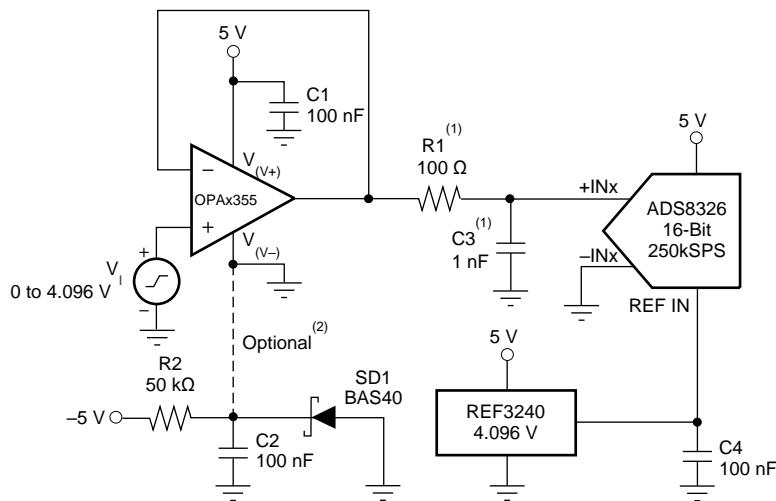


Figure 34. Noise as a Result of $I_{(BIAS)}$

9.2.3 Driving ADCs

The OPAX355 op amps are designed to drive sampling analog-to-digital converters (ADCs) with sampling speeds up to 1 MSPS. The zero-crossover distortion input stage topology allows the OPAX355 series to drive ADCs without degrading differential linearity and THD.

The OPAX355 series buffers the ADC switched input capacitance and resulting charge injection while providing signal gain. [Figure 35](#) shows the OPAX355 series configured to drive the [ADS8326](#).



(1) Suggested value; may require adjustment based on specific application.

(2) Single-supply applications lose a small number of ADC codes near ground as a result of op amp output swing limitation. If a negative power supply is available, this simple circuit creates a -0.3-V supply to allow output swing to true ground potential.

Figure 35. Driving the ADS8326

9.2.4 Active Filter

The OPAX355 series is designed for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. [Figure 36](#) shows a 500 kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components are selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is -40 dB/dec. The Butterworth response is preferred for applications requiring predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of the following options:

1. Adding an inverting amplifier
2. Adding an additional second-order MFB stage
3. Using a noninverting filter topology, such as the Sallen-Key (see [Figure 37](#)).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's [FilterPro™](#) program. This software is available as a free download at www.ti.com.

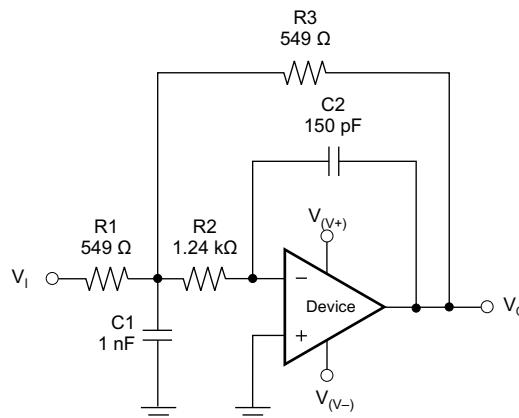


Figure 36. Second-Order Butterworth 500-kHz Low-Pass Filter

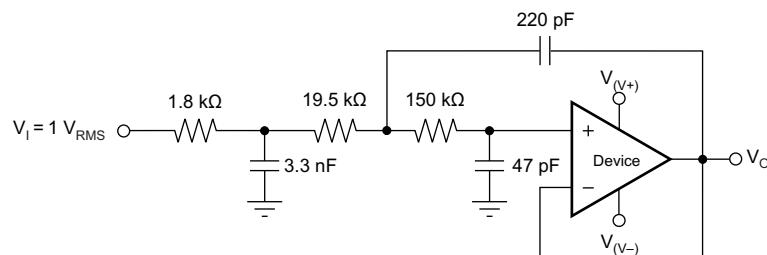


Figure 37. OPAx355 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

9.3 Video

The OPAx355 output stage is capable of driving a standard back-terminated 75- Ω video cable. By back-terminating a transmission line, the line does not exhibit a capacitive load to the driver. A properly back-terminated 75- Ω cable does not appear as capacitance; the cable presents only a 150- Ω resistive load to the OPAx355 output.

The OPAx355 can be used as an amplifier for RGB graphic signals, which have a voltage of zero at the video black level by offsetting and AC-coupling the signal, as shown in [Figure 38](#).

Video (continued)

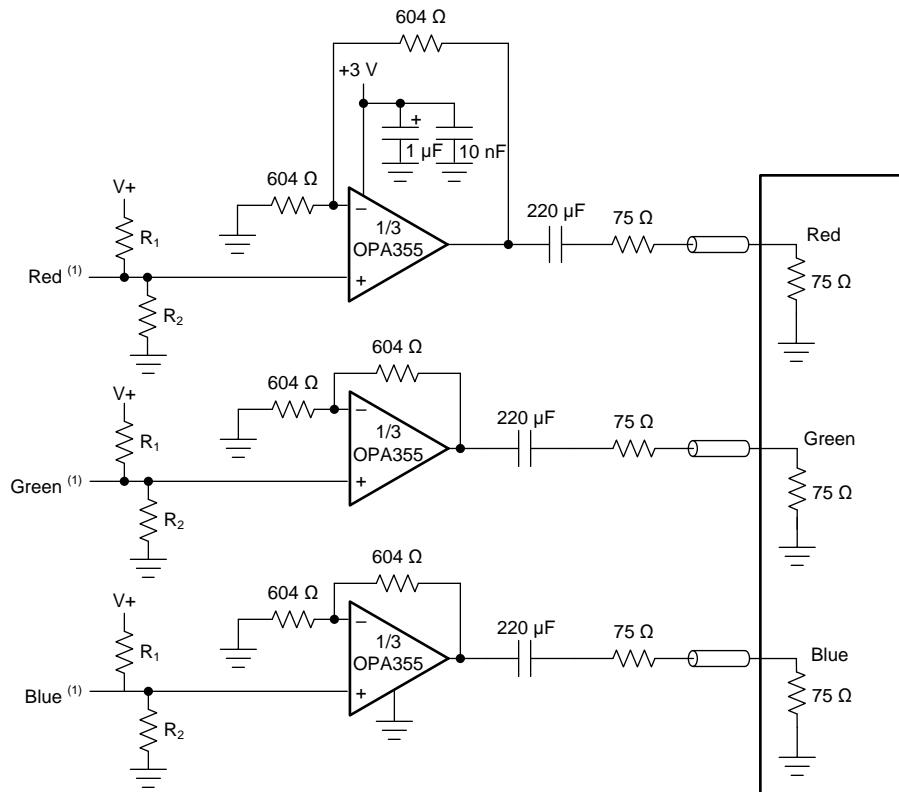


Figure 38. RGB Cable Driver

9.4 Wideband Video Multiplexing

One common application for video speed amplifiers which include an enable pin is to wire multiple amplifier outputs together, then select which one of several possible video inputs to source onto a single line. This simple wired-OR video multiplexer can be easily implemented using the OPA357; see [Figure 39](#).

Wideband Video Multiplexing (continued)

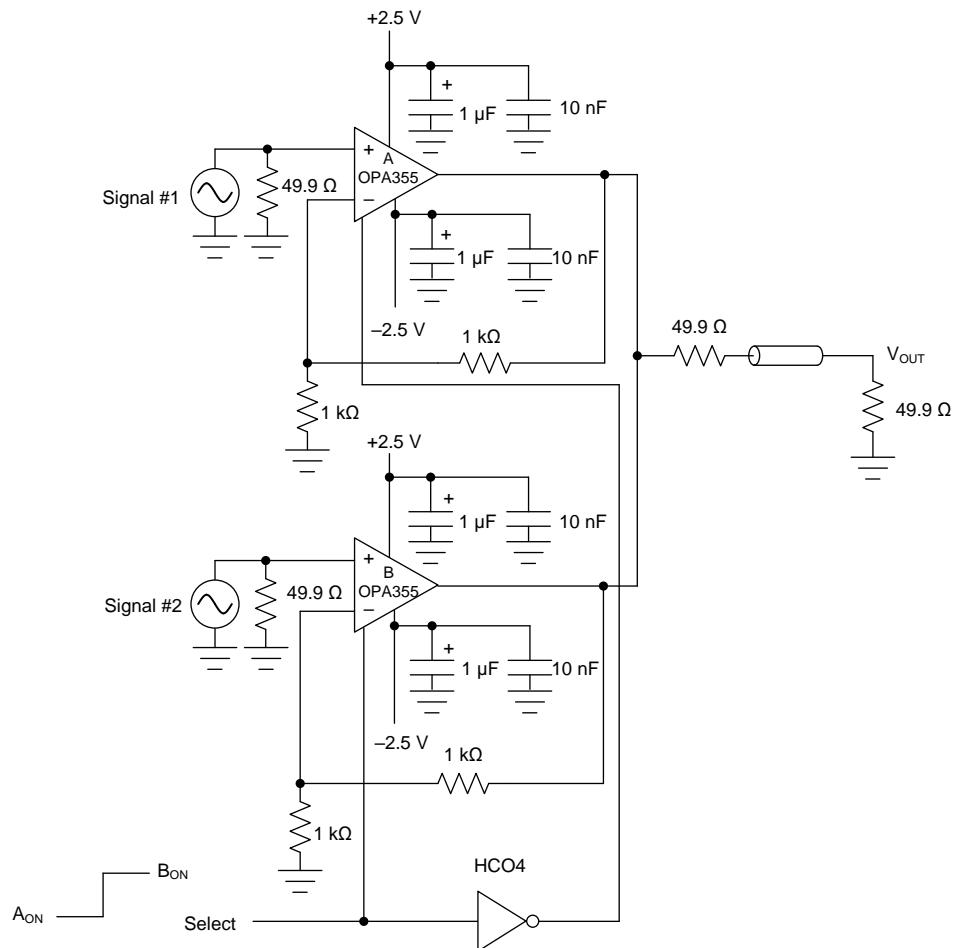


Figure 39. Multiplexed Output

10 Power Supply Recommendations

The OPAx355 is specified for operation from 2.7 to 5.5 V (± 1.35 to ± 2.75 V); many specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the *Typical Characteristics* section.

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

Power dissipation depends on power-supply voltage, signal and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, $\text{VS} - \text{VO}$. Minimize power dissipation by using the lowest possible power-supply voltage required to ensure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. *Power Amplifier Stress and Power Handling Limitations* explains how to calculate or measure power dissipation with unusual signals and loads, and is available on www.ti.com.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 150°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature to trigger the thermal protection at 160°C . The thermal protection must trigger more than 35°C above the maximum expected ambient condition of the application.

11 Layout

11.1 Layout Guidelines

Good high-frequency printed-circuit board (PCB) layout techniques must be used for the OPAx355 amplifiers. Generous use of ground planes, short direct-signal traces, and a preferred bypass capacitor located at the V^+ pin ensures clean and stable operation. Large areas of copper help dissipate heat generated within the amplifiers in normal operation.

Sockets are not recommended for use with any high-speed amplifier.

A 10-nF ceramic bypass capacitor is the minimum recommended value; adding a 1- μF or larger tantalum capacitor in parallel is beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving very low harmonic and intermodulation distortion.

11.2 Layout Example

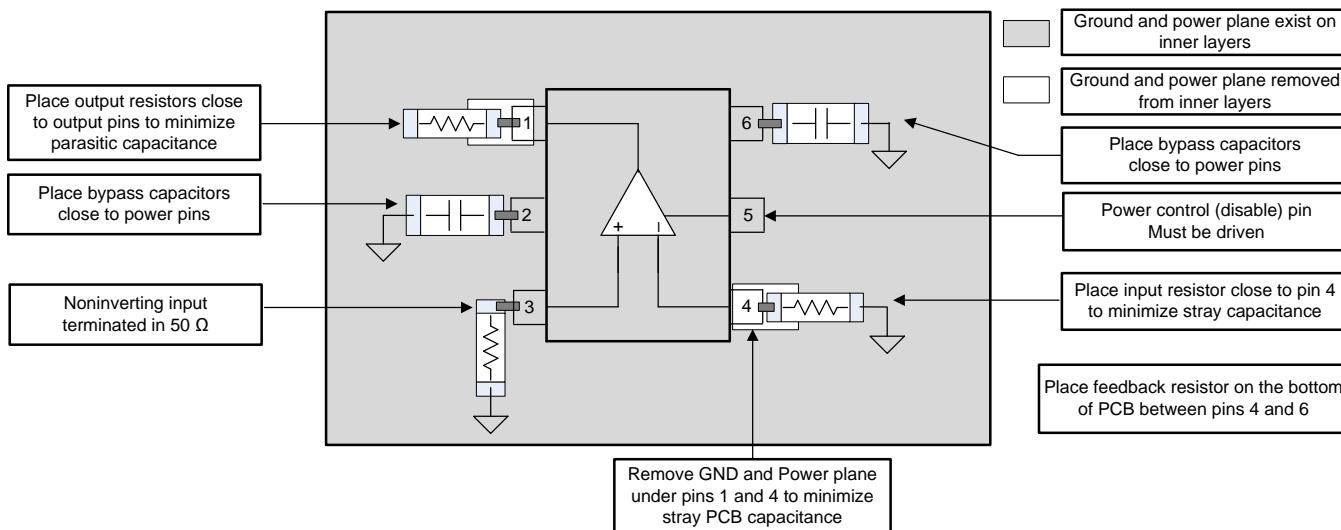


Figure 40. Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| OPA355 | Click here |
| OPA2355 | Click here |
| OPA3355 | Click here |

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community **TI's Engineer-to-Engineer (E2E) Community.** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support **TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

FilterPro is a trademark of Texas Instruments Incorporated.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

 ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| OPA2355DGSA/250 | Active | Production | VSSOP (DGS) 10 | 250 SMALL T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | D55 |
| OPA2355DGSA/250.B | Active | Production | VSSOP (DGS) 10 | 250 SMALL T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | D55 |
| OPA2355DGSA/250G4 | Active | Production | VSSOP (DGS) 10 | 250 SMALL T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | D55 |
| OPA3355EA/250 | Active | Production | TSSOP (PW) 14 | 250 SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA 3355EA |
| OPA3355EA/250.B | Active | Production | TSSOP (PW) 14 | 250 SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA 3355EA |
| OPA3355EA/2K5 | Active | Production | TSSOP (PW) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA 3355EA |
| OPA3355EA/2K5.B | Active | Production | TSSOP (PW) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA 3355EA |
| OPA3355UA | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA3355UA |
| OPA3355UA.B | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA3355UA |
| OPA355NA/250 | Active | Production | SOT-23 (DBV) 6 | 250 SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | C55 |
| OPA355NA/250.B | Active | Production | SOT-23 (DBV) 6 | 250 SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | C55 |
| OPA355NA/250G4 | Active | Production | SOT-23 (DBV) 6 | 250 SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | C55 |
| OPA355NA/3K | Active | Production | SOT-23 (DBV) 6 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | C55 |
| OPA355NA/3K.B | Active | Production | SOT-23 (DBV) 6 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | C55 |
| OPA355NA/3KG4 | Active | Production | SOT-23 (DBV) 6 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | C55 |
| OPA355UA | Active | Production | SOIC (D) 8 | 75 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA 355UA |
| OPA355UA.B | Active | Production | SOIC (D) 8 | 75 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA 355UA |
| OPA355UA/2K5 | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA 355UA |
| OPA355UA/2K5.B | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA 355UA |
| OPA355UAG4 | Active | Production | SOIC (D) 8 | 75 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA 355UA |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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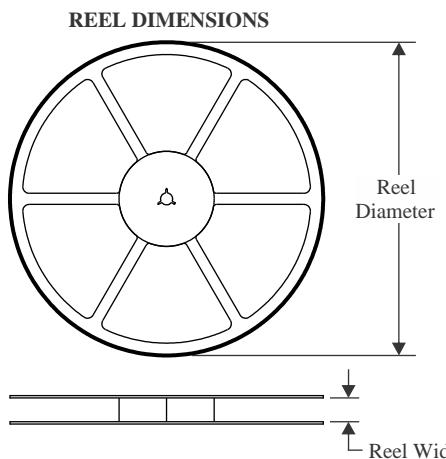
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA355 :

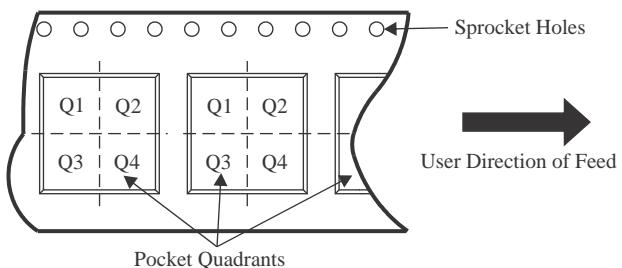
- Automotive : [OPA355-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


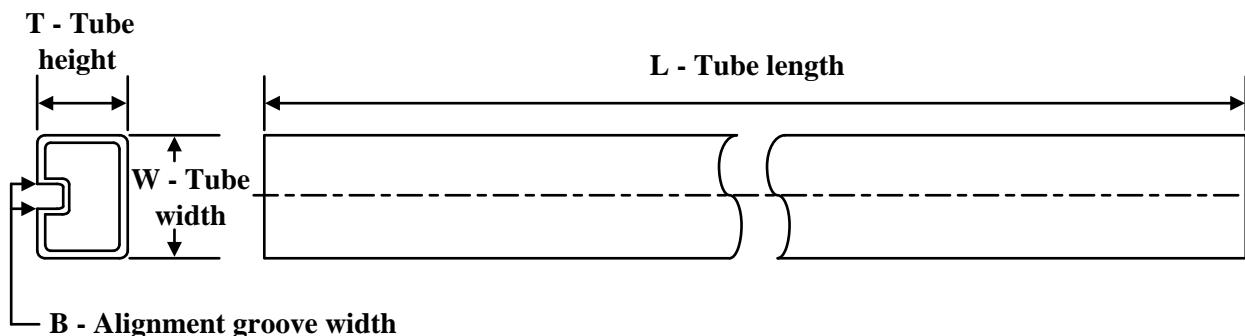
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA2355DGSA/250 | VSSOP | DGS | 10 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA3355EA/250 | TSSOP | PW | 14 | 250 | 180.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| OPA3355EA/2K5 | TSSOP | PW | 14 | 2500 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| OPA355NA/250 | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| OPA355NA/3K | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| OPA355UA/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA2355DGSA/250 | VSSOP | DGS | 10 | 250 | 213.0 | 191.0 | 35.0 |
| OPA3355EA/250 | TSSOP | PW | 14 | 250 | 213.0 | 191.0 | 35.0 |
| OPA3355EA/2K5 | TSSOP | PW | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| OPA355NA/250 | SOT-23 | DBV | 6 | 250 | 445.0 | 220.0 | 345.0 |
| OPA355NA/3K | SOT-23 | DBV | 6 | 3000 | 445.0 | 220.0 | 345.0 |
| OPA355UA/2K5 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

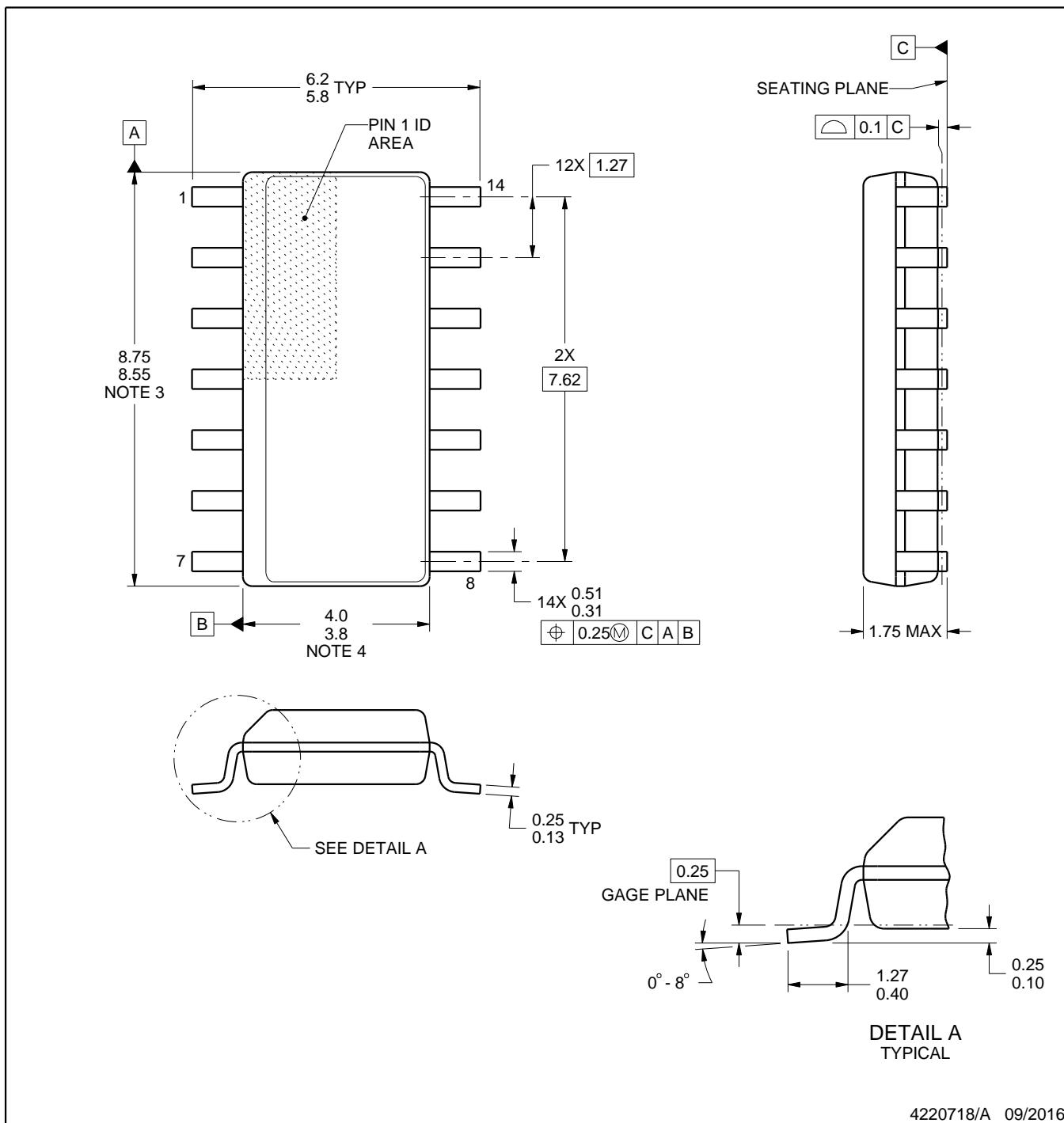
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| OPA3355UA | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| OPA3355UA.B | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| OPA355UA | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA355UA.B | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA355UAG4 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

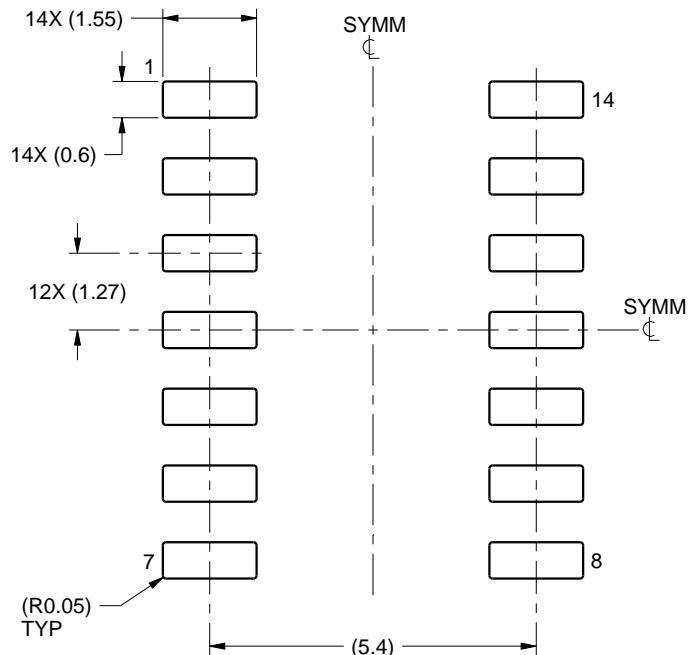
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

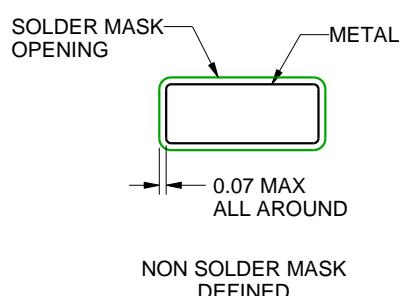
D0014A

SOIC - 1.75 mm max height

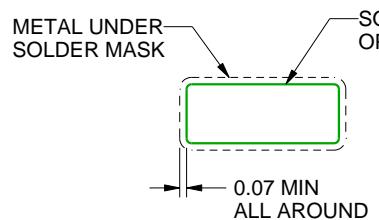
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

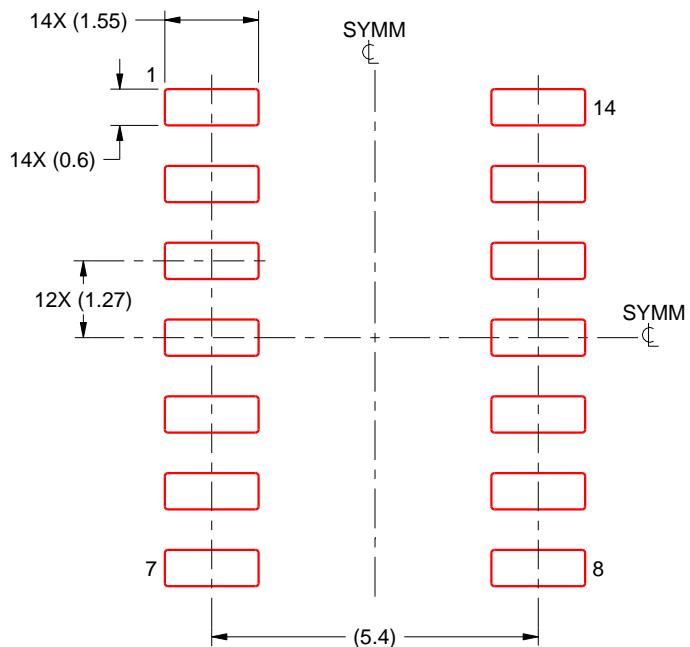
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

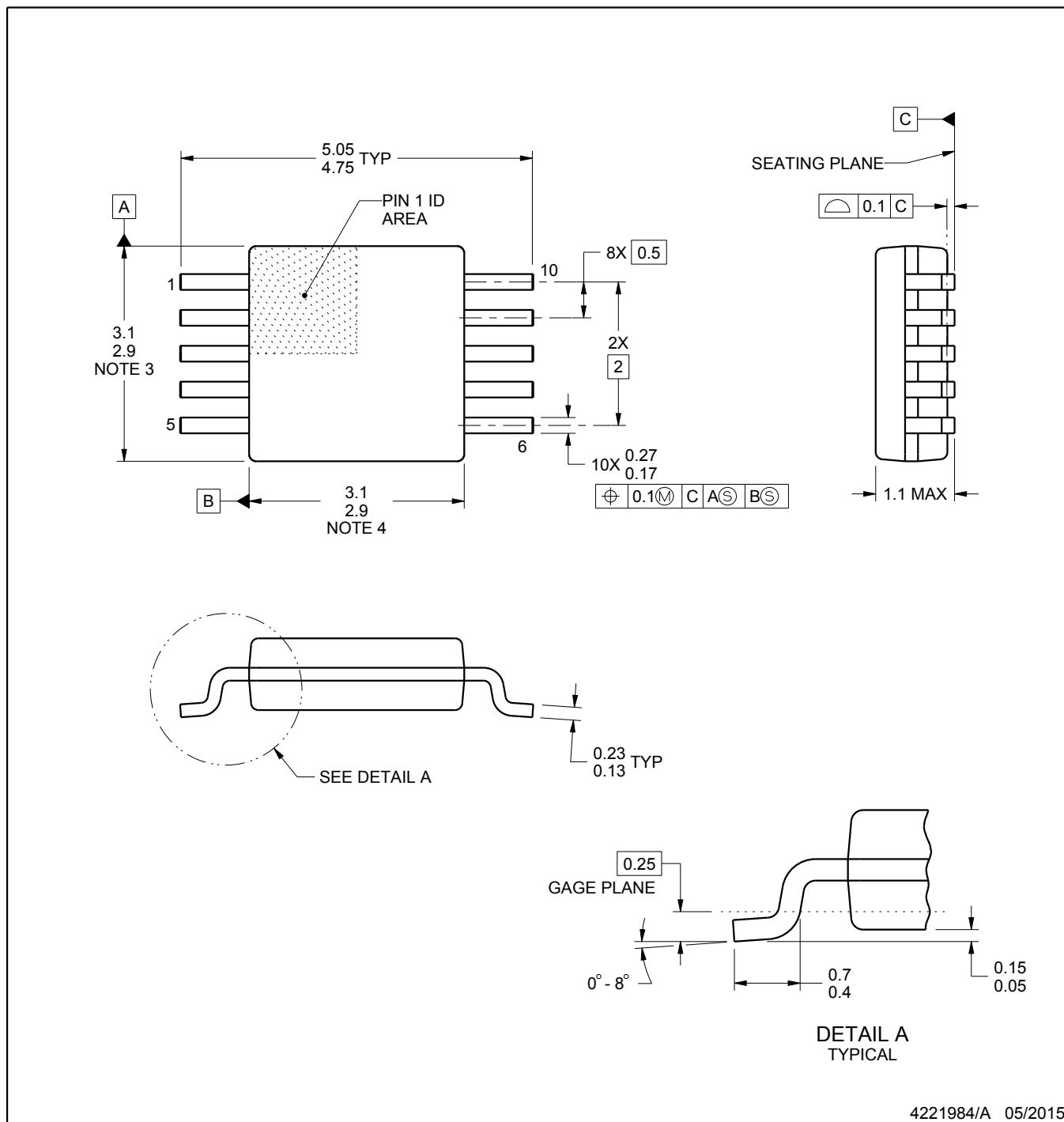
PACKAGE OUTLINE

DGS0010A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

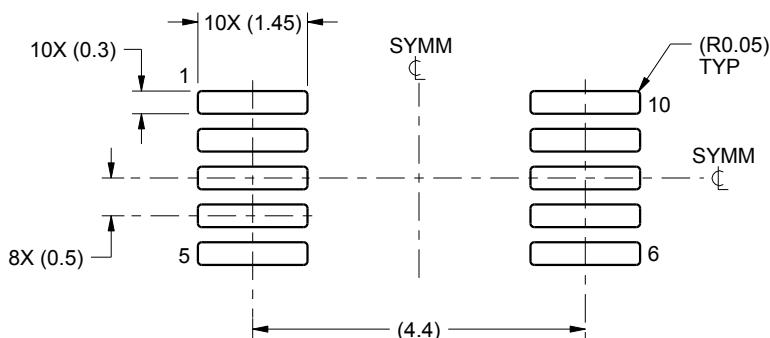
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

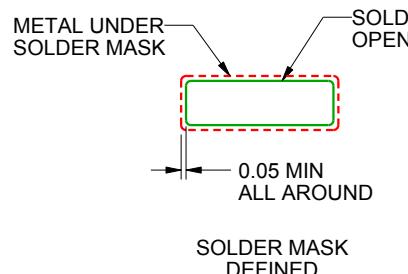
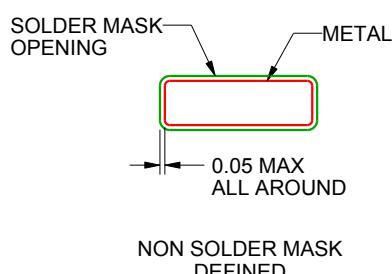
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

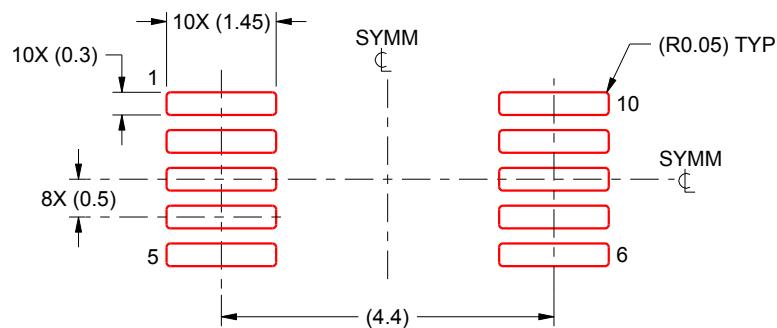
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

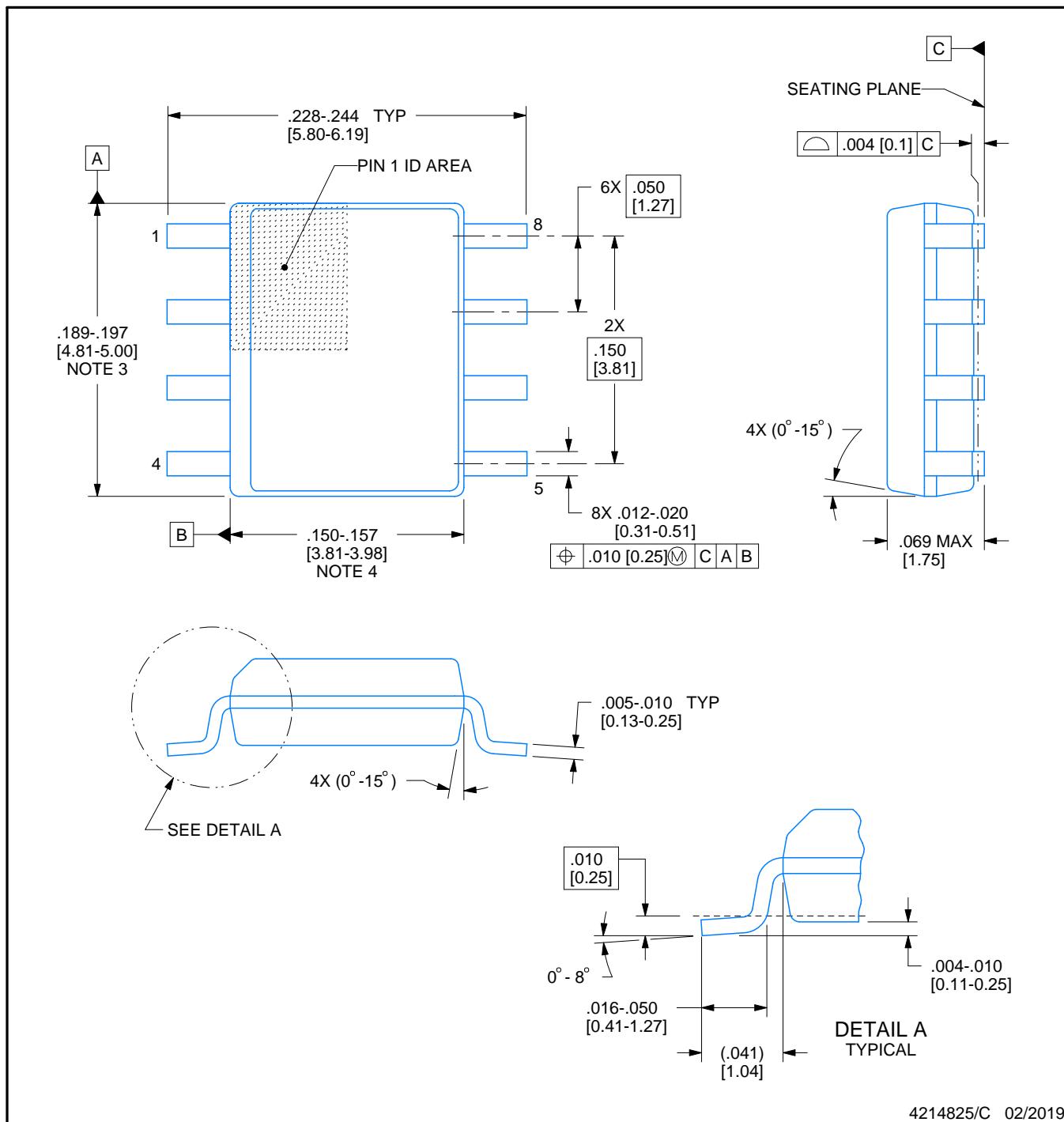


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

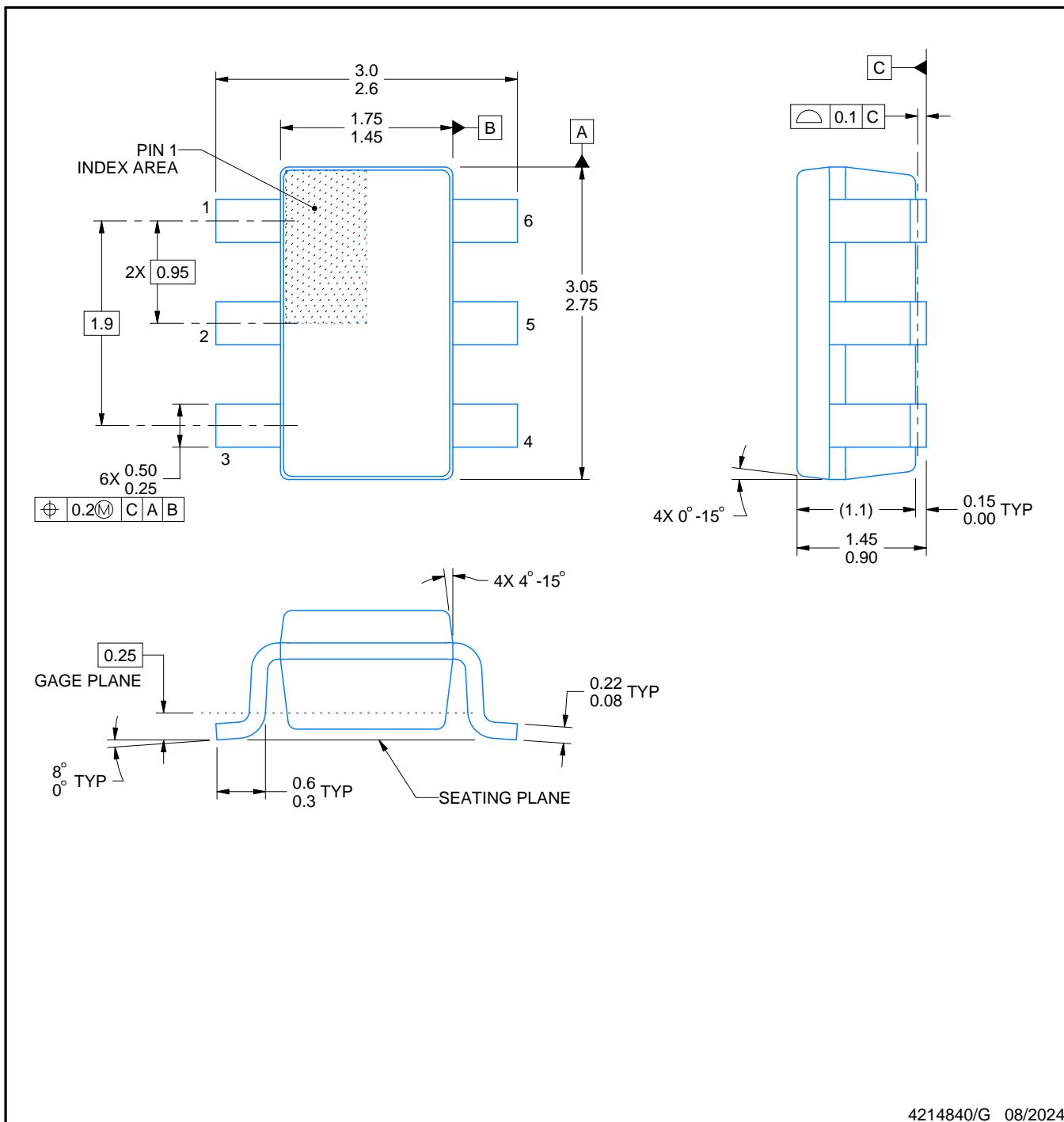
PACKAGE OUTLINE

DBV0006A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

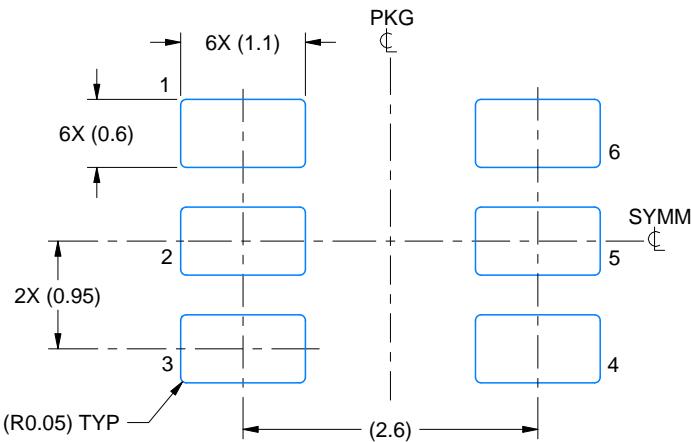
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

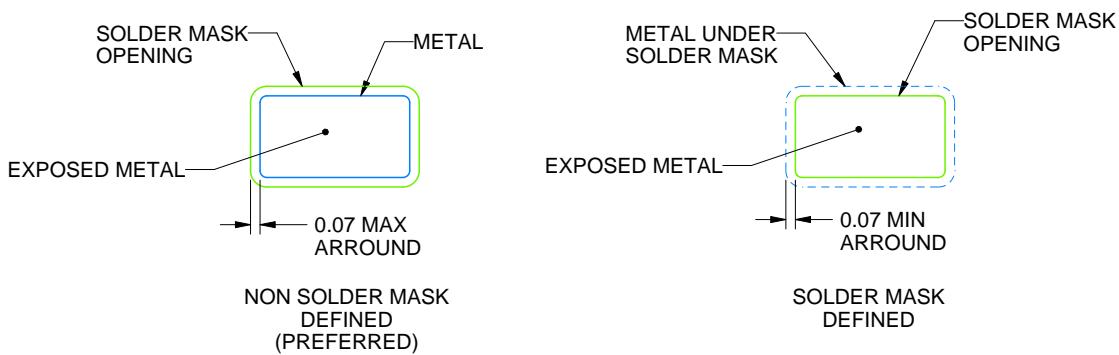
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

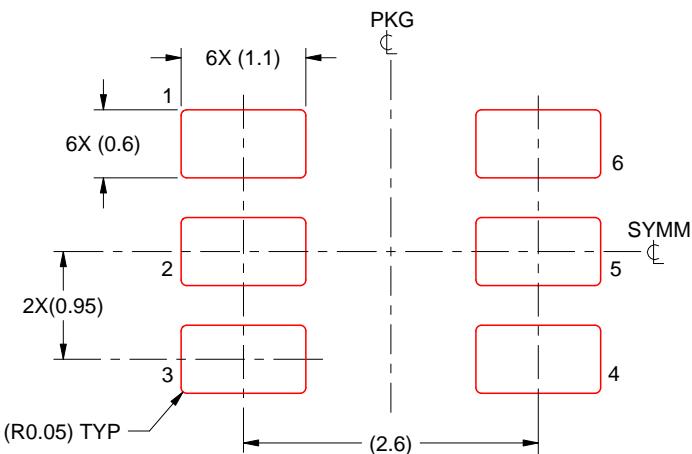
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

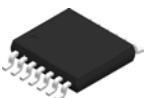
4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

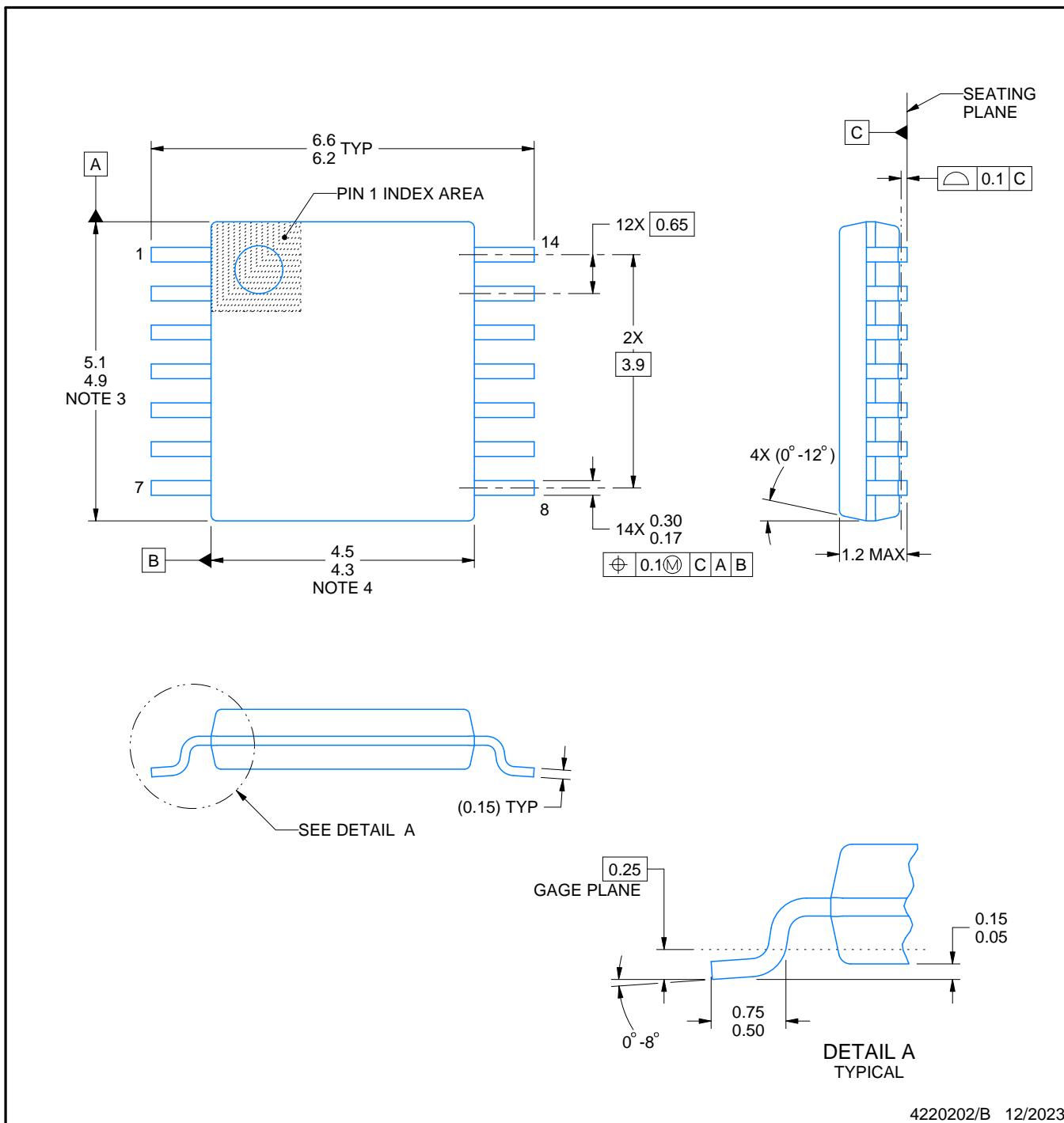
PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

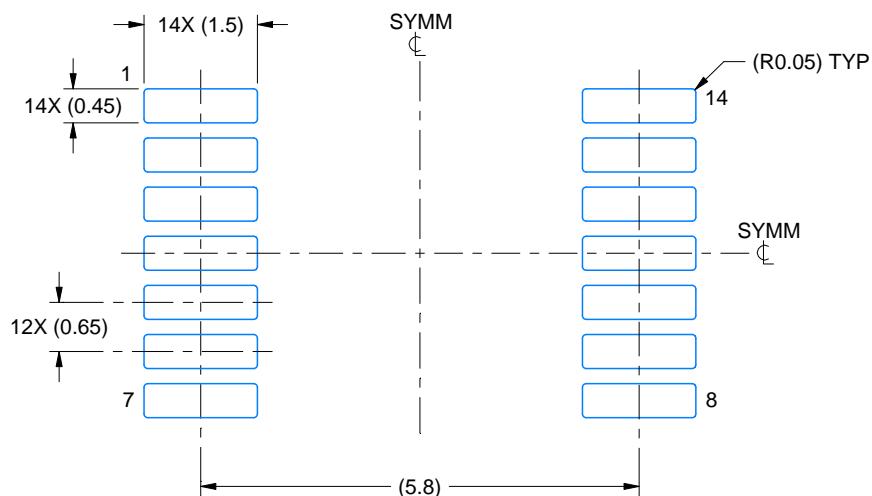
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

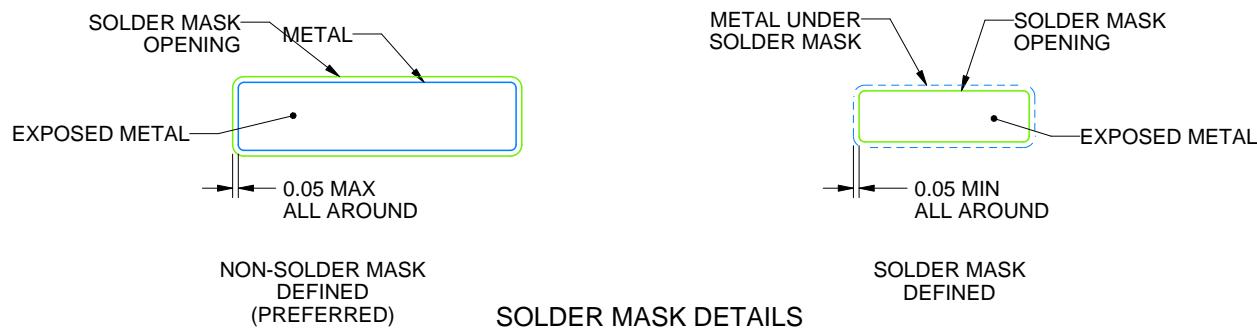
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

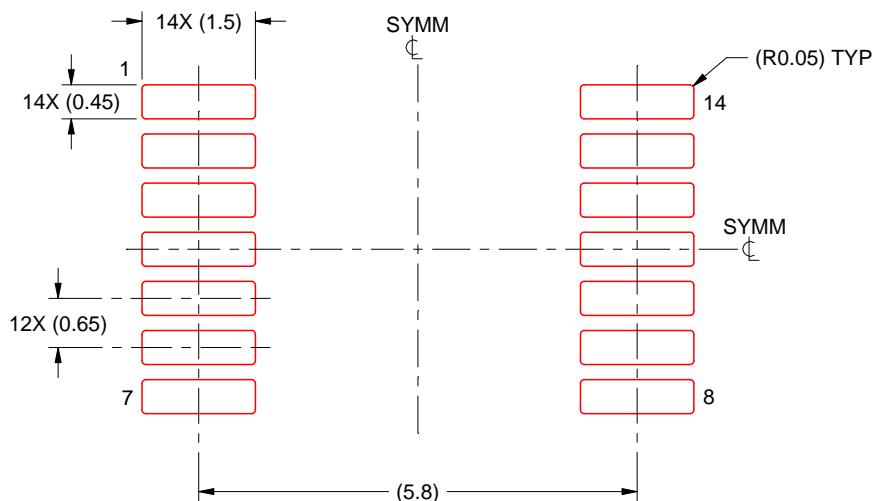
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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