

AO4615
Complementary Enhancement Mode Field Effect Transistor
General Description

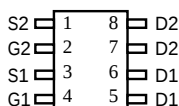
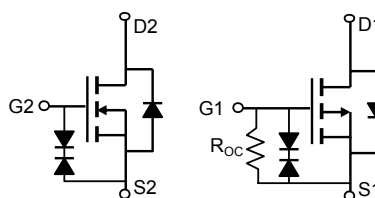
The AO4615 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications. It is ESD protected. *Standard product AO4615 is Pb-free (meets ROHS & Sony 259 specifications). AO4615L is a Green Product ordering option. AO4615 and AO4615L are electrically identical*

Features

n-channel	p-channel
$V_{DS} (V) = 30V$	-30V
$I_D = 7.2A (V_{GS}=10V)$	-5.7A ($V_{GS}=10V$)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 24m Ω ($V_{GS}=10V$)	< 39m Ω ($V_{GS} = -10V$)
< 40m Ω ($V_{GS}=4.5V$)	< 62m Ω ($V_{GS} = -4.5V$)

ESD rating: 1500V (HBM)

P-channel MOSFET has an additional $R_{OC} < 1M\Omega$ for open circuit protection.


SOIC-8

n-channel
p-channel
Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ^A	I_D	7.2	-5.7	A
$T_A=25^\circ C$				
$T_A=70^\circ C$		6.1	-4.9	
Pulsed Drain Current ^B	I_{DM}	30	-30	
Power Dissipation	P_D	2	2	W
$T_A=25^\circ C$				
$T_A=70^\circ C$		1.44	1.44	
Avalanche Current ^B	I_{AR}	15	20	A
Repetitive avalanche energy 0.1mH ^B	E_{AR}	11	20	mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ C$

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	n-ch	55	$^\circ C/W$
$t \leq 10s$			62.5	
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	n-ch	92	$^\circ C/W$
Steady-State			110	
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	n-ch	37	$^\circ C/W$
Steady-State			50	
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	p-ch	48	$^\circ C/W$
$t \leq 10s$			62.5	
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	p-ch	87	$^\circ C/W$
Steady-State			110	
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	p-ch	37	$^\circ C/W$
Steady-State			50	

N-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1	2	3	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	20			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =7.2A T _J =125°C		20 29	24 35	mΩ
		V _{GS} =4.5V, I _D =4A		30	40	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =4A	10	18		S
V _{SD}	Diode Forward Voltage	I _S =1A		0.77	1	V
I _S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		522	630	pF
C _{oss}	Output Capacitance			110		pF
C _{rss}	Reverse Transfer Capacitance			75		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		2.1	3	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =7.2A		11	15	nC
Q _g (4.5V)	Total Gate Charge			5.3	7	nC
Q _{gs}	Gate Source Charge			1.9		nC
Q _{gd}	Gate Drain Charge			4		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =2.1Ω, R _{GEN} =3Ω		4.7	7	ns
t _r	Turn-On Rise Time			4.9	10	ns
t _{D(off)}	Turn-Off DelayTime			16.2	22	ns
t _f	Turn-Off Fall Time			3.5	7	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =7.2A, dI/dt=100A/μs		15.7	20	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =7.2A, dI/dt=100A/μs		7.9	10	nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t_s 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient. R_{θJL} and R_{θJC} are equivalent terms referring to thermal resistance from junction to drain lead.

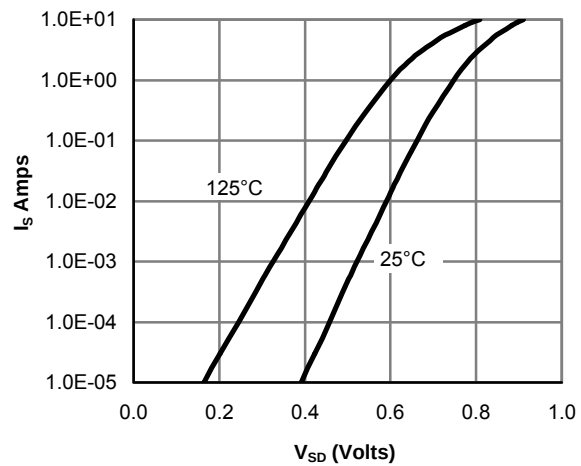
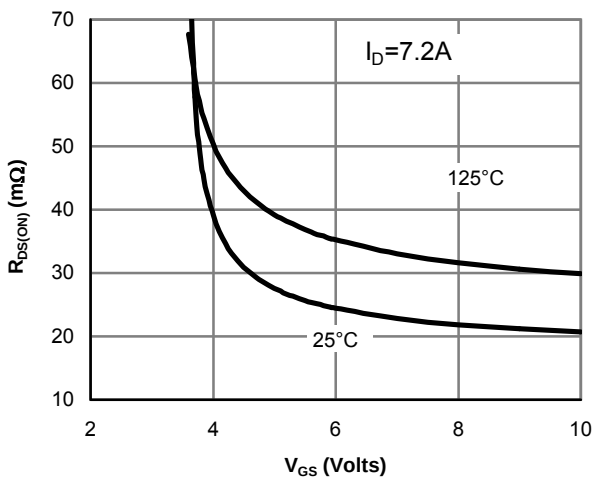
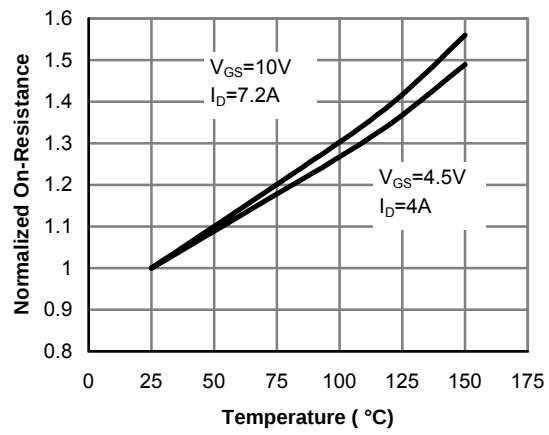
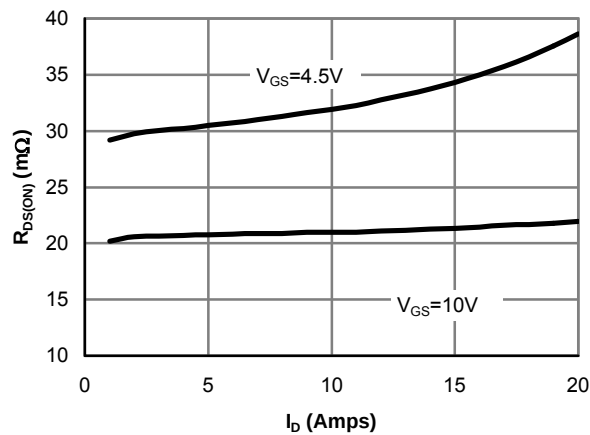
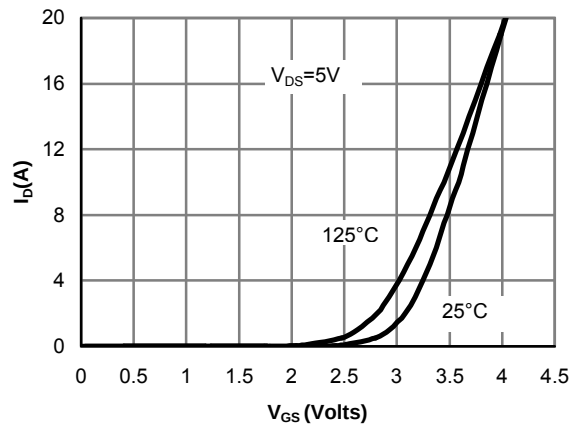
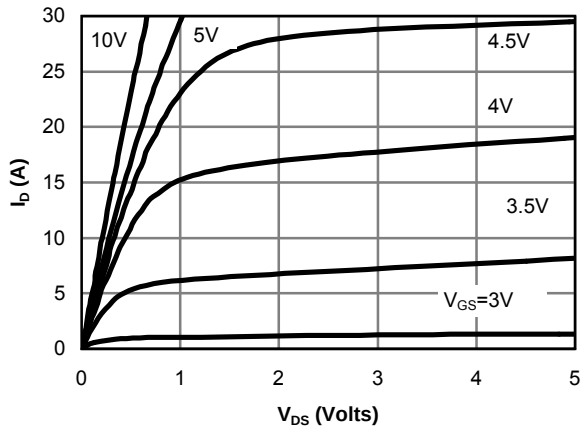
D: The static characteristics in Figures 1 to 6 are obtained using 80μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F: Rev 0: July 2005

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

N-CH TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



N-CH TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

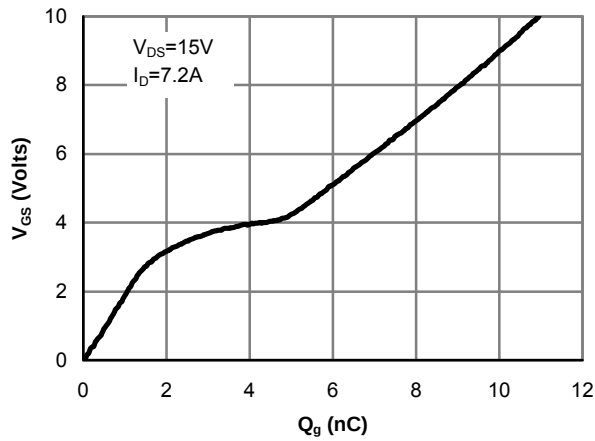


Figure 7: Gate-Charge characteristics

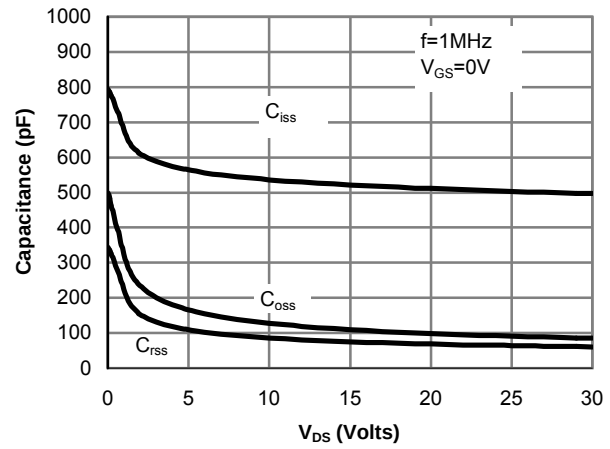


Figure 8: Capacitance Characteristics

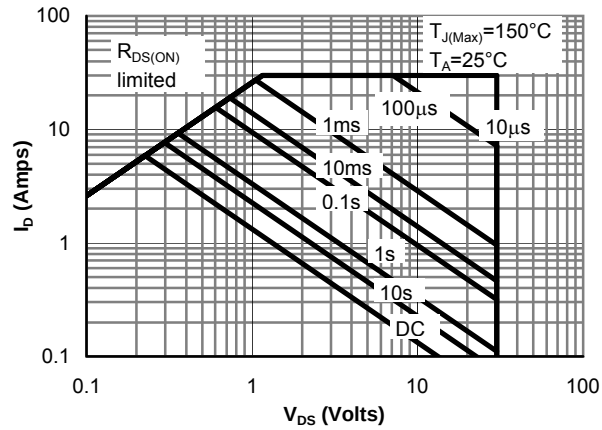


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

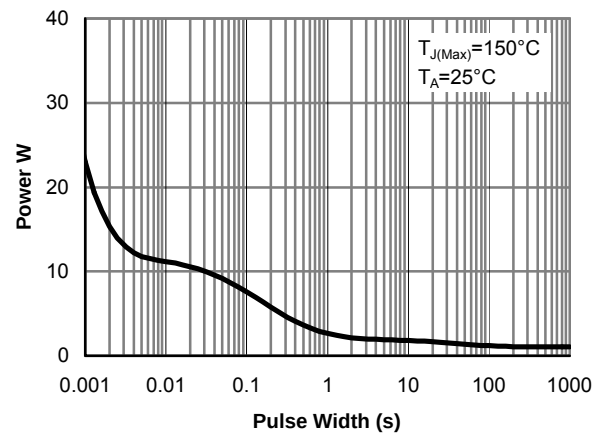


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

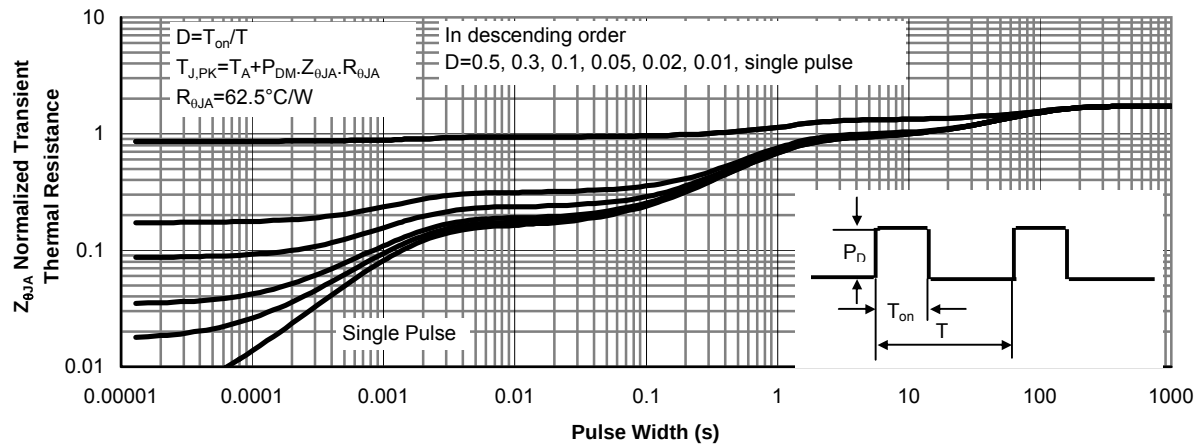


Figure 11: Normalized Maximum Transient Thermal Impedance

P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±5V			15	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1	-2	-3	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-5.7A T _J =125°C		32 46	39 56	mΩ
		V _{GS} =-4.5V, I _D =-4A		48	62	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-5.7A		13		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.77	-1	V
I _S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		1035	1250	pF
C _{oss}	Output Capacitance			161		pF
C _{rss}	Reverse Transfer Capacitance			99		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		4.5	10	Ω
R _{oc}	Open-circuit protection resistance	V _{GS} =5V	0.5	0.7	1	MΩ
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge (10V)	V _{GS} =-10V, V _{DS} =-15V, I _D =-5.7A		18	24	nC
Q _g (4.5V)	Total Gate Charge (4.5V)			8.9	12	nC
Q _{gs}	Gate Source Charge			3.8		nC
Q _{gd}	Gate Drain Charge			4.1		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-15V, R _L =2.6Ω, R _{GEN} =3Ω		8	11	ns
t _r	Turn-On Rise Time			6	12	ns
t _{D(off)}	Turn-Off DelayTime			19.5	26	ns
t _f	Turn-Off Fall Time			5.9	12	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-5.7A, dI/dt=100A/μs		20.2	27	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-5.7A, dI/dt=100A/μs		13.5	18	nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the ts 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient. R_{θJL} and R_{θJC} are equivalent terms referring to thermal resistance from junction to drain lead.

D: The static characteristics in Figures 1 to 6,12,14 are obtained using 80μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F: Rev 0: July 2005

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

P-CH TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

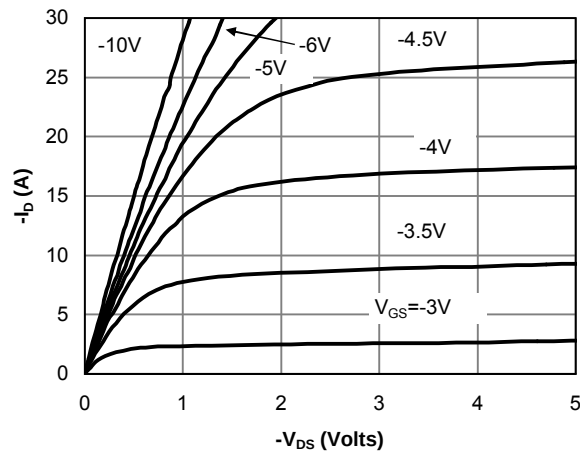


Fig 1: On-Region Characteristics

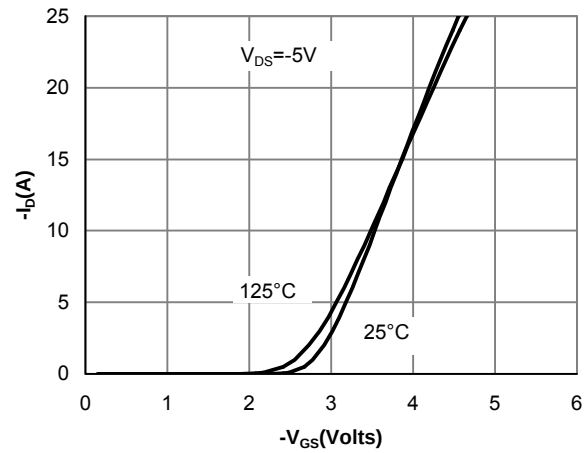


Figure 2: Transfer Characteristics

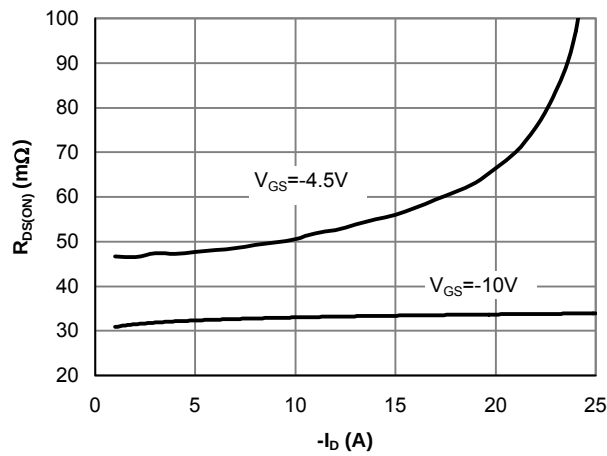


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

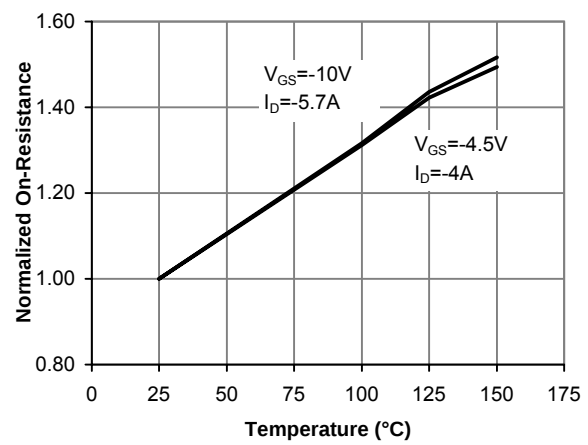


Figure 4: On-Resistance vs. Junction Temperature

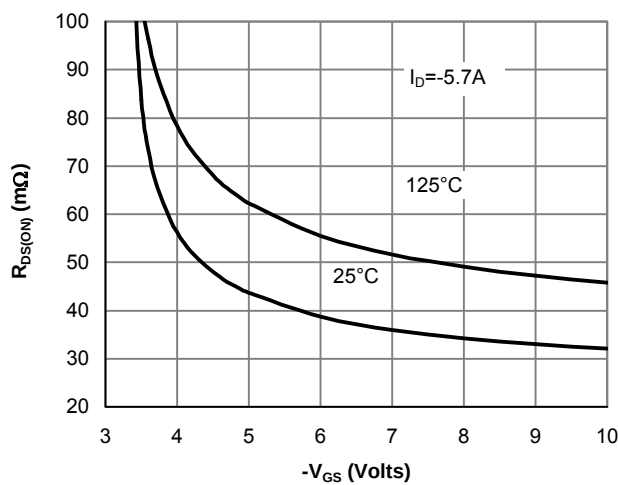


Figure 5: On-Resistance vs. Gate-Source Voltage

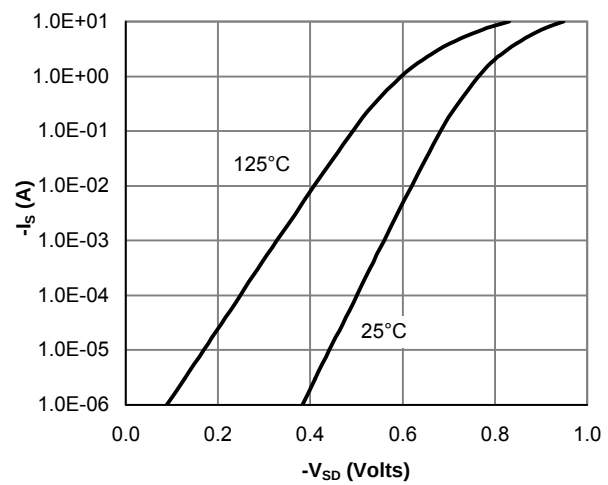


Figure 6: Body-Diode Characteristics

P-CH TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

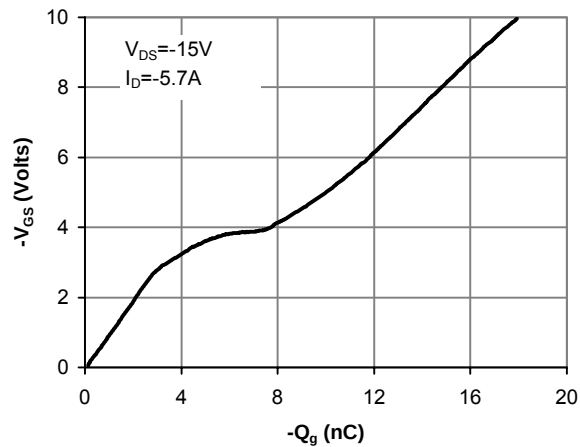


Figure 7: Gate-Charge Characteristics

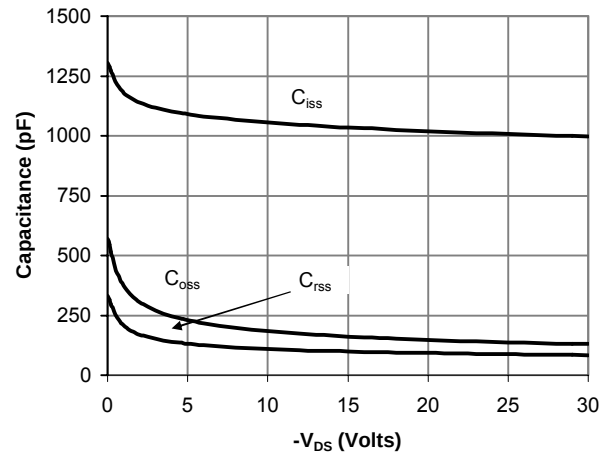


Figure 8: Capacitance Characteristics

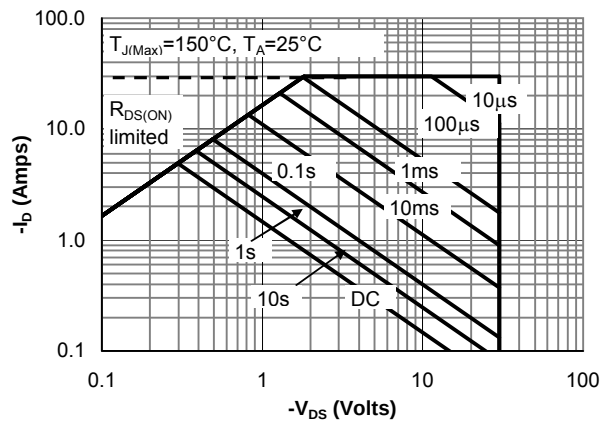


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

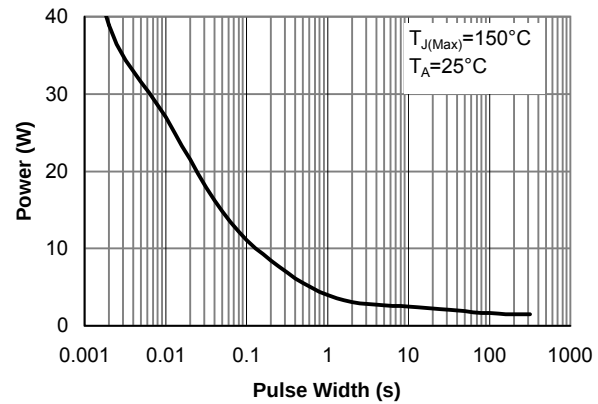


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

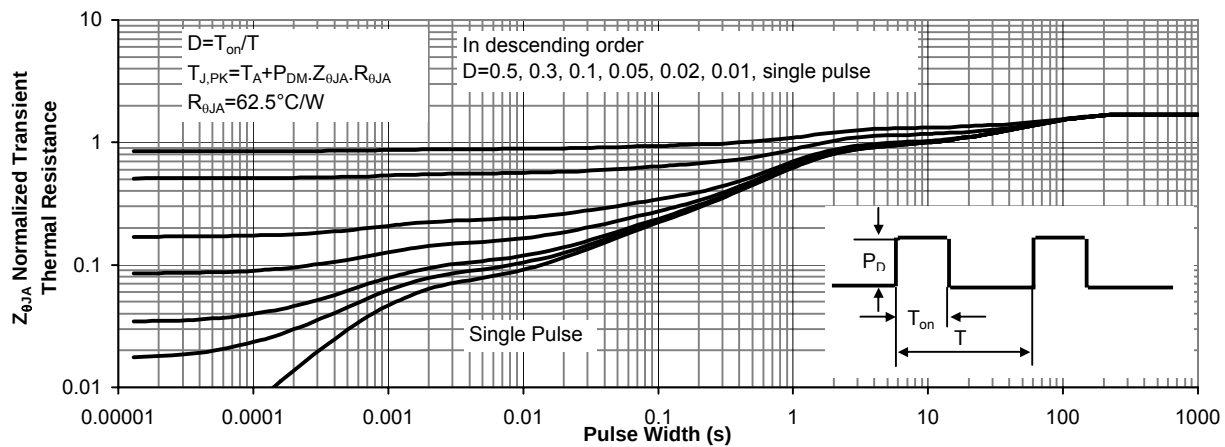


Figure 11: Normalized Maximum Transient Thermal Impedance