

CMOS 8-Bit Microcontroller

TMP87CS64F, TMP87CP64F, TMP87CM64F

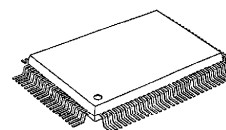
The 87CS64/CP64/CM64 are the high speed and high performance 8-bit single chip microcomputers. These MCU contain CPU core, large ROM, RAM, input/output ports, a 8-bit A/d converter, six multi-function timer/counters, three serial interfaces, and two clock generators on chip.

Part No	ROM	RAM	Package	OTP MCU
TMP87CS64F	60 K × 8-bit	2 K × 8-bit	P-QFP100-1420-0.65A	TMP87PS64F
TMP87CP64F	48 K × 8-bit			
TMP87CM64F	32 K × 8-bit			

Features

- ◆ 8-bit single chip microcomputer TLCS-870 Series
- ◆ Instruction execution time: 0.5 μ s (at 8.0 MHz / 4.5 V to 5.5 V)
0.95 μ s (at 4.2 MHz / 2.7 V to 5.5 V)
122 μ s (at 32 kHz / 2.7 V to 5.5 V)
- ◆ 412 basic instructions
 - Multiplication and Division (8bits × 8bits, 16bits ÷ 8bits): 3.5 μ s (at 8.0 MHz)
 - Bit manipulations (Set/Clear/Complement/Load/Store/Test/Exclusive OR)
 - 16-bit data operations
 - 1-byte jump/subroutine-call (Short relative jump / Vector call)
- ◆ 15 interrupt sources (External: 5, Internal: 9, External/Internal: 1)
 - All sources have independent latches each, and nested interrupt control is available.
 - 3 edge-selectable external interrupts with noise reject
 - High-speed task switching by register bank changeover
- ◆ 12 Input/Output ports (90 pins)
 - High current output: 16 pins (typ. 20 mA)
- ◆ Two 16-bit Timer/Counters
 - Timer, Event counter, Programmable pulse generator output, Pulse width measurement, External trigger timer, Window modes
- ◆ Three 8-bit Timer/Counters
 - Timer, Event counter, Capture (Pulse width/duty measurement), PWM output, Programmable divider output modes
- ◆ Time Base Timer (Interrupt frequency: 1 Hz to 16 kHz)
- ◆ Divider output function (frequency: 1 kHz to 8 kHz)
- ◆ Watchdog Timer
- ◆ Three 8-bit Serial Interfaces
 - Each 8 bytes transmit/receive data buffer (2 channels)
 - Each 32 bytes transmit/receive data buffer (1 channels)
 - Internal/external serial clock, and 4/8-bit mode
- ◆ 8-bit successive approximate type A/D converter with sample and hold
 - 16 analog inputs
 - Conversion time: 23 μ s (at 8.0 MHz)

P-QFP100-1420-0.65A



TMP87CS64F
TMP87CP64F
TMP87CM64F
TMP87PS64F

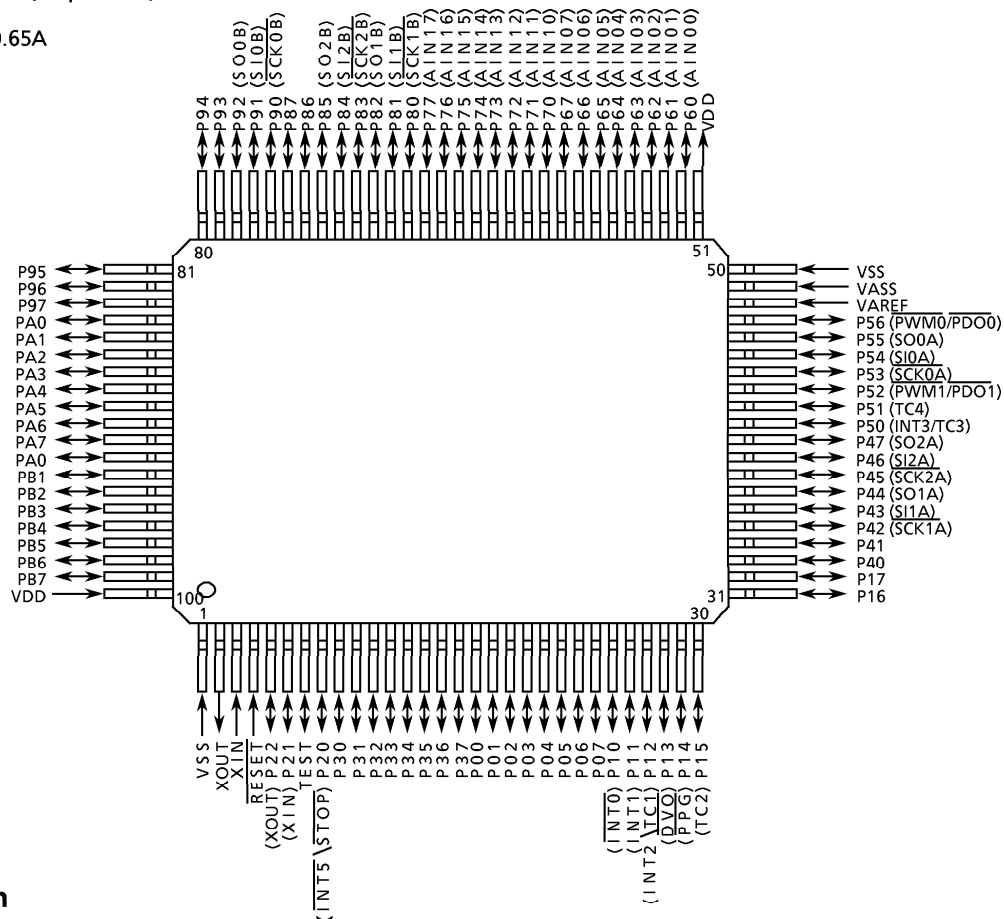
980910EBP2

- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.
- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

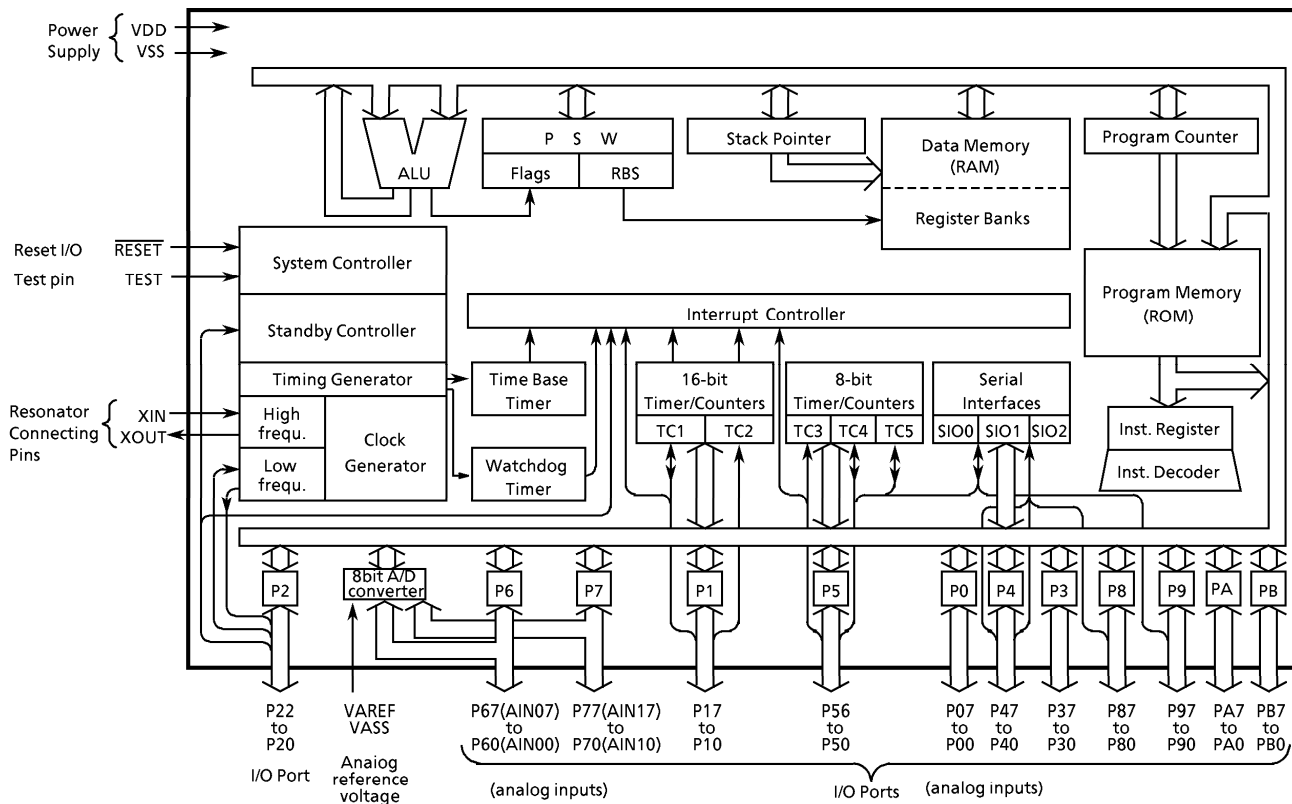
- ◆ Dual clock operation
- ◆ Five Power saving operating modes
 - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/high-impedance.
 - SLOW mode: Low power consumption operation on low-frequency clock (32.768 kHz).
 - IDLE1 mode: CPU Stops, and Peripherals operation using low-frequency clock. Release by interrupts.
 - IDLE2 mode: CPU Stops, and Peripherals operate using high and low frequency clock. Release by interrupts.
 - SLEEP mode: CPU Stops, and Peripherals operate using low-frequency clock. Release by interrupts.
- ◆ Emulation Pod: BM87CS64F0A

Pin Assignments (Top View)

P-QFP100-1420-0.65A



Block Diagram



Pin Function

Pin Name	Input / Output	Function	
P07 - P00	I/O	8-bit programmable input/output port (tri-state).	
P17, P16			
P15 (TC2)	I/O (Input)	Each bit of these ports can be individually configured as an input or an output under software control.	Timer/Counter 2 input
P14 (PPG)	I/O (Output)		Programmable pulse generator output
P13 (DVO)			Divider output
P12 (INT2/TC1)	I/O (Input)		External interrupt input 2 or Timer/Counter 1 input
P11 (INT1)		When used as timer/counter input or external interrupt input, the latch must be set to "0". When used as PPG output or divider output, the latch must be set to "1".	External interrupt input 1
P10 (INT0)			External interrupt input 0
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch.	Resonator connecting pins (32.8 kHz). For inputting external clock, XTIN is used and XTOUT is opened.
P21 (XTIN)	I/O (Input)	When used as input port, the latch must be set to "1".	
P20 (INT5/STOP)			
			External interrupt input 5 or STOP mode release signal input.
P37 - P30	I/O	8-bit input/output port (high current output port) with latch.	
		When used as input port, the latch must be set to "1".	
P47 (SO2A)	I/O (Output)	8-bit input/output port with latch.	SIO2 serial data output A
P46 (SI2A)	I/O (Input)	When used as input port or SIO input/output port, the latch must be set to "1".	SIO2 serial data input A
P45 (SCK2A)	I/O (I/O)		SIO2 serial clock input/output A
P44 (SO1A)	I/O (Output)		SIO1 serial data output A
P43 (SI1A)	I/O (Input)		SIO1 serial data input A
P42 (SCK1A)	I/O (I/O)		SIO1 serial clock input/output A
P41, P40	I/O		
P56 (PWM0/PDO0)	I/O (Output)		8-bit PWM (Timer/Counter 4) output or 8-bit programmable divider output
P55 (SO0A)			SIO0 serial data output A
P54 (SI0A)	I/O (Input)	When used as input port or SIO input/output port or PWM output or divider output or external interrupt or timer/counter input, the latch must be set to "1".	SIO0 serial data input A
P53 (SCK0A)	I/O (I/O)		SIO0 serial clock input/output A
P52 (PWM1/POD1)	I/O (Output)		8-bit PWM (Timer/Counter 5) output or 8-bit programmable divider output
P51 (TC4)	I/O (Input)		Timer/Counter 4 input
P50 (INT3/TC3)			External interrupt input 3 or Timer/Counter 3 input
P67 (AIN07)	I/O (Input)	Two 8-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. When used as analog input, the latch must be set to "0".	A/D converter analog inputs
-			
P60 (AIN00)			
P77 (AIN17)			
-			
P70 (AIN10)			
P87, P86	I/O	Two 8-bit input/output port with latch.	
P85 (SO2B)	I/O (Output)	When used as input port or SIO input/output port, the latch must be set to "1".	SIO2 serial data output B
P84 (SI2B)	I/O (Input)		SIO2 serial data input B
P83 (SCK2B)	I/O (I/O)		SIO2 serial clock input/output B
P82 (SO1B)	I/O (Output)		SIO1 serial data output B
P81 (SI1B)	I/O (Input)		SIO1 serial data input B
P80 (SCK1B)	I/O (I/O)		SIO1 serial clock input/output B
P97 - P93	I/O		
P92 (SO0B)	I/O (Output)		SIO0 serial data output B
P91 (SI0B)	I/O (Input)		SIO0 serial data input B
P90 (SCK0B)	I/O (I/O)		SIO0 serial clock input/output B
PA7 - PA0	I/O	8-bit input/output port with latch. When used as input port, the latch must be set to "1".	
PB7 - PB0		8-bit input/output port (high current output port) with latch. When used as input port, the latch must be set to "1".	
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
RESET	Input	Reset signal input or watchdog timer output/address-trap-reset output.	
TEST		Test pin for out-going test. Be fixed to low.	
VDD, VSS	Power Supply	+ 2.7 V to 5.5 V, 0 V (GND)	
VAREF, VASS		Analog reference voltage inputs (High, Low)	

OPERATIONAL DESCRIPTION

1. CPU CORE FUNCTIONS

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLC870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the 87CS64/CP64/CM64. In the TLC870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

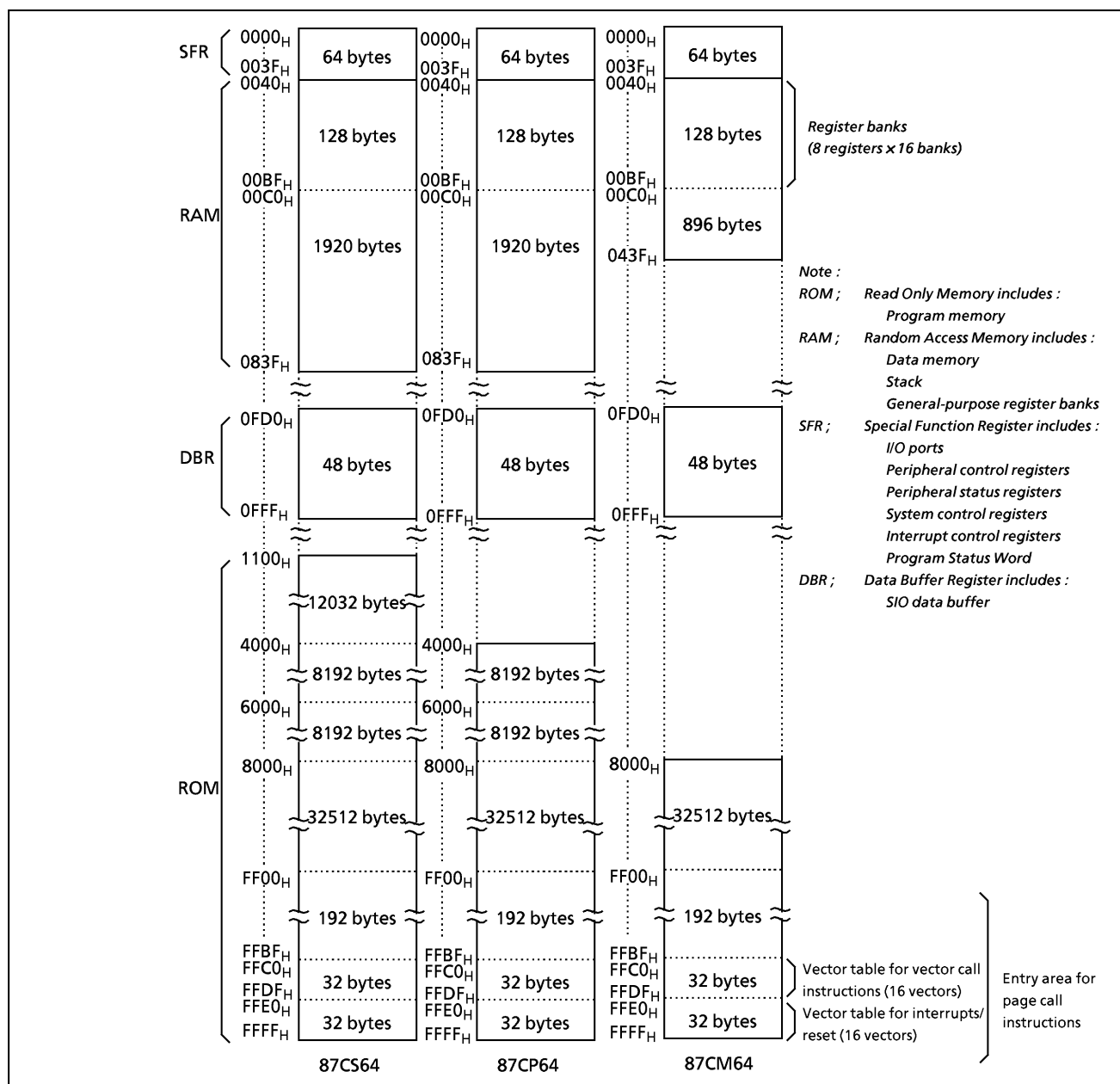


Figure 1-1. Memory Address Maps

Electrical Characteristics

Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V _{DD}		– 0.3 to 6.5	V
Input Voltage	V _{IN}		– 0.3 to V _{DD} + 0.3	V
Output Voltage	V _{OUT1}		– 0.3 to V _{DD} + 0.3	V
	V _{OUT2}		– 0.3 to 5.5	
Output Current (Per 1pin)	I _{OUT1}	Ports P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, PA	3.2	mA
	I _{OUT2}	Port P3, PB	30	
Output Current (Total)	Σ I _{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7, P8, P9, PA	175	mA
	Σ I _{OUT2}	Port P3, PB	120, 120	
Power Dissipation [T _{opr} = 70°C]	PD		350	mW
Soldering Temperature (time)	T _{sld}		260 (10 s)	°C
Storage Temperature	T _{stg}		– 55 to 125	°C
Operating Temperature	T _{opr}		– 30 to 60	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions

(V_{SS} = 0 V, T_{opr} = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V _{DD}		fc = 8 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 mode			
			fc = 4.2 MHz	NORMAL1, 2 mode	2.7		
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
	STOP mode	2.0					
Input High Voltage	V _{IH1}	Except hysteresis input	V _{DD} ≥ 4.5 V		V _{DD} × 0.70	V _{DD}	V
	V _{IH2}	Hysteresis input			V _{DD} × 0.75		
	V _{IH3}		V _{DD} < 4.5 V	V _{DD} × 0.90			
Input Low Voltage	V _{IL1}	Except hysteresis input	V _{DD} ≥ 4.5 V		0	V _{DD} × 0.30	V
	V _{IL2}	Hysteresis input				V _{DD} × 0.25	
	V _{IL3}		V _{DD} < 4.5 V	V _{DD} × 0.10			
Clock Frequency	fc	XIN, XOUT	V _{DD} = 4.5 to 5.5 V		0.4	8.0	MHz
			V _{DD} = 2.7 to 5.5 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating Conditions for a device are operating Conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating Conditions other than the recommended operating Conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating Conditions for the device are always adhered to.

Note2: Clock frequency fc ; The supply voltage range of the Conditions shows the value in NORMAL1, 2 modes and IDLE1, 2 modes.

D.C. Characteristics

(V_{SS} = 0 V, T_{opr} = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V _{HS}	Hysteresis inputs	V _{DD} = 5.0 V	–	0.9	–	V
Input Current	I _{IN1}	TEST	V _{DD} = 5.5 V V _{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I _{IN2}	Open drain ports					
	I _{IN3}	Tri-state ports					
Input Low Current	I _{IL}	Push-pull ports	V _{DD} = 5.5 V, V _{IN} = 0.4 V	–	–	–	mA
Input Resistance	R _{IN2}	RESET		100	220	450	kΩ
Output Leakage Current	I _{LO1}	Sink open drain ports	V _{DD} = 5.5 V, V _{OUT} = 5.5 V	–	–	2	μA
	I _{LO2}	Tri-state ports	V _{DD} = 5.5 V, V _{OUT} = 5.5 V / 0 V	–	–	± 2	
Output High Voltage	V _{OL1}	Push-pull ports	V _{DD} = 4.5 V, I _{OH} = – 200 μA	2.4	–	–	V
	V _{OH2}	Tri-state ports	V _{DD} = 4.5 V, I _{OH} = – 0.7 mA	4.1	–	–	
Output Low Voltage	V _{OL}	Except XOUT and port P3, PB	V _{DD} = 4.5 V, I _{OL} = 1.6 mA	–	–	0.4	
Output Low current	I _{OL3}	Port P3, PB	V _{DD} = 4.5 V, V _{OL} = 1.0 V	–	20	–	V
Supply Current in NORMAL 1, 2 mode	I _{DD}		V _{DD} = 5.5 V f _c = 8 MHz f _s = 32.768 kHz V _{IN} = 5.3 V / 0.2 V	–	11	14	
Supply Current in IDLE 1, 2 mode				–	6	9	
Supply Current in NORMAL 1, 2 mode			V _{DD} = 3.0 V f _c = 4.19 MHz f _s = 32.768 kHz V _{IN} = 2.8 V / 0.2 V	–	3.5	5.0	mA
Supply Current in IDLE 1, 2 mode				–	2.5	3	
Supply Current in SLOW mode			V _{DD} = 3.0 V f _s = 32.768 kHz V _{IN} = 2.8 V / 0.2 V	–	30	60	μA
Supply Current in SLEEP mode				–	15	30	μA
Supply Current in STOP mode			V _{DD} = 5.5 V V _{IN} = 5.3 V / 0.2 V	–	0.5	10	μA

Note 1: Typical values show those at T_{opr} = 25 °C.

Note 2: Input Current ; The current through pull-up or pull-down resistor is not included.

Note 3: I_{DD} ; Except for I_{REF}

A / D Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, T_{opr} = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V _{AREF}	V _{AREF} – V _{ASS} ≥ 2.5 V	2.7	—	V _{DD}	V
	V _{ASS}		V _{SS}	—	1.5	
Analog Input Voltage	V _{AIN}		V _{ASS}	—	V _{AREF}	V
Analog Supply Current	I _{REF}	V _{AREF} = 5.5 V, V _{ASS} = 0.0 V	—	0.5	1.0	mA
Nonlinearity Error		V _{DD} = 5.0 V, V _{SS} = 0 V V _{AREF} = 5.000 V	—	—	± 1	LSB
Zero Point Error		V _{ASS} = 0.000 V or	—	—	± 1	
Full Scale Error		V _{DD} = 2.7 V, V _{SS} = 0 V V _{AREF} = 2.700 V	—	—	± 1	
Total Error		V _{ASS} = 0.000 V	—	—	± 2	

Note: Total Error = total number of each type error excluding quantization error.

A.C. Characteristics

(V_{SS} = 0 V, T_{opr} = – 40 to 85°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t _{cy}	In NORMAL1, 2 mode	0.5	—	10	μs
		In IDLE1, 2 mode				
		In SLOW mode	117.6	—	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t _{WCH}	For external clock operation (XIN input), f _c = 8 MHz	50	—	—	ns
Low Level Clock Pulse Width	t _{WCL}					
High Level Clock Pulse Width	t _{WSH}	For external clock operation (XTIN input), f _s = 32.768 kHz	14.7	—	—	μs
Low Level Clock Pulse Width	t _{WSL}					

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, T_{opr} = – 30 to 70°C)

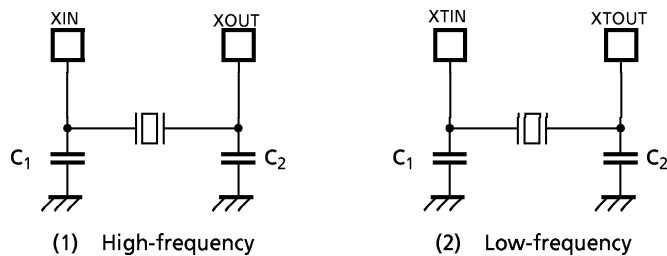
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t _{cy}	In NORMAL1, 2 mode	0.95	—	10	μs
		In IDLE1, 2 mode				
		In SLOW mode	117.6	—	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t _{WCH}	For external clock operation (XIN input), f _c = 4.2 MHz	110	—	—	ns
Low Level Clock Pulse Width	t _{WCL}					
High Level Clock Pulse Width	t _{WSH}	For external clock operation (XTIN input), f _s = 32.768 kHz	14.7	—	—	μs
Low Level Clock Pulse Width	t _{WSL}					

Recomended Oscillating Condition-1 (VSS = 0 V, VDD = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Osillator	Frequency	Recommender Oscillator		Recommended Condition	
					C ₁	C ₂
High-frequency	Ceramic Resonator	8 MHz	KYOCERA	KBR8.0M	30 pF	30 pF
			Standard/Lead Type (MURATA)	CSA8.00MTZ CST8.00MTW	built-in 30 pF	built-in 30 pF
			Standard/SMP Type (MURATA)	CSACS8.00MT	30 pF	30 pF
			Standard/Small ChipType (MURATA)	CSTCS8.00MT	built-in 30 pF	built-in 30 pF
	Crystal Oscillator	4 MHz	KYOCERA	KBR4.0MS	30 pF	30 pF
		8 MHz	TOYOCOM	210B 8.0000	20 pF	20 pF
		4 MHz	TOYOCOM	204B 4.0000		
Low-frequency	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15 pF	15 pF

Recomended Oscillating Condition-2 (VSS = 0 V, VDD = 2.7 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Osillator	Frequency	Recommender Oscillator		Recommended Condition	
					C ₁	C ₂
High-frequency	Ceramic Resonator	4 MHz	Standard/Lead Type (MURATA)	CSA4.00MG CST4.00MGW	30 pF built-in 30 pF	30 pF built-in 30 pF
			Standard/SMD Type (MURATA)	CSA4.00MGC CSAC4.00MGCM CSTC4.00MG	30 pF built-in 30 pF	30 pF built-in 30 pF
			Standard/Small Chip Type	CSTCS4.00MG	built-in 10 pF	built-in 10 pF



Note: When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations.