NEC

MOS FIELD EFFECT TRANSISTOR
2SK3204

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK3204 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3204	MP-10

FEATURES

- Low on-state resistance :
  $R_{DS(on)1}$ = 34 mΩ MAX. (V_{GS} = 10 V, I_D = 8 A)
  $R_{DS(on)2}$ = 50 mΩ MAX. (V_{GS} = 4 V, I_D = 8 A)
- Low C_{iss} : C_{iss} = 940 pF TYP.
- Built-in gate protection diode.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	60	V
Gate to Source Voltage (V_{DS} = 0 V)	$V_{GSS(AC)}$	±20	V
Gate to Source Voltage (V_{DS} = 0 V)	$V_{GSS(DC)}$	+20, –10	V
Drain Current (DC) (T_C = 25 °C)	$I_{D(DC)}$	±15	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±45	A
Total Power Dissipation (T_A = 25°C)	P_T	1.8	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	15	A
Single Avalanche Energy Note2	E_{AS}	22.5	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

★ **2.** Starting T_{ch} = 25°C, V_{DD} = 30 V, R_G = 25 Ω, V_{GS} = 20 → 0 V

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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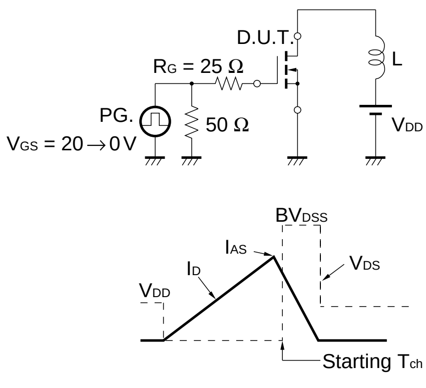
The mark ★ shows major revised points.

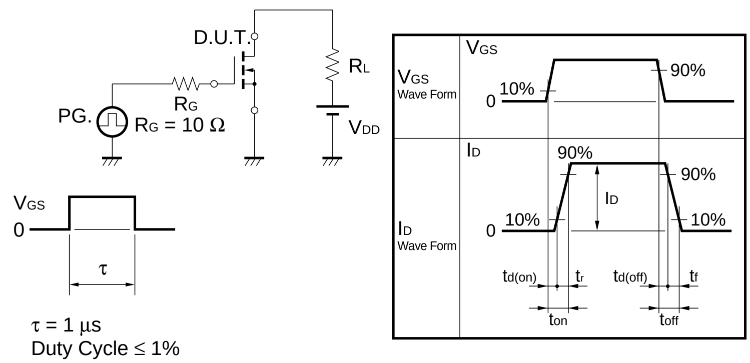
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PARAMATERS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	$\| y_{fs} \|$	V_{DS} = 10 V, I_D = 8 A	8.0	14		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 8 A		25	34	mΩ
	$R_{DS(on)2}$	V_{GS} = 4 V, I_D = 8 A		35	50	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		940		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		290		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		120		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 8 A		17		ns
Rise Time	t_r	V_{GS} = 10 V		150		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		58		ns
Fall Time	t_f			52		ns
Total Gate Charge	Q_G	V_{DD} = 48 V		25		nC
Gate to Source Charge	Q_{GS}	$V_{GS(on)}$ = 10 V		2.9		nC
Gate to Drain Charge	Q_{GD}	I_D = 15 A		7.5		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 15 A, V_{GS} = 0 V		0.92		V
Reverse Recovery Time	t_{rr}	I_F = 15 A, V_{GS} = 0 V		45		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		81		nC

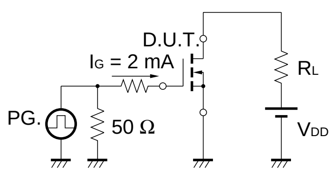
TEST CIRCUIT 1 AVALANCHE CAPABILITY



★ TEST CIRCUIT 2 SWITCHING TIME

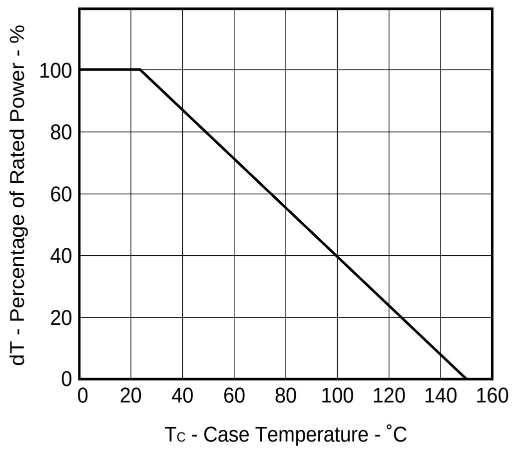


TEST CIRCUIT 3 GATE CHARGE

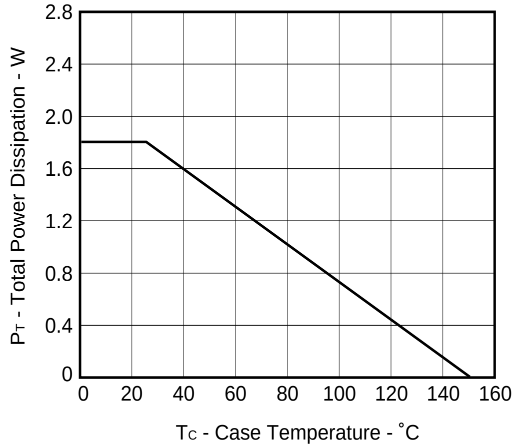


★ TYPICAL CHARACTERISTICS (T_A = 25°C)

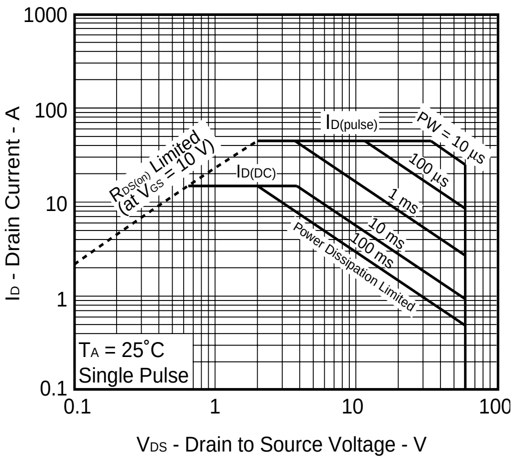
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



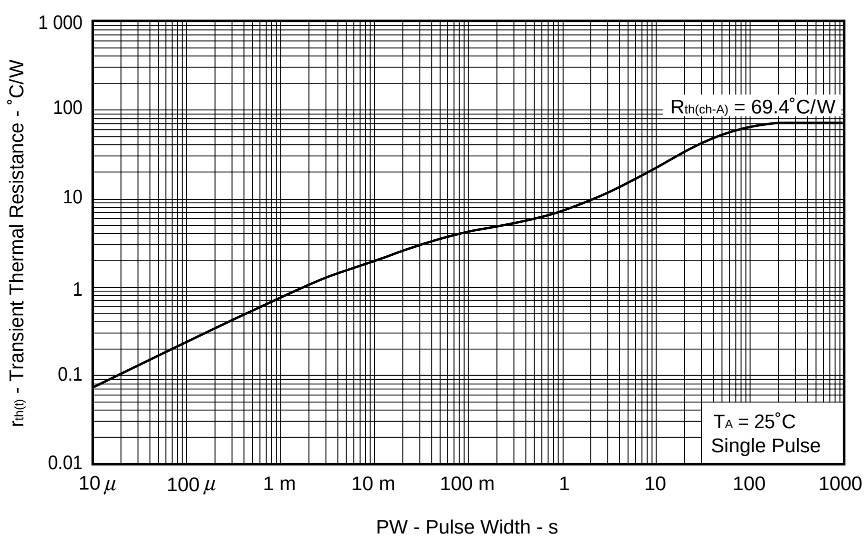
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



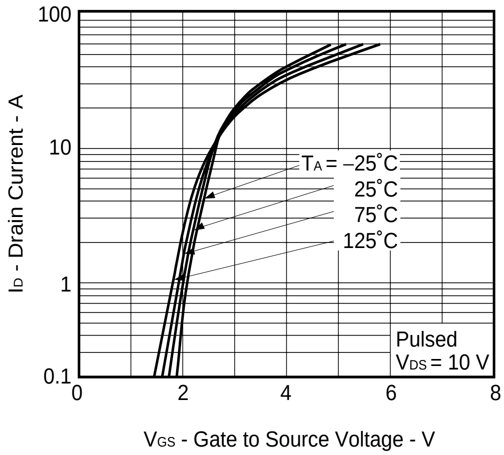
FORWARD BIAS SAFE OPERATING AREA



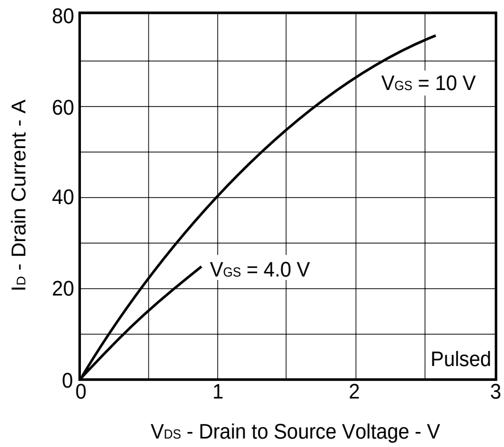
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



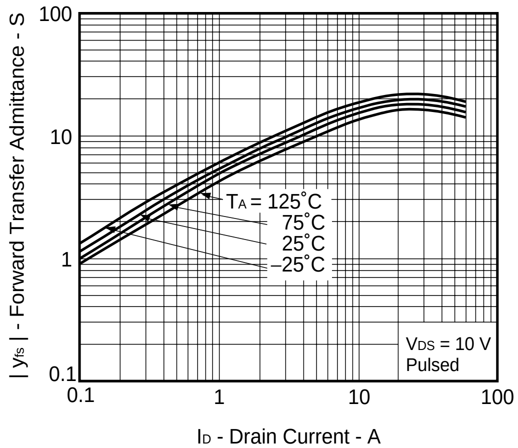
FORWARD TRANSFER CHARACTERISTICS



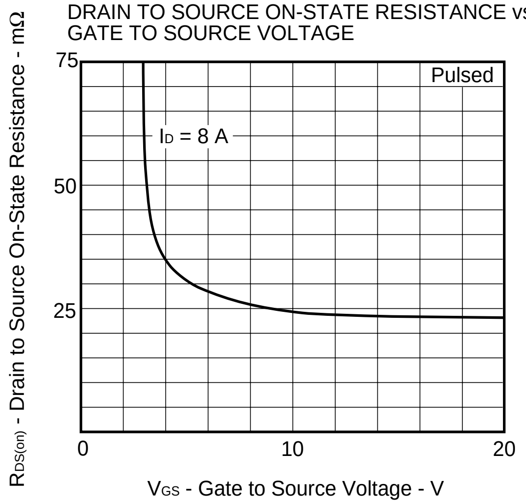
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



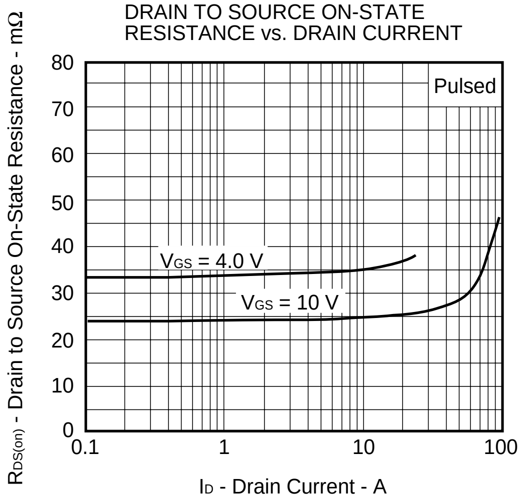
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



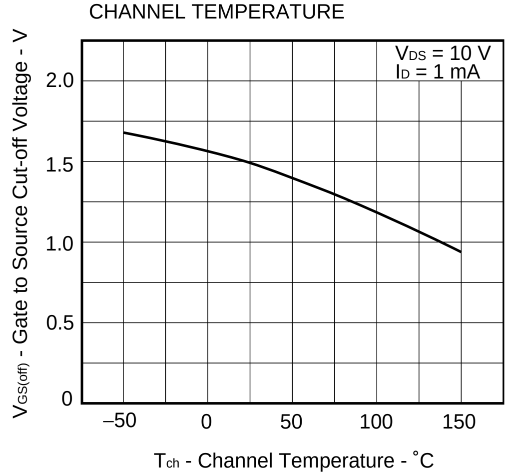
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



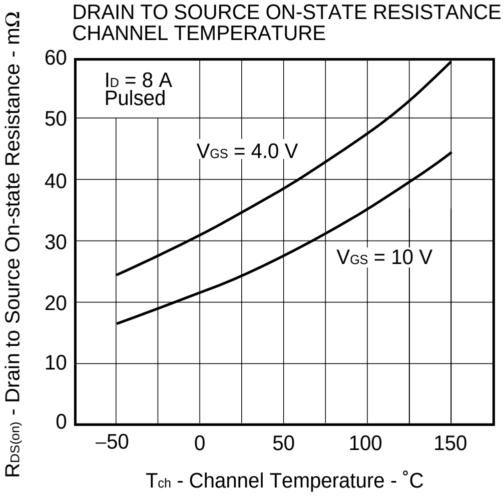
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



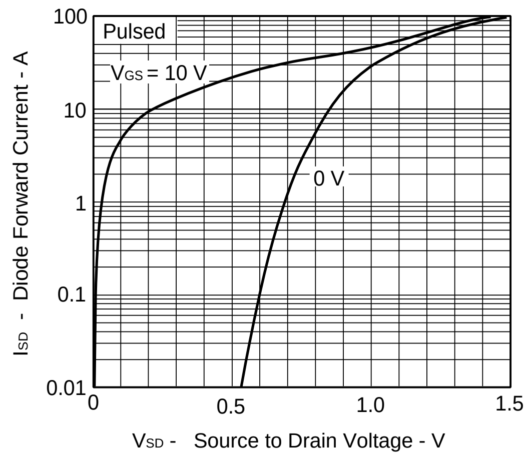
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



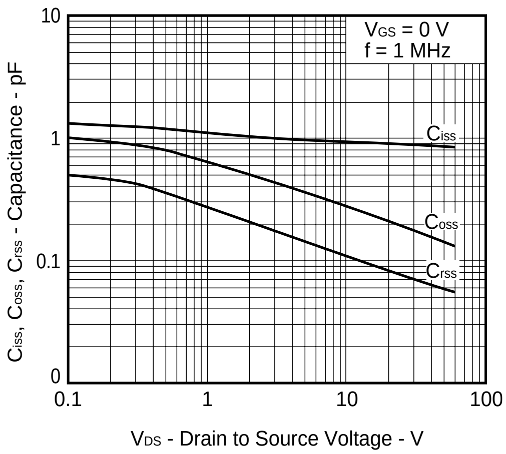
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



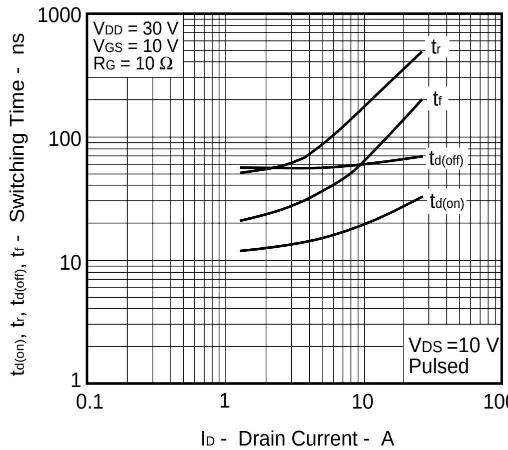
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



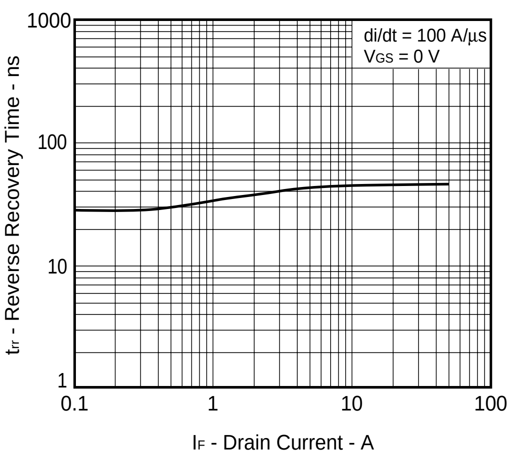
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



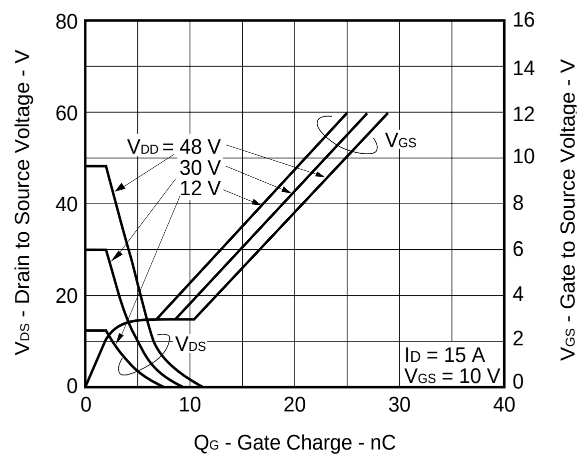
SWITCHING CHARACTERISTICS



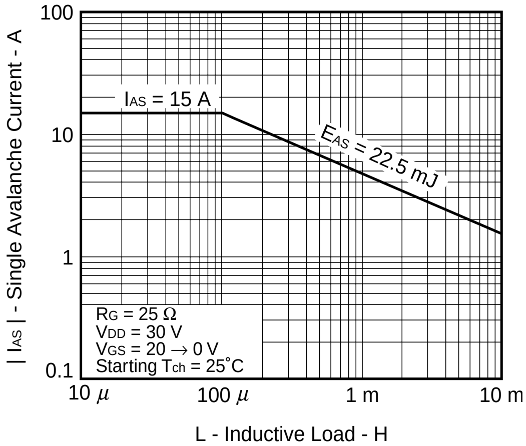
REVERSE RECOVERY TIME vs. DRAIN CURRENT



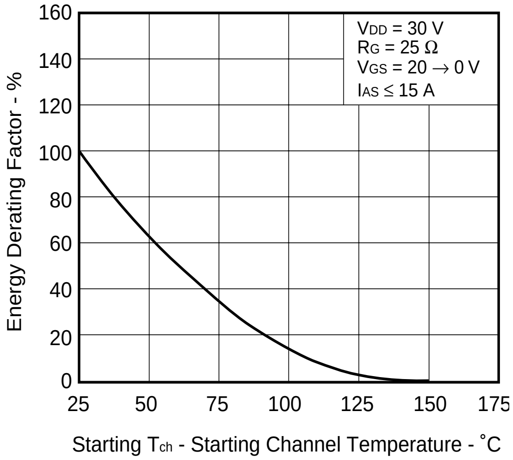
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

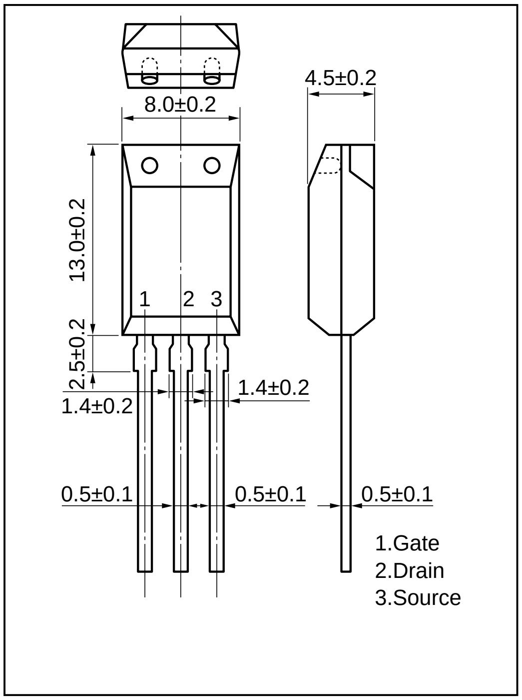


SINGLE AVALANCHE ENERGY
DERATING FACTOR

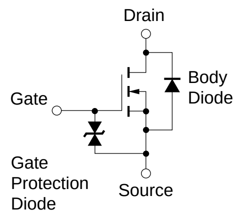


PACKAGE DRAWING (Unit: mm)

MP-10



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.