

Precision 8-Ch/Dual 4-Ch Low Voltage Analog Multiplexers

DESCRIPTION

The DG408L, DG409L are low voltage pin-for-pin compatible companion devices to the industry standard DG408, DG409 with improved performance.

Using BiCMOS wafer fabrication technology allows the DG408L, DG409L to operate on single and dual supplies. Single supply voltage ranges from 3 V to 12 V while dual supply operation is recommended with ± 3 V to ± 6 V.

The DG408L is an 8 channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3 bit binary address (A_0 , A_1 , A_2). The DG409L is a dual 4 channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2 bit binary address (A_0 , A_1). Break-before-make switching action to protect against momentary crosstalk between adjacent channels.

The DG408L, DG409L provides lower on-resistance, faster switching time, lower leakage, less power consumption and higher off-Isolation than the DG408, DG409.

FEATURES

- **Halogen-free according to IEC 61249-2-21 Definition**
- Pin-for-pin compatibility with DG408, DG409
- 2.7 V to 12 V single supply or ± 3 V to ± 6 V dual supply operation
- Lower on-resistance: $R_{DS(ON)}$ - 17 Ω typ.
- Fast switching: t_{ON} - 38 ns, t_{OFF} - 18 ns
- Break-before-make guaranteed
- Low leakage: $I_{S(off)}$ - 0.2 nA max.
- Low charge injection: 1 pC
- TTL, CMOS, LV logic (3 V) compatible
- 82 dB off-isolation at 1 MHz
- 2000 V ESD protection (HBM)
- **Compliant to RoHS Directive 2002/95/EC**



RoHS*
COMPLIANT
HALOGEN
FREE

BENEFITS

- High accuracy
- Single and dual power rail capacity
- Wide operating voltage range
- Simple logic interface

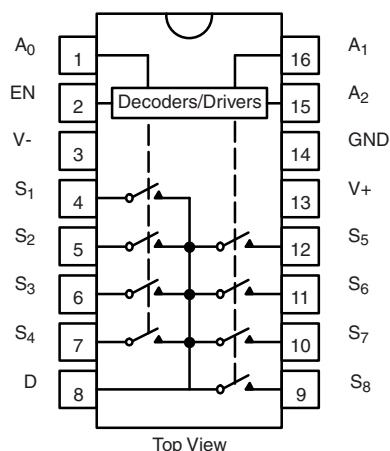
APPLICATIONS

- Data acquisition systems
- Battery operated equipment
- Portable test equipment
- Sample and hold circuits
- Communication systems
- SDSL, DSLAM
- Audio and video signal routing

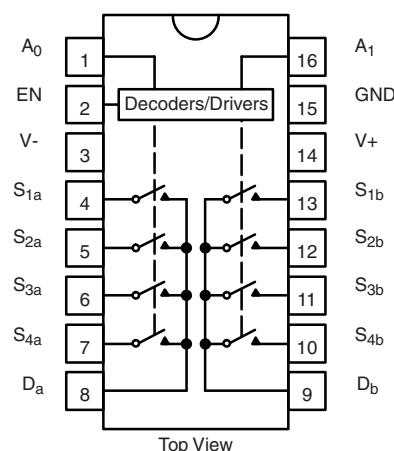
FUNCTIONAL BLOCK DIAGRAMS AND PIN CONFIGURATIONS

DG408L

Dual-In- Line, SOIC and TSSOP


DG409L

Dual-In- Line, SOIC and TSSOP



* Pb containing terminations are not RoHS compliant, exemptions may apply

TRUTH TABLE DG408L				
A ₂	A ₁	A ₀	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE DG409L			
A ₁	A ₀	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{AL} \leq 0.8\text{ V}$
 Logic "1" = $V_{AH} \geq 2.4\text{ V}$
 X = Do not Care

For low and high voltage levels for V_{AX} and V_{EN} consult "Digital Control" parameters for specific V+ operation.

ORDERING INFORMATION DG408L		
Temp. Range	Package	Part Number
- 40 °C to 85 °C	16-pin SOIC	DG408LDY DG408LDY-E3 DG408LDY-T1 DG408LDY-T1-E3
	16-pin TSSOP	DG408LDQ DG408LDQ-E3 DG408LDQ-T1 DG408LDQ-T1-E3

ORDERING INFORMATION DG409L		
Temp. Range	Package	Part Number
- 40 °C to 85 °C	16-pin SOIC	DG409LDY DG409LDY-E3 DG409LDY-T1 DG409LDY-T1-E3
	16-pin TSSOP	DG409LDQ DG409LDQ-E3 DG409LDQ-T1 DG409LDQ-T1-E3

ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
Voltage referenced V+ to V-		14	V
GND		7	
Digital inputs ^a , V _S , V _D		(V-) - 0.3 to (V) + 0.3	
Current (any terminal)		30	mA
Peak current, S or D (pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage Temperature	(A suffix)	- 65 to 150	°C
	(D suffix)	- 65 to 125	
Power Dissipation (Package) ^b	16-pin plastic TSSOP ^c	650	mW
	16-pin narrow SOIC ^c	600	
	16-pin CerDIP ^d	900	
	LCC-20 ^e	750	

Notes:

- Signals on S_X, DX, A_X, or EN exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads soldered or welded to PC board.
- Derate 7.6 mW/°C above 75 °C.
- Derate 12 mW/°C above 75 °C.
- Derate 10 mW/°C above 75 °C.

**SPECIFICATIONS** (Single Supply 12 V)

		Test Conditions Unless Otherwise Specified V+ = 12 V, ± 10 %, V- = 0 V V _{EN} = 0.8 V or 2.4 V ^f			A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		
Parameter	Symbol		Temp. ^b	Typ. ^d	Min. ^c	Max. ^c	Min. ^c	Max. ^c	Unit
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	R _{DS(on)}	V _D = 10.8 V, V _D = 2 V or 9 V, I _S = 10 mA sequence each switch on	Room Full	17		29 38		29 35	Ω
R _{DS(on)} Matching Between Channels ^g	ΔR _{DS}	V _D = 10.8 V, V _D = 2 V or 9 V I _S = 10 mA	Room	1		3		3	
On-Resistance Flatness ⁱ	R _{FLAT(on)}		Room	3		7		7	
Switch Off Leakage Current	I _{S(off)}	V _{EN} = 0 V, V _D = 11 V or 1 V V _S = 1 V or 11 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	nA
	I _{D(off)}		Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Channel On Leakage Current	I _{D(on)}	V _S = V _D = 1 V or 11 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Digital Control									
Logic High Input Voltage	V _{INH}		Full		2.4		2.4		V
Logic Low Input Voltage	V _{INL}		Full			0.8		0.8	
Input Current	I _{IN}	V _{AX} = V _{EN} = 2.4 V or 0.8 V	Full		- 1.5	1.5	- 1	1	μA
Dynamic Characteristics									
Transition Time	t _{TRANS}	V _{S1} = 8 V, V _{S8} = 0 V, (DG408L) V _{S1b} = 8 V, V _{S4b} = 0 V, (DG409L) see figure 2	Room Full	30		60 68		60 65	ns
Break-Before-Make Time	t _{OPEN}	V _{S(all)} = V _{DA} = 5 V see figure 4	Room Full	11	1		1		
Enable Turn-On Time	t _{ON(EN)}	V _{AX} = 0 V, V _{S1} = 5 V (DG408L) V _{AX} = 0 V, V _{S1b} = 5 V (DG409L) see figure 3	Room Full	38		55 60		55 60	
Enable Turn-Off Time	t _{OFF(EN)}		Room Full	18		25 35		25 30	
Charge Injection ^e	Q	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω	Room	1		5		5	pC
Off Isolation ^{e, h}	OIRR	f = 100 kHz, R _L = 1 kΩ	Room	- 70					dB
Crosstalk ^e	X _{TALK}		Room	- 82					
Source Off Capacitance ^e	C _{S(off)}	f = 1 MHz, V _S = 0 V, V _{EN} = 0 V	Room	7					pF
Drain Off Capacitance ^e	C _{D(off)}	f = 1 MHz, V _D = 2.4 V, V _{EN} = 0 V	Room	20					
Drain On Capacitance ^e	C _{D(on)}	f = 1 MHz, V _D = 0 V, V _{EN} = 2.4 V (DG409L only)	Room	31					
Power Supplies									
Power Supply Range	V+				3	12	3	12	V
Power Supply Current	I+	V _{EN} = V _A = 0 V or 5 V	Room	0.2		0.7		0.7	mA

Notes:

- a. Leakage parameters are guaranteed by worst case test condition and not subject to production test.
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Guaranteed by design, not subject to production test.
- f. V_{IN} = input voltage to perform proper function.
- g. $\Delta R_{DS(on)} = R_{DS(on)} \text{ Max} - R_{DS(on)} \text{ Min}$.
- h. Worst case isolation occurs on Channel 4 do to proximity to the drain pin.
- i. $R_{DS(on)}$ flatness is measured as the difference between the minimum and maximum measured values across a defined Analog signal.

SPECIFICATIONS (Dual Supply V+ = 5 V, V- = - 5 V)									
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, ± 10 %, V- = - 5 V VEN = 0.6 V or 2.4 V ^f	Temp. ^b	Typ. ^d	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
					Min. ^c	Max. ^c	Min. ^c	Max. ^c	
Analog Switch									
Analog Signal Range ^e	VANALOG		Full		- 5	5	- 5	5	V
Drain-Source On-Resistance	RDS(on)	VD = ± 3.5 V, IS = 10 mA sequence each switch on	Room Full	20		40 50		40 50	Ω
Switch Off Leakage Current ^a	IS(off)	V+ = 5.5 V, V- = 5.5 V VEN = 0 V, VD = ± 4.5 V, VS = ± 4.5 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	nA
	ID(off)		Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Channel On Leakage Current ^a	ID(on)	V+ = 5.5 V, V- = - 5.5 V VEN = 2.4 V, VD = ± 4.5 V, VS = ± 4.5 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Digital Control									
Logic High Input Voltage	VINH		Full		2.4		2.4		V
Logic Low Input Voltage	VINL		Full			0.6		0.6	
Input Current ^a	IIN	VAX = VEN = 2.4 V or 0.6 V	Full		- 1.5	1.5	- 1	1	μA
Dynamic Characteristics									
Transition Time ^e	tTRANS	VS1 = 3.5 V, VS8 = - 3.5 V, (DG408L) VS1b = 3.5 V, VS4b = - 3.5 V, (DG409L) see figure 2	Room Full	30		60 78		60 65	ns
Break-Before-Make Time ^e	tOPEN	VS(all) = VDA = 3.5 V see figure 4	Room Full	8	1		1		
Enable Turn-On Time ^e	tON(EN)	VAX = 0 V, VS1 = 3.5 V (DG408L) VAX = 0 V, VS1b = 3.5 V (DG409L) see figure 3	Room Full	25		55 68		55 60	
Enable Turn-Off Time ^e	tOFF(EN)		Room Full	20		40 50		40 45	
Source Off Capacitance ^e	CS(off)	f = 1 MHz, VS = 0 V, VEN = 0 V	Room	6					pF
Drain Off Capacitance ^e	CD(off)	f = 1 MHz, VD = 0 V, VEN = 0 V	Room	15					
Drain On Capacitance ^e	CD(on)	f = 1 MHz, VD = 0 V, VEN = 2.4 V	Room	29					

Notes:

- Leakage parameters are guaranteed by worst case test condition and not subject to production test.
- Room = 25 °C, full = as determined by the operating temperature suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.
- $\Delta R_{DS(on)} = R_{DS(on)} \text{ max.} - R_{DS(on)} \text{ min.}$
- Worst case isolation occurs on channel 4 do to proximity to the drain pin.
- $R_{DS(on)}$ flatness is measured as the difference between the minimum and maximum measured values across a defined analog signal.



SPECIFICATIONS (Single Supply 5 V)									
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, ± 10 %, V- = 0 V VEN = 0.6 V or 2.4 V ^f	Temp. ^b	Typ. ^d	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
					Min. ^c	Max. ^c	Min. ^c	Max. ^c	
Analog Switch									
Analog Signal Range ^e	VANALOG		Full		0	5	0	5	V
Drain-Source On-Resistance	RDS(on)	V+ = 4.5 V, VD or VS = 1 V or 3.5 V, ID = 5 mA	Room Full	35		49 62		40 62	Ω
RDS(on) Matching Between Channels ^g	ΔRDS	V+ = 4.5 V, VD = 1 V or 3.5 V, IS = 5 mA	Room	1.5		3		3	
On-Resistance Flatness ⁱ	RFLAT(on)		Room			4		4	
Switch Off Leakage Current ^a	IS(off)	V+ = 5.5 V, VS = 1 V or 4 V VD = 4 V or 1 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	nA
	ID(off)		Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Channel On Leakage Current ^a	ID(on)	V+ = 5.5 V, VD = VS = 1 V or 4 V sequence each switch on	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Digital Control									
Logic High Input Voltage	VINH	V+ = 5 V	Full		2.4		2.4		V
Logic Low Input Voltage	VINL		Full			0.6		0.6	
Input Current ^a	IIN	VAX = VEN = 2.4 V or 0.6 V	Full		- 1.5	1.5	- 1	1	μA
Dynamic Characteristics									
Transition Time ^e	tTRANS	VS1 = 3.5 V, VS8 = 0 V, (DG408L) VS1b = 3.5 V, VS4b = 0 V, (DG409L) see figure 2	Room Full	44		125 138		125 135	ns
Break-Before-Make Time ^e	tOPEN	VS(all) = VDA = 3.5 V, see figure 4	Room Full	17	1		1		
Enable Turn-On Time ^e	tON(EN)	VAX = 0 V, VS1 = 3.5 V (DG408L) VAX = 0 V, VS1b = 3.5 V (DG409L) see figure 3	Room Full	43		60 70		60 65	
Enable Turn-Off Time ^e	tOFF(EN)		Room Full	26		45 60		45 50	
Charge Injection ^e	Q	CL = 1 nF, RGEN = 0 Ω, VGEN = 0 Ω	Room	1		5		5	pC
Off Isolation ^{e, h}	OIRR	f = 100 kHz, RL = 1 kΩ	Room	- 70					dB
Crosstalk ^e	XTALK		Room	- 80					
Source Off Capacitance ^e	CS(off)	f = 1 MHz, VS = 0 V, VEN = 0 V	Room	8					pF
Drain Off Capacitance ^e	CD(off)	f = 1 MHz, VD = 0 V, VEN = 0 V	Room	21					
Drain On Capacitance ^e	CD(on)	f = 1 MHz, VD = 0 V, VEN = 2.4 V (DG409L only)	Room	32					

Notes:

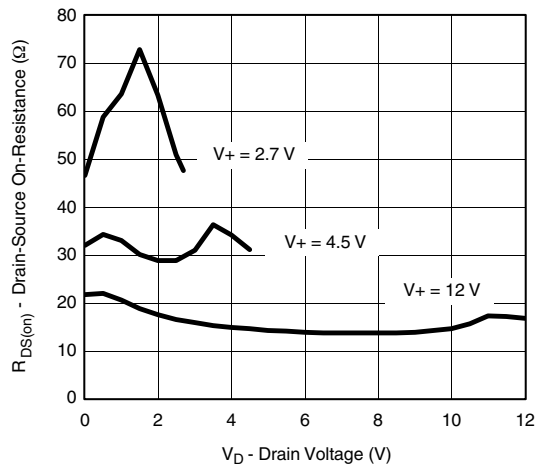
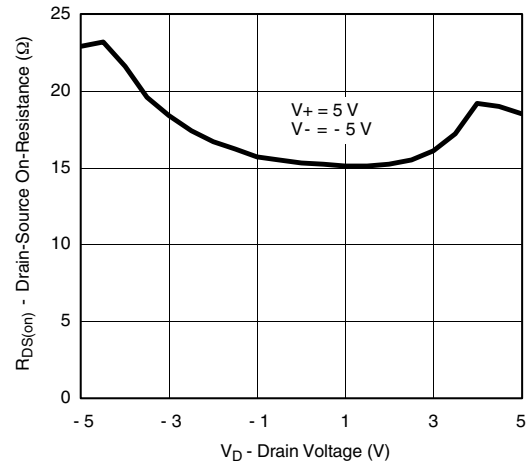
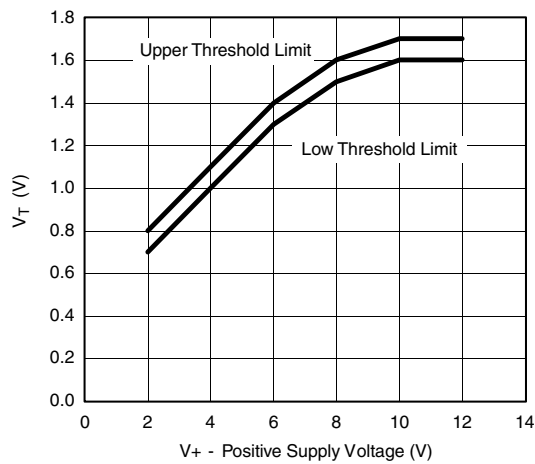
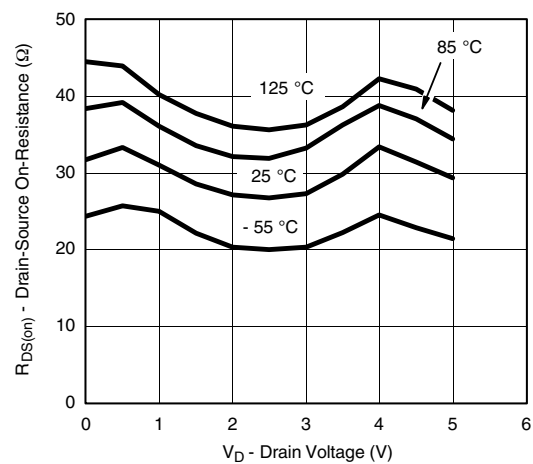
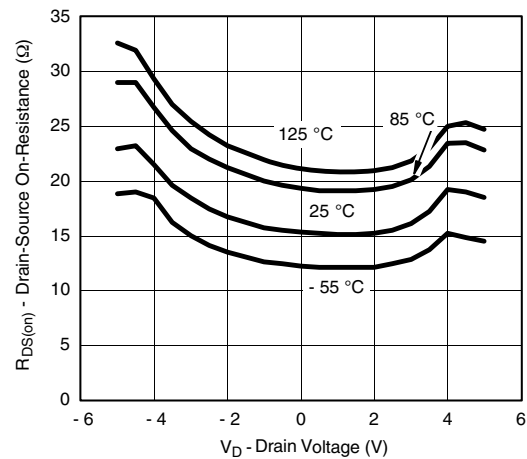
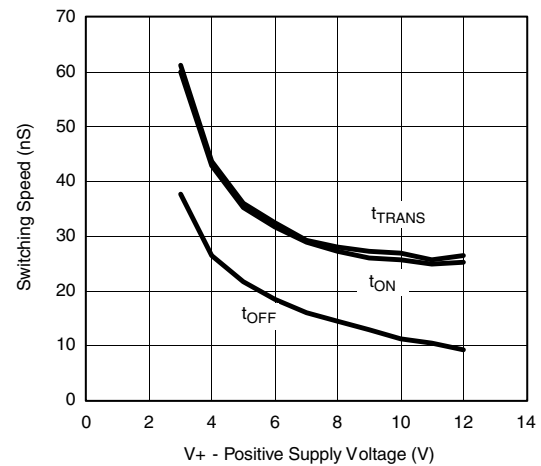
- a. Leakage parameters are guaranteed by worst case test condition and not subject to production test.
b. Room = 25 °C, full = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta R_{DS(on)} = R_{DS(on)} \text{ max.} - R_{DS(on)} \text{ min.}$
h. Worst case isolation occurs on channel 4 do to proximity to the drain pin.
i. $R_{DS(on)}$ flatness is measured as the difference between the minimum and maximum measured values across a defined analog signal.

SPECIFICATIONS (Single Supply 3 V)									
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 3 V, ± 10 %, V ₋ = 0 V V _{EN} = 0.4 V or 2 V ^f	Temp. ^b	Typ. ^d	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
					Min. ^c	Max. ^c	Min. ^c	Max. ^c	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		0	3	0	3	V
Drain-Source On-Resistance	R _{DS(on)}	V ₊ = 2.7 V, V _D = 0.5 or 2.2 V, I _S = 5 mA	Room Full	60		80 105		80 100	Ω
Switch Off Leakage Current ^a	I _{S(off)}	V ₊ = 3.3 V, V _S = 2 or 1 V, V _D = 1 or 2 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	nA
	I _{D(off)}		Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Channel On Leakage Current ^a	I _{D(on)}	V ₊ = 3.3 V, V _D = V _S = 1 or 2 V sequence each switch on	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Digital Control									
Logic High Input Voltage	V _{INH}		Full		2		2		V
Logic Low Input Voltage	V _{INL}		Full			0.4		0.4	
Input Current ^a	I _{IN}	V _{AX} = V _{EN} = 2.4 V or 0.4 V	Full		- 1.5	1.5	- 1	1	μA
Dynamic Characteristics									
Transition Time	t _{TRANS}	V _{S1} = 1.5 V, V _{S8} = 0 V, (DG408L) V _{S1b} = 1.5 V, V _{S4b} = 0 V, (DG409L) see figure 2	Room Full	75		150 175		150 175	ns
Break-Before-Make Time	t _{OPEN}	V _{S(all)} = V _{DA} = 1.5 V, see figure 4	Room Full	32	1		1		
Enable Turn-On Time	t _{ON(EN)}	V _{AX} = 0 V, V _{S1} = 1.5 V (DG408L) V _{AX} = 0 V, V _{S1b} = 1.5 V (DG409L) see figure 3	Room Full	70		95 115		95 105	
Enable Turn-Off Time	t _{OFF(EN)}		Room Full	55		100 115		100 105	
Charge Injection ^e	Q	C _L = 1 nF, R _{GEN} = 0 Ω, V _{GEN} = 0 V	Room	0.4		5		5	pC
Off Isolation ^{e, h}	OIRR	R _L = 1 kΩ, f = 100 kHz	Room	- 70					dB
Crosstalk ^e	X _{TALK}		Room	- 79					
Source Off Capacitance ^e	C _{S(off)}	f = 1 MHz, V _S = 0 V, V _{EN} = 0 V	Room	8					pF
Drain Off Capacitance ^e	C _{D(off)}	f = 1 MHz, V _D = 0 V, V _{EN} = 0 V	Room	19					
Drain On Capacitance ^e	C _{D(on)}	f = 1 MHz, V _D = 0 V, V _{EN} = 2 V (DG409L only)	Room	33					

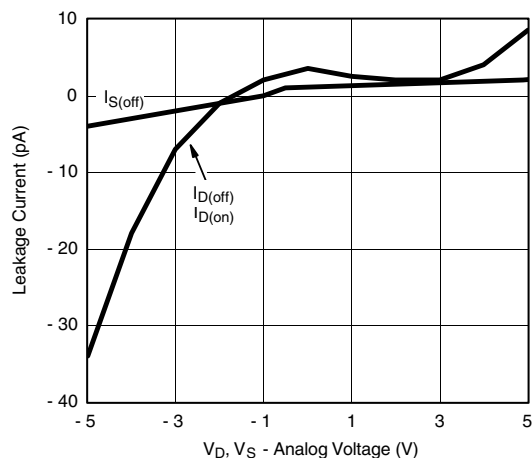
Notes:

- Leakage parameters are guaranteed by worst case test condition and not subject to production test.
- Room = 25 °C, full = as determined by the operating temperature suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.
- $\Delta R_{DS(on)} = R_{DS(on)} \text{ max.} - R_{DS(on)} \text{ min.}$
- Worst case isolation occurs on channel 4 do to proximity to the drain pin.
- $R_{DS(on)}$ flatness is measured as the difference between the minimum and maximum measured values across a defined analog signal.

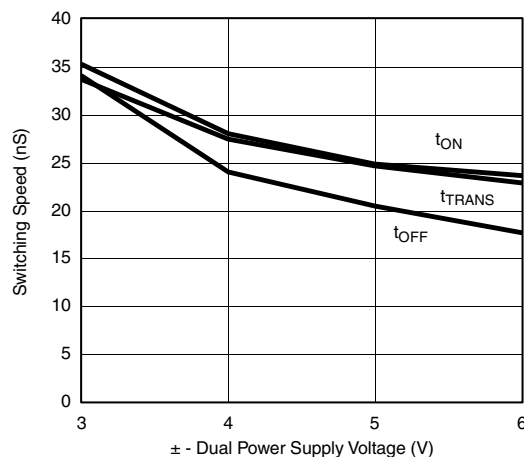
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted) **$R_{DS(on)}$ vs. V_D and Power Supply** **$R_{DS(on)}$ vs. V_D and Power Supply****Input Threshold vs. V_+ Supply Voltage** **$R_{DS(on)}$ vs. V_D and Temperature** **$R_{DS(on)}$ vs. V_D and Temperature****Switching Time vs. Positive Supply Voltage**

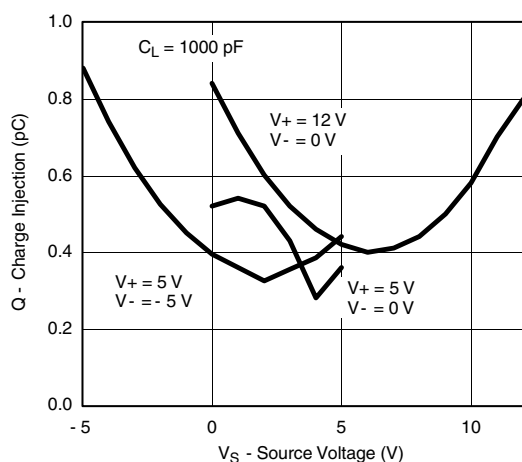
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



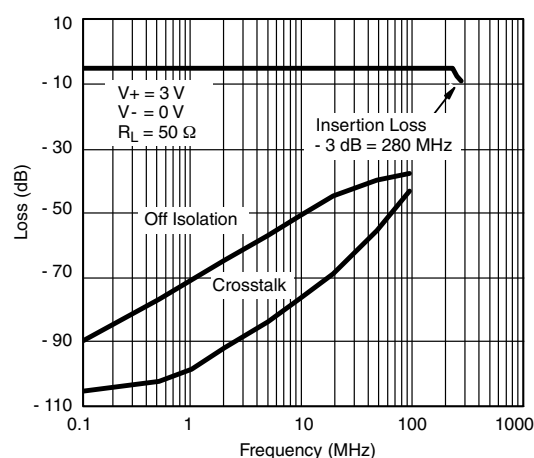
Leakage Current vs. Analog Voltage



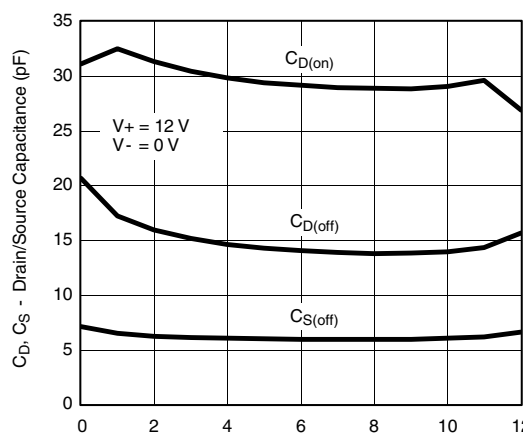
Switching Time vs. Dual Power Supply Voltage



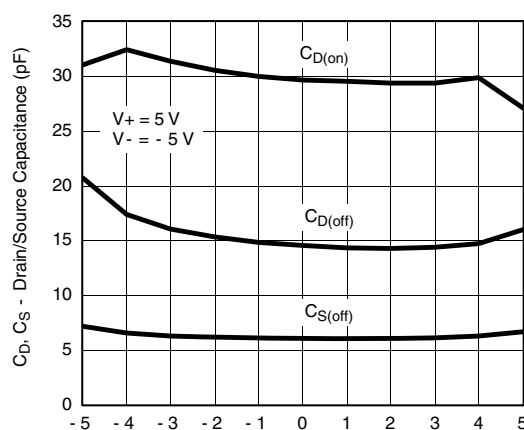
Charge Injection vs. Analog Voltage



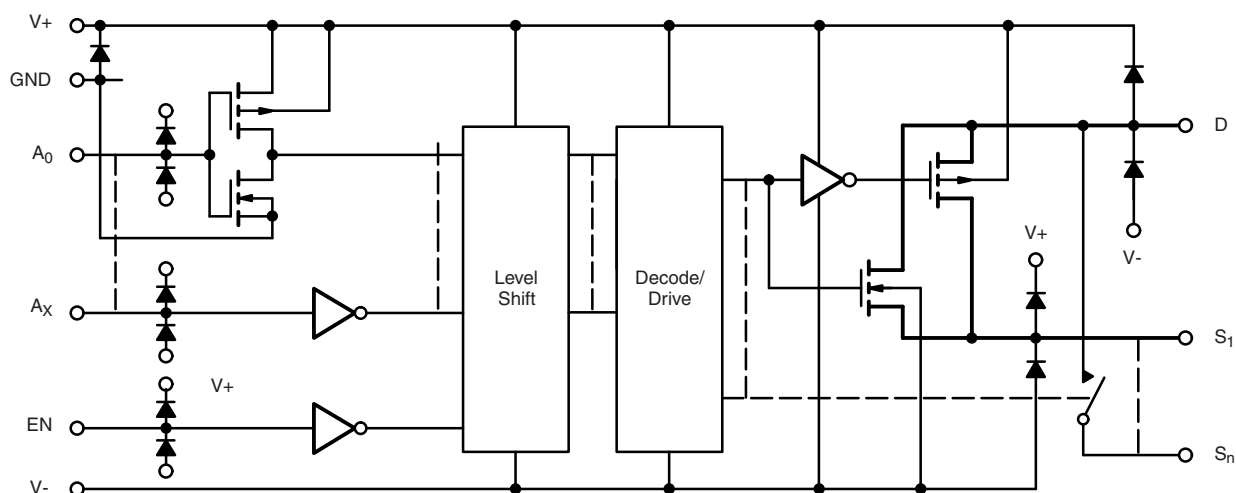
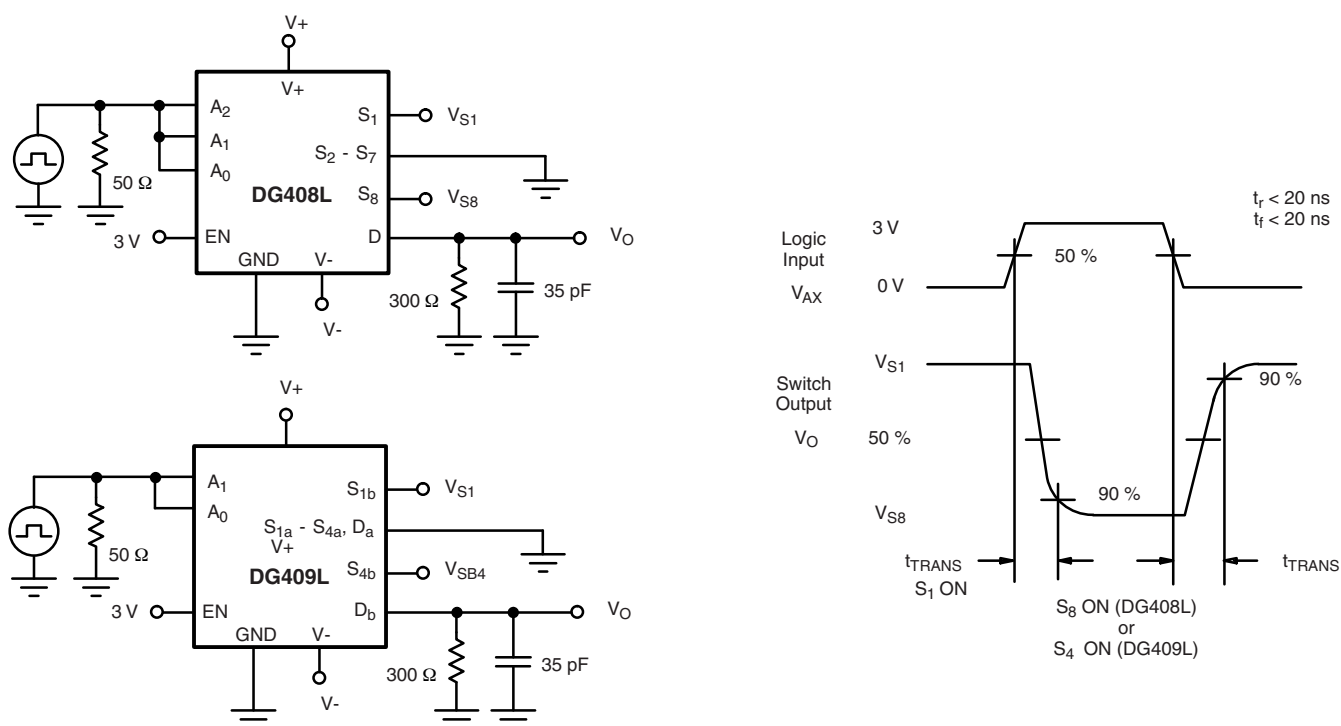
Insertion Loss, Off Isolation and Crosstalk vs. Frequency (Single Supply)



Drain/Source Capacitance vs. Analog Voltage



Drain/Source Capacitance vs. Analog Voltage

SCHEMATIC DIAGRAM (Typical Channel)

Figure 1.
TEST CIRCUITS

Figure 2. Transition Time

TEST CIRCUITS

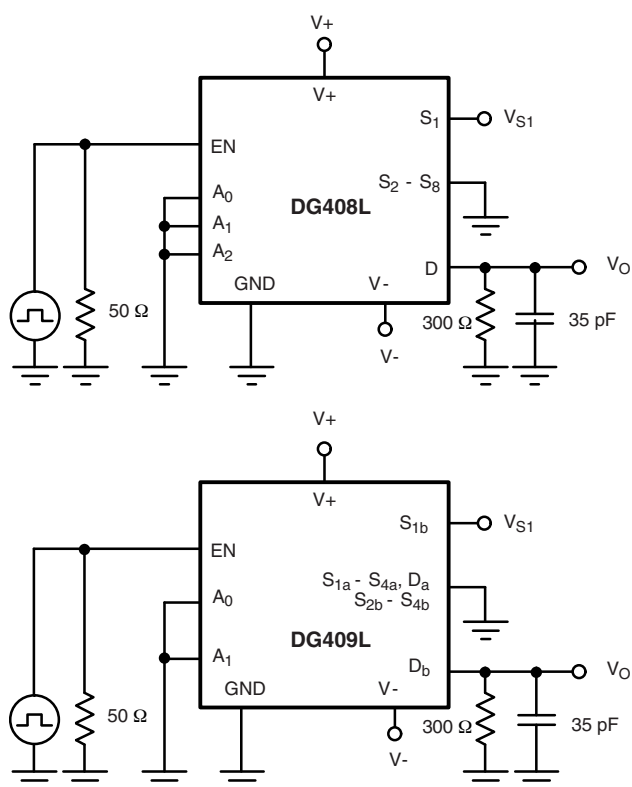


Figure 3. Enable Switching Time

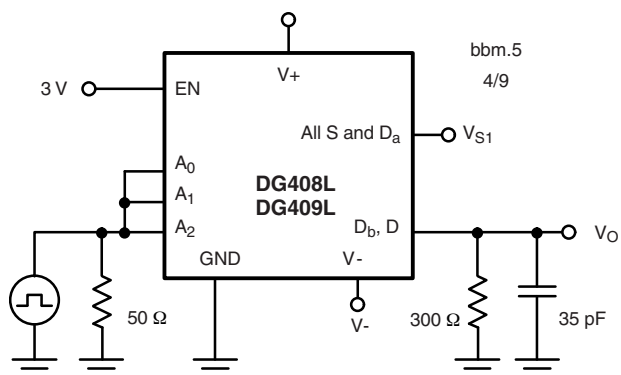
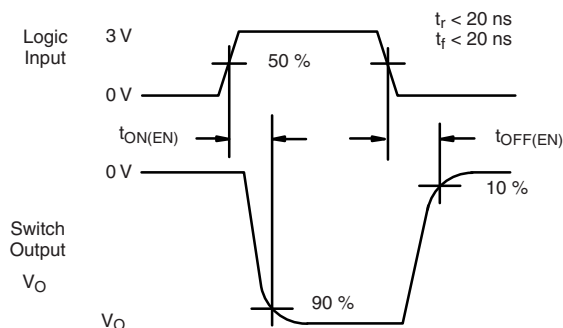
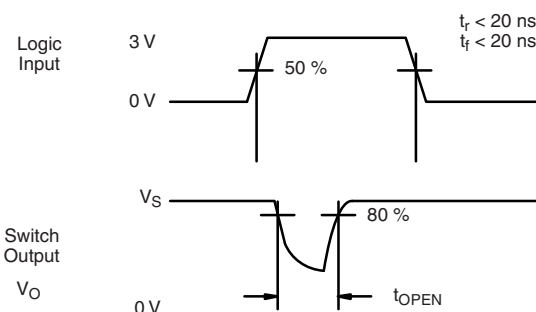
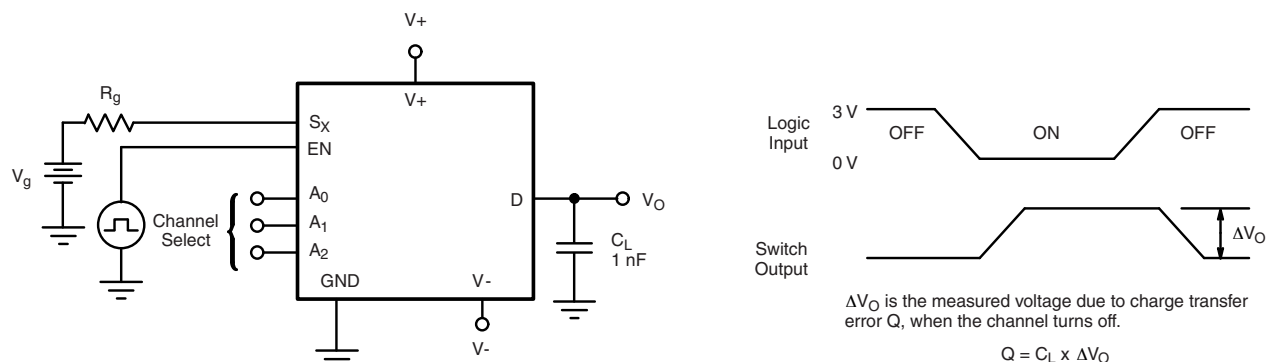
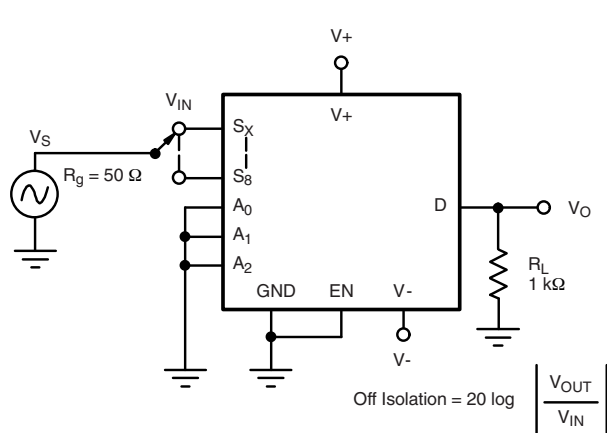
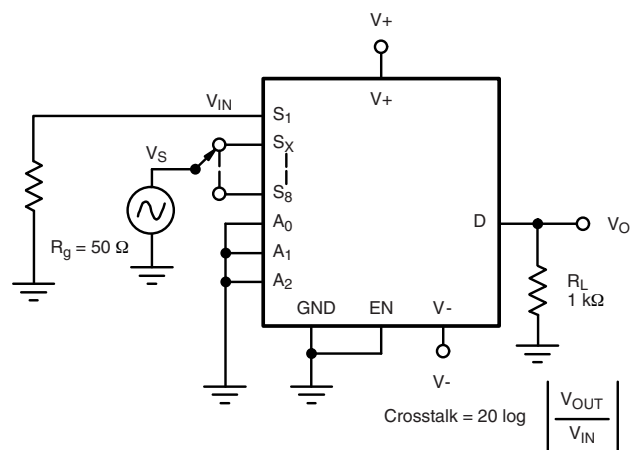
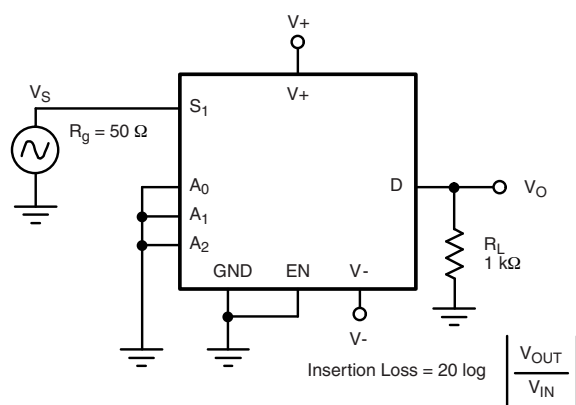
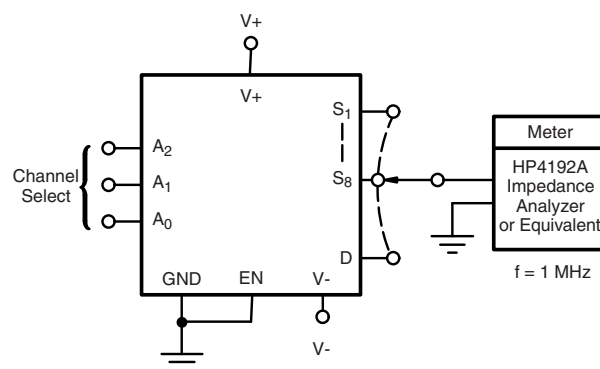


Figure 4. Break-Before-Make Interval



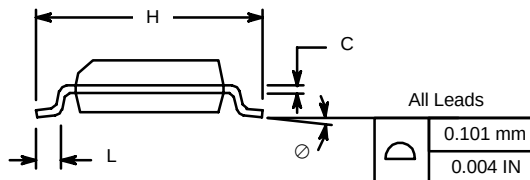
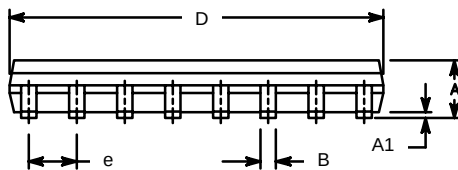
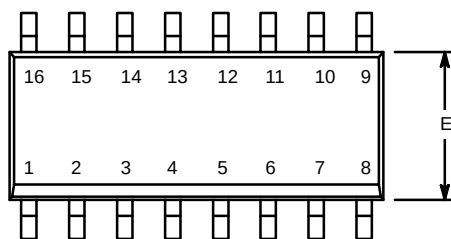
TEST CIRCUITS

Figure 5. Charge Injection

Figure 6. Off Isolation

Figure 7. Crosstalk

Figure 8. Insertion Loss

Figure 9. Source Drain Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg271342.



SOIC (NARROW): 16-LEAD

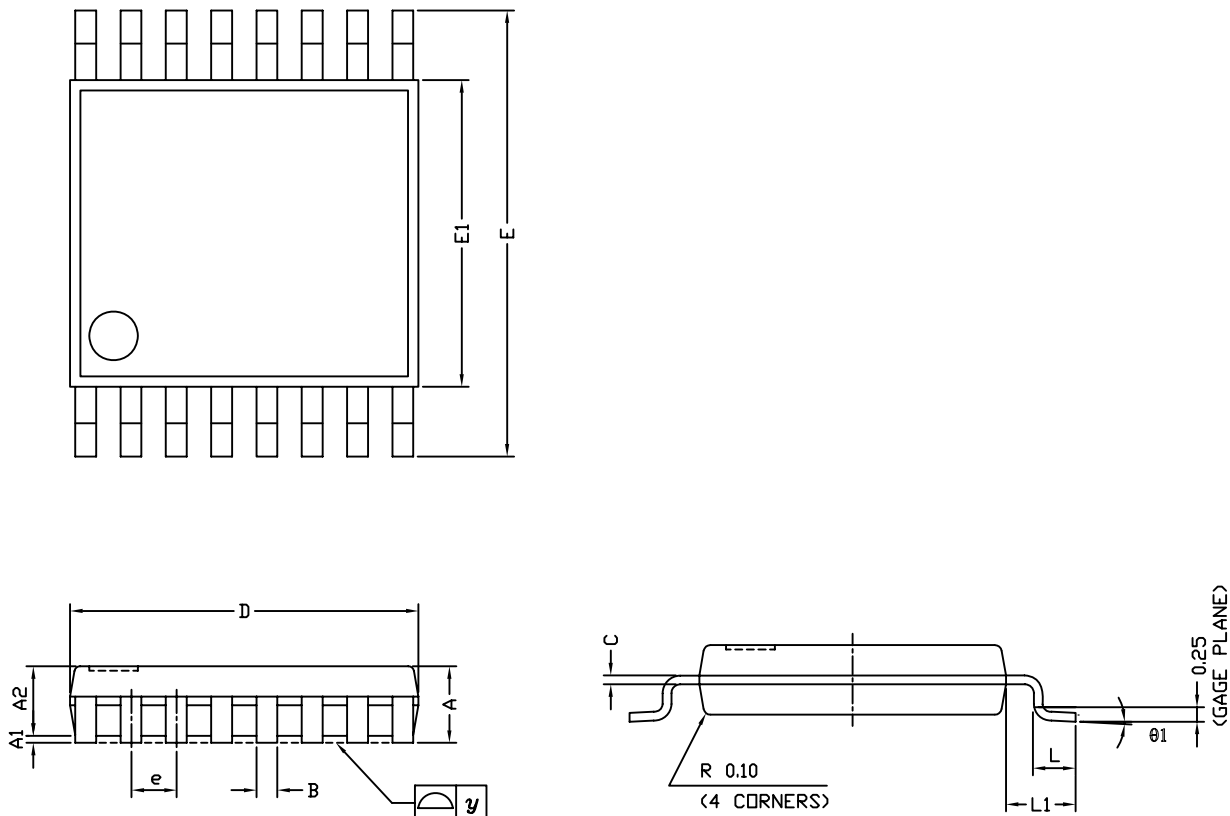
JEDEC Part Number: MS-012



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
Ø	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300

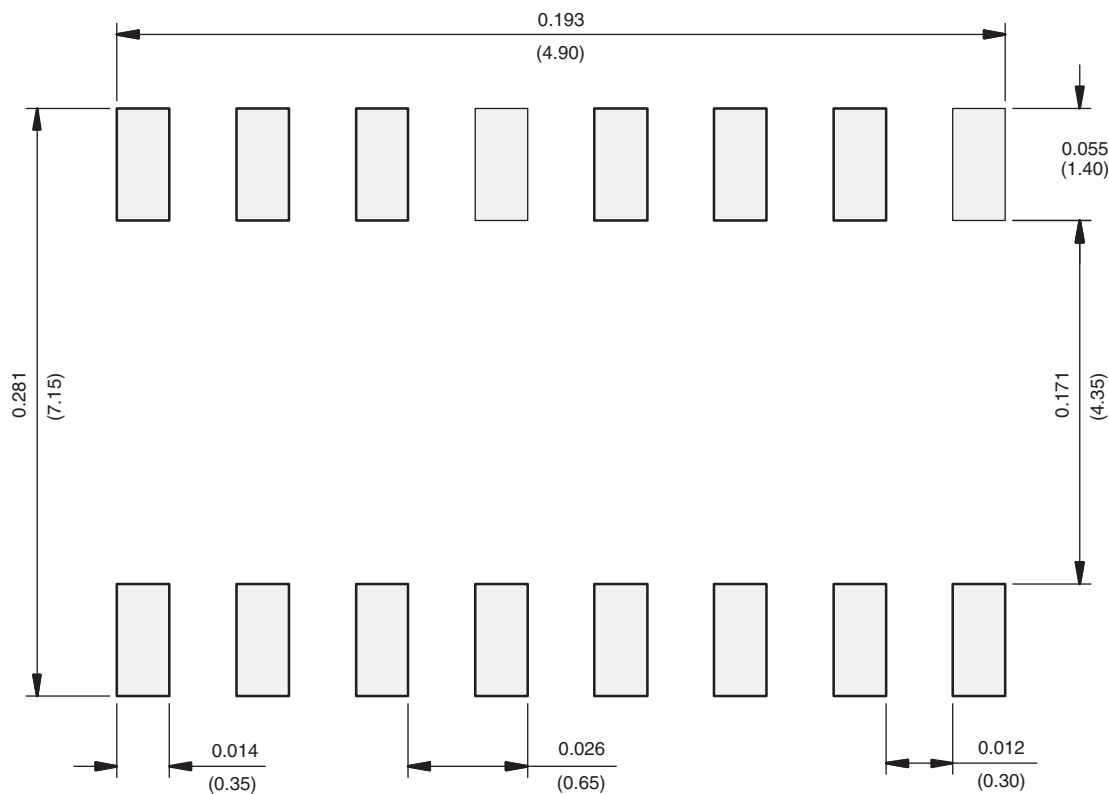
TSSOP: 16-LEAD



Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06			
DWG: 5624			

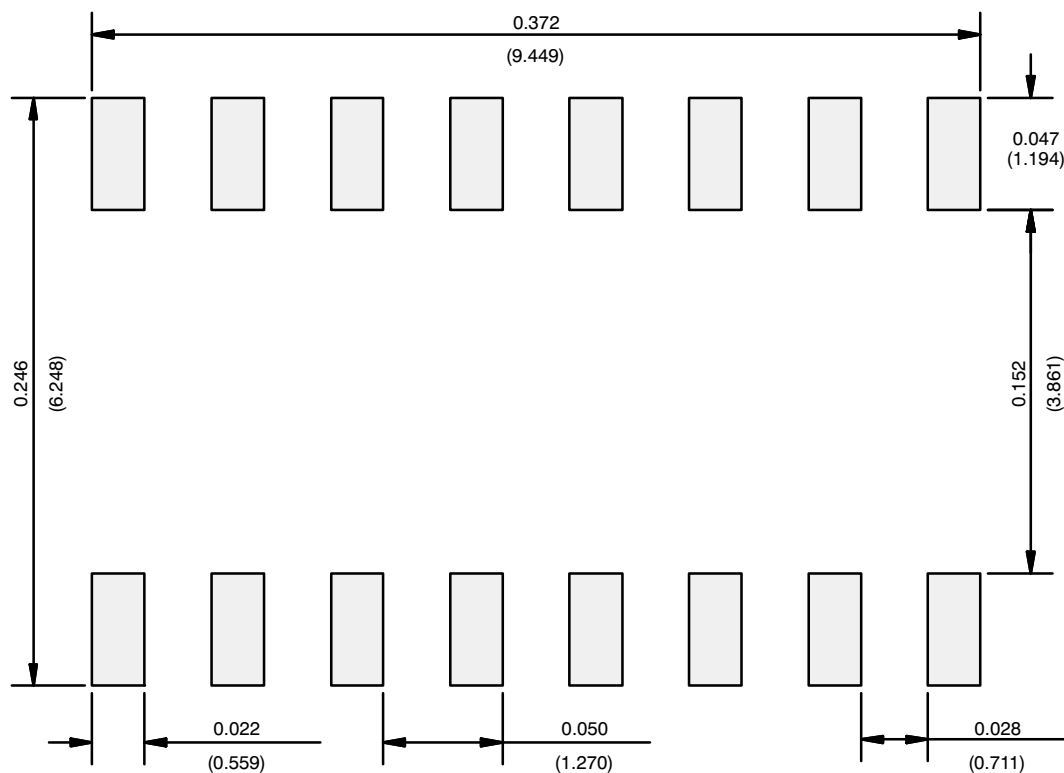


RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and/or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.