

## 74LCX16500

# Low Voltage 18-Bit Universal Bus Transceivers with 5V Tolerant Inputs and Outputs

### General Description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ), latch-enable ( $\overline{LEAB}$  and  $\overline{LEBA}$ ), and clock ( $\overline{CLKAB}$  and  $\overline{CLKBA}$ ) inputs.

The LCX16500 is designed for low voltage (2.5V or 3.3V)  $V_{CC}$  applications with the capability of interfacing to a 5V signal environment.

The LCX16500 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power.

### Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V  $V_{CC}$  specifications provided
- 6.0 ns  $t_{PD}$  max ( $V_{CC} = 3.3V$ ), 20  $\mu A$   $I_{CC}$  max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- $\pm 24$  mA output drive ( $V_{CC} = 3.0V$ )
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

**Note 1:** To ensure the high-impedance state during power up or down,  $\overline{OE}$  should be tied to  $V_{CC}$  and OE tied to GND through a resistor; the minimum value or the resistor is determined by the current-sourcing capability of the driver.

### Ordering Code:

Order Number	Package Number	Package Description
74LCX16500G (Note 2)(Note 3)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LCX16500MEA (Note 3)	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCX16500MTD (Note 3)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

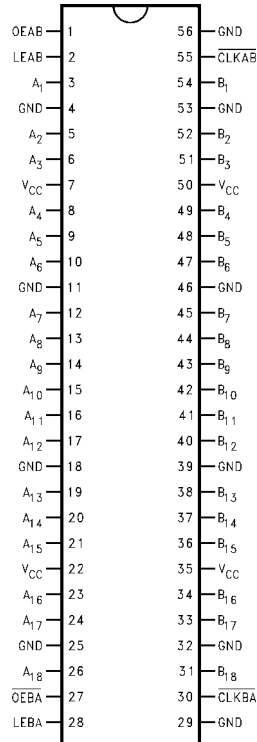
**Note 2:** Ordering code "G" indicates Trays.

**Note 3:** Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

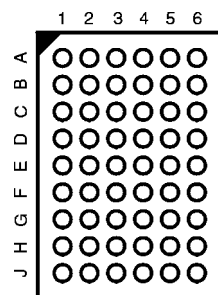
74LCX16500 Low Voltage 18-Bit Universal Bus Transceivers with 5V Tolerant Inputs and Outputs

## Connection Diagrams

### Pin Assignment for SSOP and TSSOP



### Pin Assignment for FBGA



**(Top Thru View)**

## Pin Descriptions

Pin Names	Description
A <sub>1</sub> - A <sub>18</sub>	Data Register A Inputs/3-STATE Outputs
B <sub>1</sub> - B <sub>18</sub>	Data Register B Inputs/3-STATE Outputs
CLKAB, CLKBA	Clock Pulse Inputs
LEAB, LEBA	Latch Enable Inputs
OEBA, $\overline{OEBA}$	Output Enable Inputs

## FBGA Pin Assignments

	1	2	3	4	5	6
A	A <sub>2</sub>	A <sub>1</sub>	OEAB	GND	B <sub>1</sub>	B <sub>2</sub>
B	A <sub>4</sub>	A <sub>3</sub>	LEAB	$\overline{\text{CLKAB}}$	B <sub>3</sub>	B <sub>4</sub>
C	A <sub>6</sub>	A <sub>5</sub>	V <sub>CC</sub>	V <sub>CC</sub>	B <sub>5</sub>	B <sub>6</sub>
D	A <sub>8</sub>	A <sub>7</sub>	GND	GND	B <sub>7</sub>	B <sub>8</sub>
E	A <sub>10</sub>	A <sub>9</sub>	GND	GND	B <sub>9</sub>	B <sub>10</sub>
F	A <sub>12</sub>	A <sub>11</sub>	GND	GND	B <sub>11</sub>	B <sub>12</sub>
G	A <sub>14</sub>	A <sub>13</sub>	V <sub>CC</sub>	V <sub>CC</sub>	B <sub>13</sub>	B <sub>14</sub>
H	A <sub>16</sub>	A <sub>15</sub>	$\overline{\text{OEBA}}$	$\overline{\text{CLKBA}}$	B <sub>15</sub>	B <sub>16</sub>
J	A <sub>17</sub>	A <sub>18</sub>	LEBA	GND	B <sub>18</sub>	B <sub>17</sub>

### Truth Table (Note 4)

Inputs				Output
OEAB	LEAB	CLKAB	A <sub>n</sub>	B <sub>n</sub>
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B <sub>0</sub> (Note 5)
H	L	L	X	B <sub>0</sub> (Note 6)

**Note 4:** A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

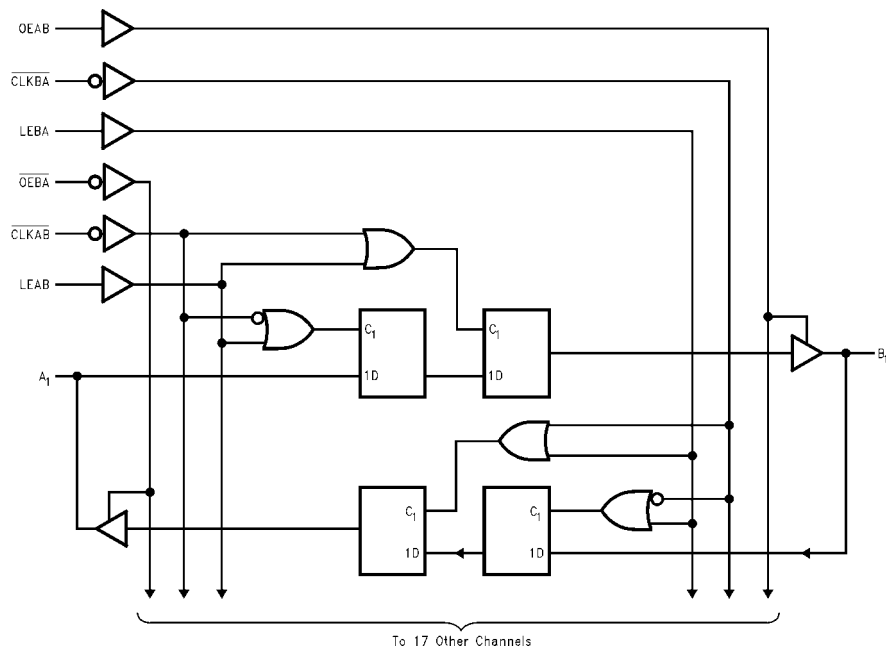
**Note 5:** Output level before the indicated steady-state input conditions were established.

**Note 6:** Output level before the indicated steady-state input conditions were established, provided that  $\overline{\text{CLKAB}}$  was LOW before LEAB went LOW.

## Functional Description

For A-to-B data flow, the LCX16500 operates in the transparent mode when **LEAB** is HIGH. When **LEAB** is LOW, the A data is latched if **CLKAB** is held at a HIGH or LOW logic level. If **LEAB** is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of **CLKAB**. Output-enable **OEAB** is active-HIGH. When **OEAB** is HIGH, the outputs are active. When **OEAB** is LOW, the outputs are in the high impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active HIGH and OEBA is active LOW).

**Logic Diagram**

**Absolute Maximum Ratings**(Note 7)

Symbol	Parameter	Value	Conditions	Units
V <sub>CC</sub>	Supply Voltage	−0.5 to +7.0		V
V <sub>I</sub>	DC Input Voltage	−0.5 to +7.0		V
V <sub>O</sub>	DC Output Voltage	−0.5 to +7.0 −0.5 to V <sub>CC</sub> + 0.5	Output in 3-STATE Output in HIGH or LOW State (Note 8)	V
I <sub>IK</sub>	DC Input Diode Current	−50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	−50 +50	V <sub>O</sub> < GND V <sub>O</sub> > V <sub>CC</sub>	mA
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature	−65 to +150		°C

**Recommended Operating Conditions**

(Note 9)

Symbol	Parameter	Min	Max	Units
V <sub>CC</sub>	Supply Voltage	Operating	2.0	3.6
		Data Retention	1.5	3.6
V <sub>I</sub>	Input Voltage	0	5.5	V
V <sub>O</sub>	Output Voltage	HIGH or LOW State	0	V <sub>CC</sub>
		3-STATE	0	5.5
I <sub>OH</sub> /I <sub>OL</sub>	Output Current	V <sub>CC</sub> = 3.0V – 3.6V		±24
		V <sub>CC</sub> = 2.7V – 3.0V		±12
		V <sub>CC</sub> = 2.3V – 2.7V		±8
T <sub>A</sub>	Free-Air Operating Temperature	−40	85	°C
Δt/ΔV	Input Edge Rate, V <sub>IN</sub> = 0.8V–2.0V, V <sub>CC</sub> = 3.0V	0	10	ns/V

**Note 7:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 8:** I<sub>O</sub> Absolute Maximum Rating must be observed.

**Note 9:** Unused (inputs or I/O's) must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = −40°C to +85°C		Units
				Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V <sub>IL</sub>	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = −100 μA	2.3 – 3.6	V <sub>CC</sub> − 0.2		V
		I <sub>OH</sub> = −8 mA	2.3	1.8		
		I <sub>OH</sub> = −12 mA	2.7	2.2		
		I <sub>OH</sub> = −18 mA	3.0	2.4		
		I <sub>OH</sub> = −24 mA	3.0	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	2.3 – 3.6		0.2	V
		I <sub>OL</sub> = 8 mA	2.3		0.6	
		I <sub>OL</sub> = 12 mA	2.7		0.4	
		I <sub>OL</sub> = 16 mA	3.0		0.4	
		I <sub>OL</sub> = 24 mA	3.0		0.55	
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>I</sub> ≤ 5.5V	2.3 – 3.6		±5.0	μA
I <sub>OZ</sub>	3-STATE I/O Leakage	0 ≤ V <sub>O</sub> ≤ 5.5V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.3 – 3.6		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>I</sub> or V <sub>O</sub> = 5.5V	0		10	μA

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units
				Min	Max	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 – 3.6		20	μA
		3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 5.5V (Note 10)	2.3 – 3.6		±20	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> -0.6V	2.3 – 3.6		500	μA

**Note 10:** Outputs disabled or 3-STATE only.

**AC Electrical Characteristics**

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500 Ω						Units
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		
		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30 pF		
		Min	Max	Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	170						MHz
t <sub>PHL</sub>	Propagation Delay	1.5	6.0	1.5	7.0	1.5	7.2	ns
t <sub>PLH</sub>	Bus to Bus	1.5	6.0	1.5	7.0	1.5	7.2	
t <sub>PHL</sub>	Propagation Delay	1.5	6.7	1.5	8.0	1.5	8.4	ns
t <sub>PLH</sub>	Clock to Bus	1.5	6.7	1.5	8.0	1.5	8.4	
t <sub>PHL</sub>	Propagation Delay	1.5	7.0	1.5	8.0	1.5	8.4	ns
t <sub>PLH</sub>	LE to Bus	1.5	7.0	1.5	8.0	1.5	8.4	
t <sub>PZL</sub>	Output Enable Time	1.5	7.2	1.5	8.2	1.5	9.4	ns
t <sub>PZH</sub>		1.5	7.2	1.5	8.2	1.5	9.4	
t <sub>PLZ</sub>	Output Disable Time	1.5	7.0	1.5	8.0	1.5	8.4	ns
t <sub>PHZ</sub>		1.5	7.0	1.5	8.0	1.5	8.4	
t <sub>S</sub>	Setup Time	2.5		2.5		3.0		ns
t <sub>H</sub>	Hold Time	1.5		1.5		2.0		ns
t <sub>W</sub>	Pulse Width	3.0		3.0		3.5		ns
t <sub>OSSL</sub>	Output to Output Skew		1.0					ns
t <sub>OSLH</sub>	(Note 11)		1.0					

**Note 11:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>), or LOW-to-HIGH (t<sub>OSLH</sub>).

**Dynamic Switching Characteristics**

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units
				Typical	
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	0.8	V
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	2.5	0.6	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	-0.8	V
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	2.5	-0.6	

**Capacitance**

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0V or V <sub>CC</sub>	7	pF
C <sub>IO</sub>	Input/Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz	20	pF

# AC LOADING and WAVEFORMS Generic for LCX Family

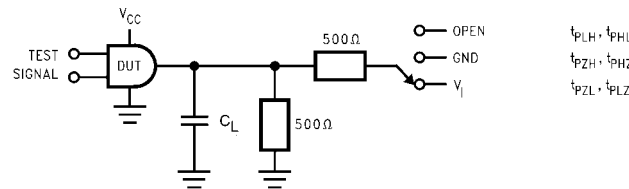
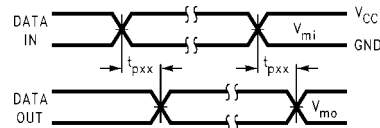
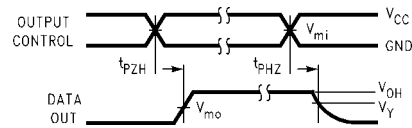


FIGURE 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)

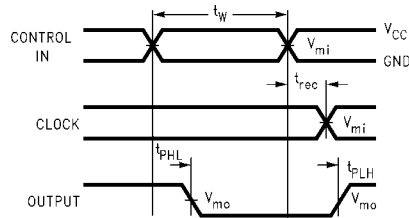
Test	Switch
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ , and 2.7V $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
$t_{PZH}$ , $t_{PHZ}$	GND



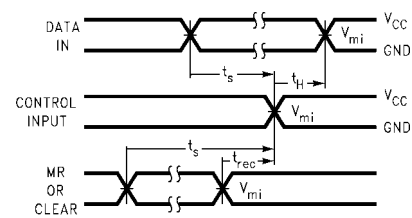
Waveform for Inverting and Non-Inverting Functions



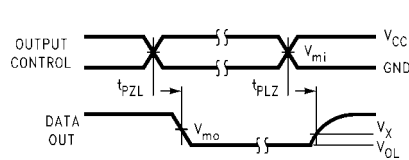
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

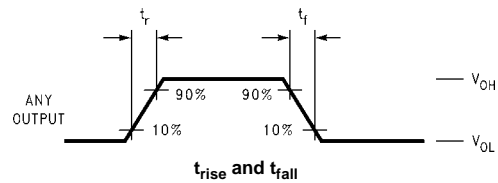
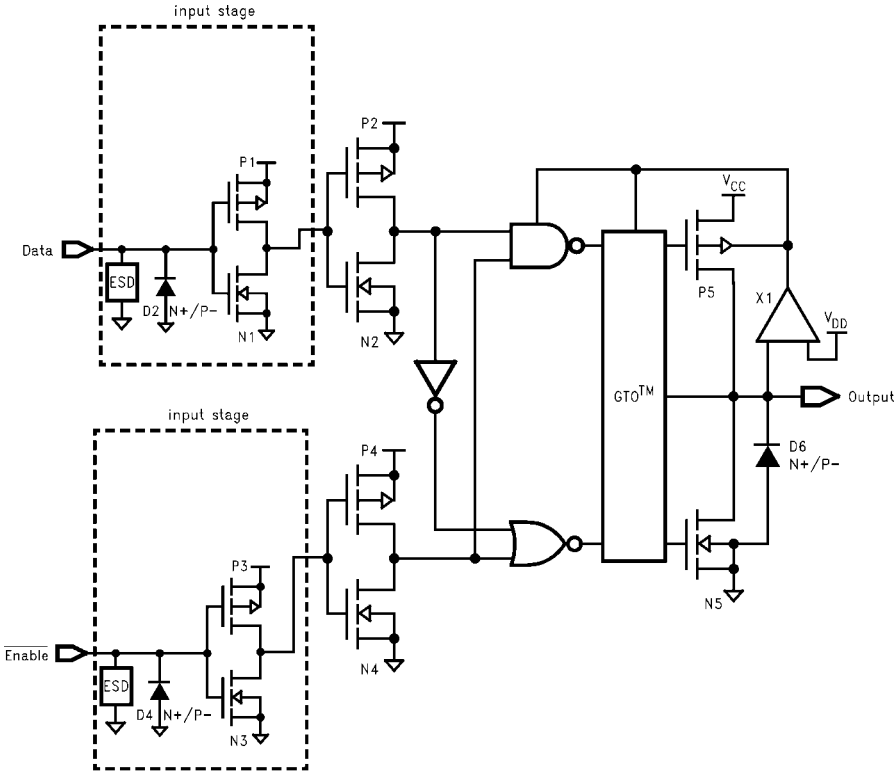


FIGURE 2. Waveforms  
(Input Characteristics;  $f = 1MHz$ ,  $t_r = t_f = 3ns$ )

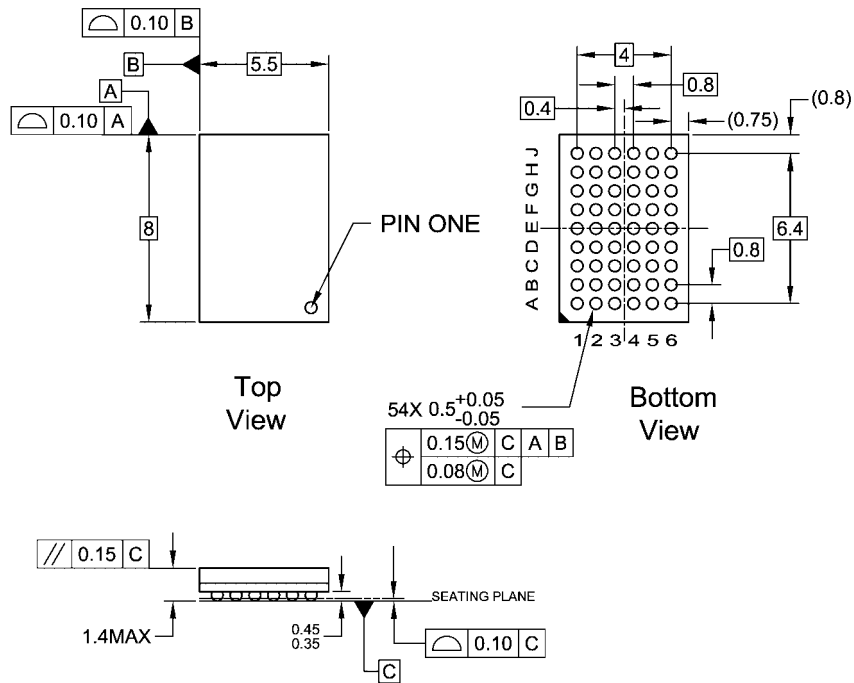
Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	2.7V	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

**Schematic Diagram** Generic for LCX Family



74LCX16500

# Physical Dimensions inches (millimeters) unless otherwise noted



## NOTES:

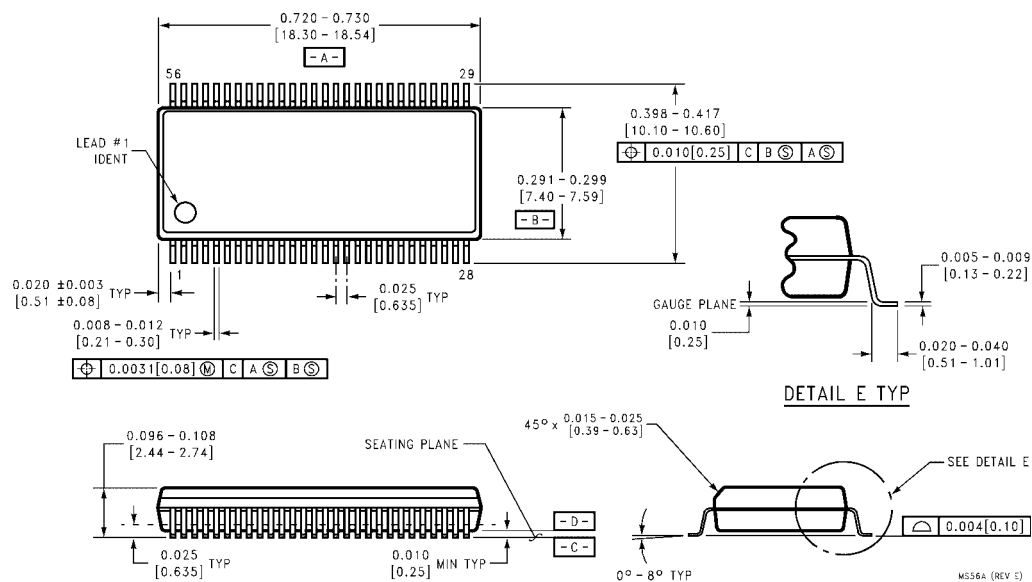
- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide  
Package Number BGA54A**

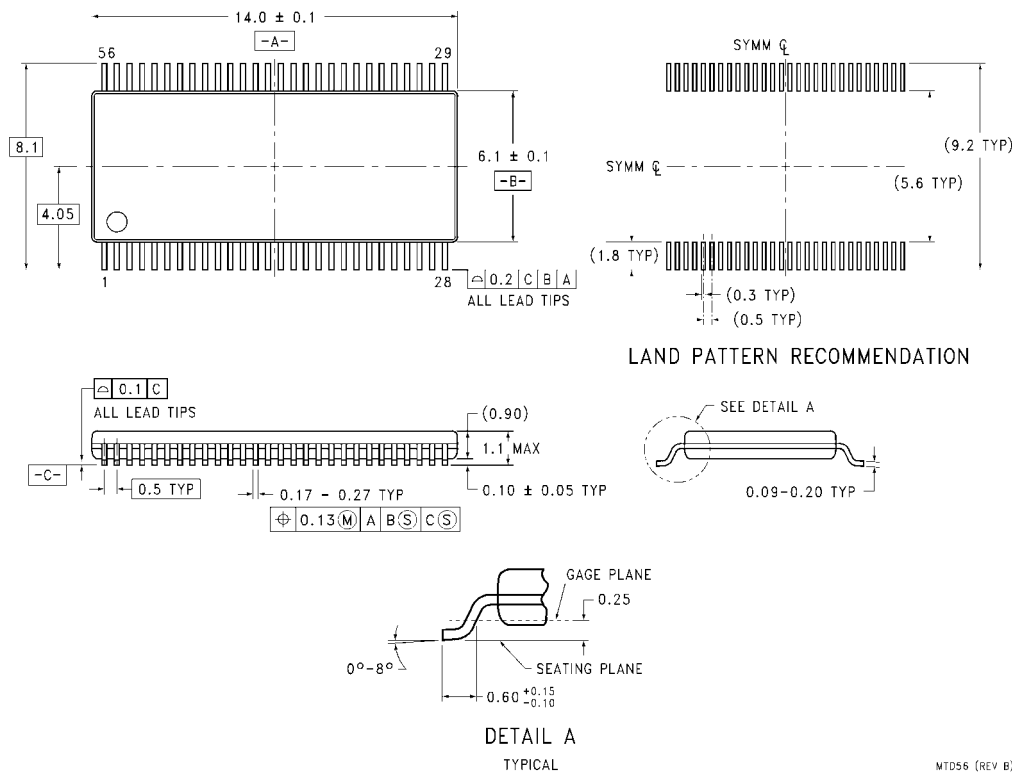


**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS56A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
Package Number MTD56

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)