NCP5810D: Dual 1 W Output AMOLED Driver Supply Evaluation Board

ON Semiconductor®

http://onsemi.com

Prepared by: Hubert Grandry

Overview

The NCP5810D is a dual−output DC/DC converter which can generate both a positive and a negative voltage. The device is optimized for powering modules such as AMOLED display drivers where very good output voltage accuracy and regulation, signal integrity and space is essential for handsets applications.

The output voltage of the inverter is fully configurable using external feedback resistors, where the output voltage of the boost is internally fixed at + 4.6 V.

The intent of the demo boards is to illustrate typical operation of the NCP5810D device for laboratory characterization. The NCP5810DGEVB schematic is depicted.

Operation

The operating power supply of the NCP5810D is from 2.7 V to 4.6 V. The absolute maximum input voltage is 7.0 V. A power supply set to 3.7 V and current limit set to at least 1.5 A must be connected to J1 connector to powering the NCP5810DGEVB/D. Also to compensate for parasitic inductance of wires between the power supply and the evaluation board it is highly recommended to connect a 470 μF electrolytic capacitor to bypass J1 terminal. Like this the device can be evaluate under powering condition very similar that battery power supplies.

Performances of EVB Solution

To be as close as possible with final handset application, the design of this power conversion solution used small size footprints where possible. Changing components may positively or negatively impact the demo board performance illustrate Figures 2 to 4. For example, should one change inductors: a larger one having a lower DCR or/and higher value (in micro Henri) may improve efficiency. Adding the optional Schottky diode D2 provides a lower drop when the current flowing from the inductor to the load, thereby improving the boost converter efficiency. Also placing a jumper across Pins 1−2 of J6 shorts the True−Shut Down function but improved the efficiency. For more information please refer to the NCP5810D datasheet.

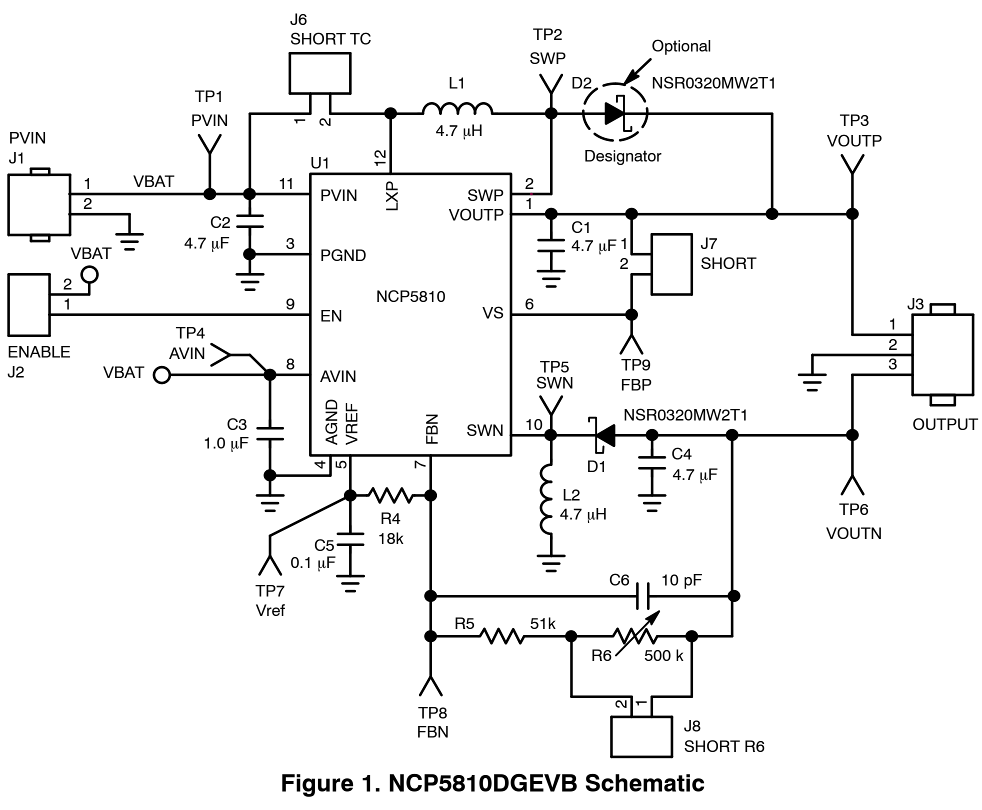

Figure 1. NCP5810DGEVB Schematic

INPUT POWER

Symbol	Descriptions
J1−1	This is the positive connection for power supply. The leads (positive + ground) to the input supply should be twisted and kept as short as possible.
J1−2	This is the return connection for the power supply (Ground signal)
J4, J5	Ground clip

OUTPUT POWER

Symbol	Descriptions
J3−1	This is the positive output connection (VOUTP) of the boost converter.
J3−2	Ground to connect the load.
J3−3	This is the negative output connection (VOUTN) of the inverter.

OUTPUT SETUP

Symbol	Descriptions
R6	This adjustable resistor setup the negative output voltage from –2.0 to –15 V.

SWITCHES SETUP

Symbol	Switch Descriptions
J2	To enable the converter connect a shorting jumper between J2−1 and J2−2
J6	SHORT True SD: Short the True Shutdown function: When a jumper is connected, the internal PMOS used disconnect the load from the battery is bypassed.
J8	A solder dot can be place to short R6 in order to fix VOUTN by R4 and R5 only.

TEST POINT

Symbol	Switch Descriptions
TP1	Test point is directly connected to the PVIN pin to sense the battery voltage.
TP2	This test point is connected to the SWP pin signal.
TP3	This test point is connected to the positive output voltage: VOUTP
TP4	This test point is directly connected to the AVIN pin to sense battery voltage.
TP5	This test point is connected to the SWN pin signal.
TP6	This test point is connected to the negative output voltage: VOUTN
TP7	This test point is connected to the Vref pin signal.
TP8	This test point is connected to the FBN pin signal.
TP9	This test point is connected to the VS pin signal.

TYPICAL OPERATING CHARACTERISTICS

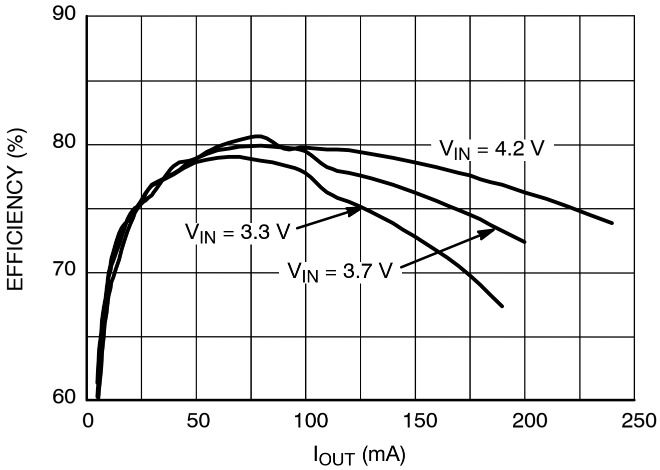

Figure 2. Efficiency vs. I_{OUT} at V_{OUTN} = −5.4 V
L1 = TDK VLF3010 4R7

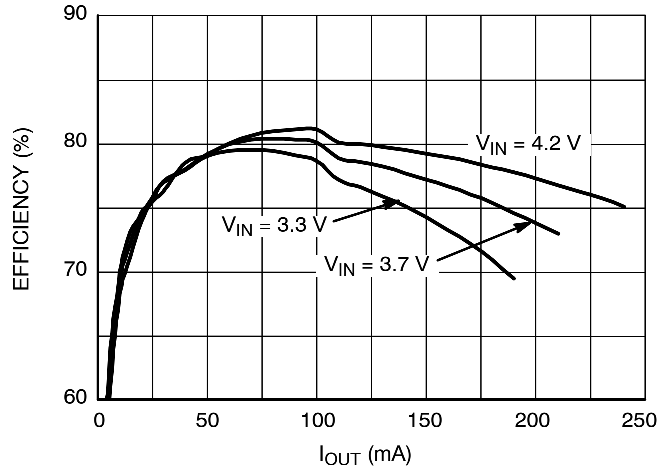

Figure 3. Efficiency vs. I_{OUT} at V_{OUTN} = −5.4 V
L1 = TDK VLF3010 4R7, J2 Short

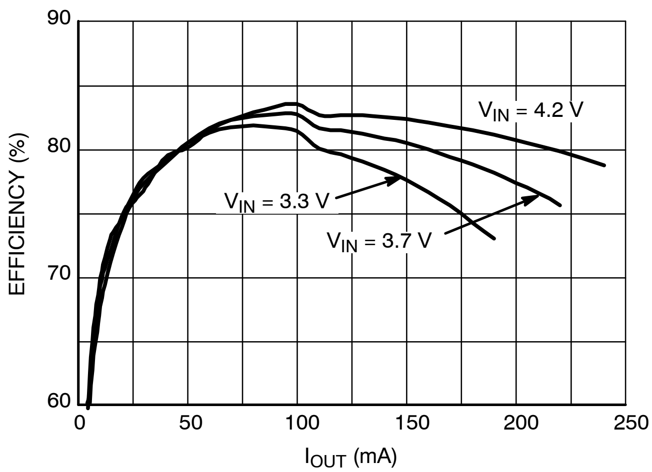

Figure 4. Efficiency vs. I_{OUT} at V_{OUTN} = −5.4 V
L1 = TDK VLF3010 4R7, D2 = NSR0320, J2 Short

PCB Layout

As with all switching DC/DC converter, care must has been observed to place the components on the PCB and layout the critical nodes. Noise−sensitive feedback path such as VS and FBN has been isolated from SWP and SWN nodes how carry high−frequency switching current. Also in order to compensate voltage drop due to the parasitic resistance through output power tracks, feedback pins are sensing directly the corresponding output voltage: TP3 of the boost for VS and TP6 of the inverter for FBN. Finally to provide EMI behavior similar as mass production application, the evaluation board is made of 4 PCB layers where first internal layer is a GND plane at 90 μm from to top. Figures 5, 6 and 7 show the layout of the NCP5810DGEVB board.

For more specific layout guidelines please refer to the NCP5810D datasheet.

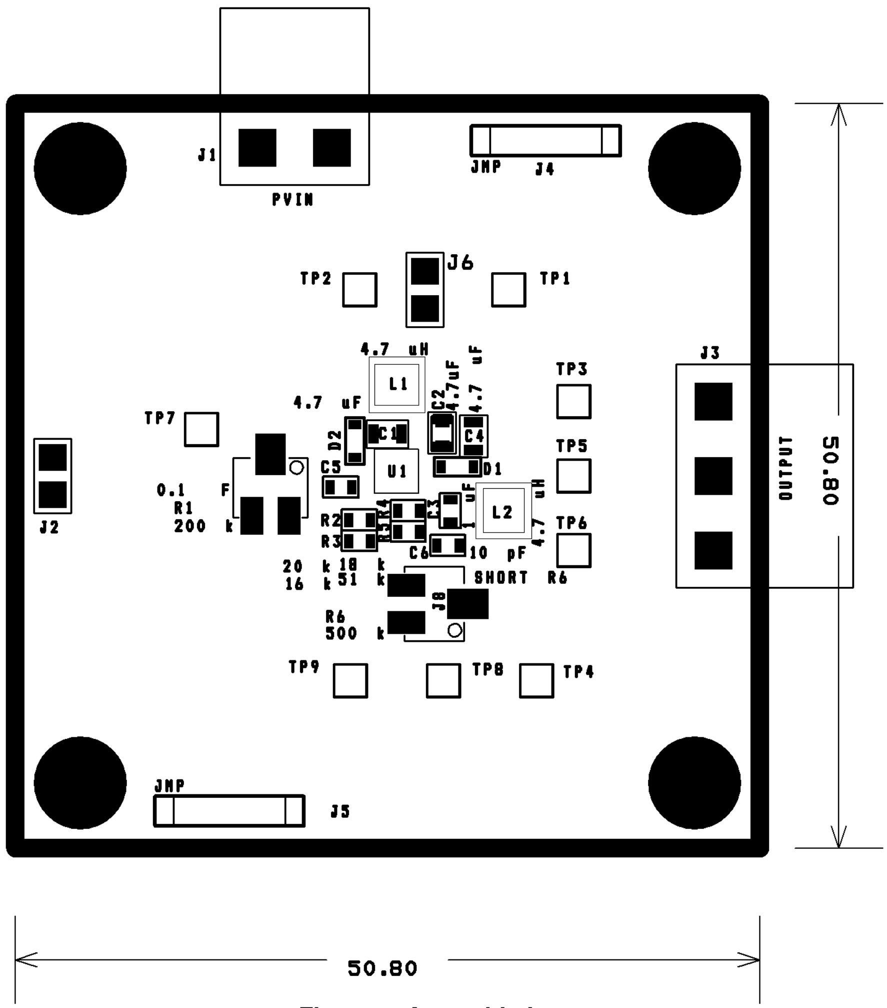

Figure 5. Assembly Layer

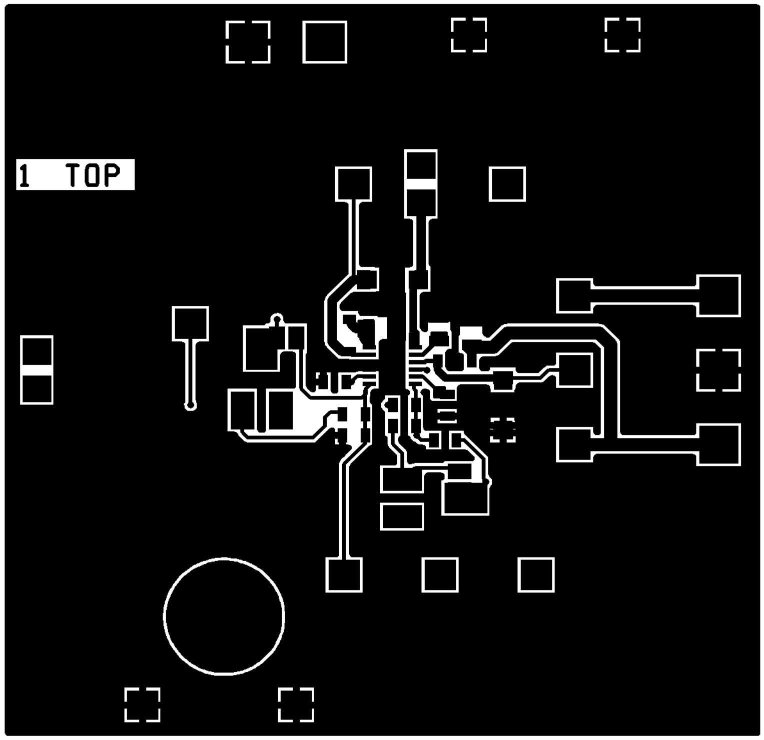

Figure 6. Top Layer Routing

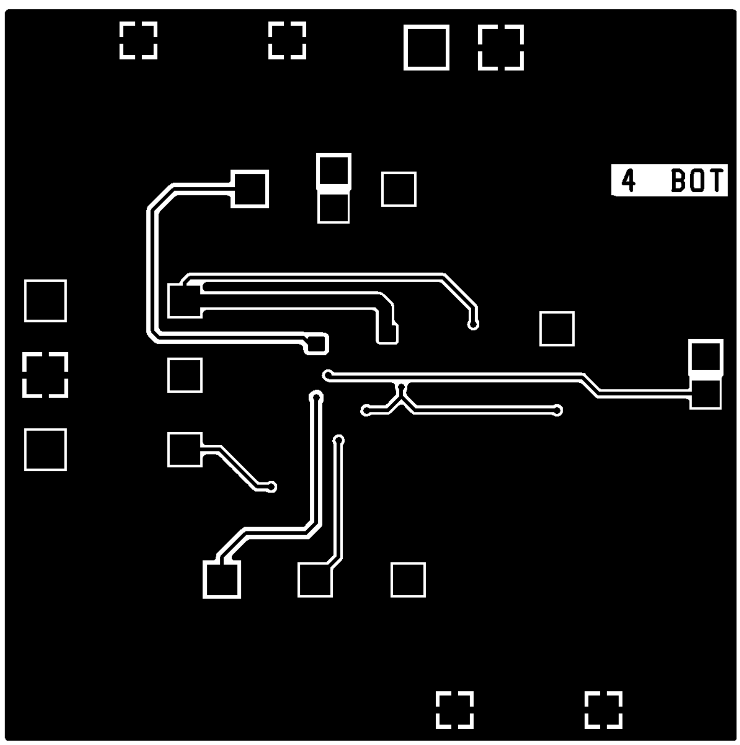

Figure 7. Bottom Layer Routing

BILL OF MATERIALS

Qty	Ref Des.	Description	Size	Manufacturer	Part Number
1	U1	Dual 1 W Output AMOLED Driver Supply	12−Pin UDFN 3 x 3 x 0.55	ON Semiconductor	NCP5810D
3	C1, C4	Capacitor, Ceramic 4.7 μF 10 V	0805	TDK	C2012X5R1A475M
1	C2	Capacitor, Ceramic 4.7 μF 10 V	0603	TDK	C1608X5R1A475M
1	C3	Capacitor, Ceramic 1.0 μF 16 V	0603	TDK	C1608X5R1C105MT
1	C5	Capacitor, Ceramic 0.1 μF 25 V	0603	TDK	C1608X5R1E104M
1	C6	Capacitor, NPO 10 pF 50 V	0603	TDK	C1608COG1H100D
1	D1	Schottky Diode	SOD−323	ON Semiconductor	NSR0320MW2T1G
1	D2	Schottky Diode (Optional)	SOD−323	ON Semiconductor	NSR0320MW2T1G
2	L1, L2	Inductor, SMT, 4.7 μH, 700 mA, 240 mΩ	2.6 x 2.8 x 1.0 mm	TDK	VLF3010AT−4R7MR70
1	R1	NC	–	–	–
1	R2	NC	–	–	–
1	R3	NC	–	–	–
1	R4	Resistor, Chip, 18 kΩ, 1%	0603	Std	Std
1	R5	Resistor, Chip, 51 kΩ, 1%	0603	Std	Std
1	R6	Top Adjust Resistor, 500 kΩ	3.9 x 4.8 x 5.3 mm	BOURNS	3224W−1−504
1	J1	Mal. SL5.08/2/90B plus Fem. BLZ 5.08/2		Weidmuller	SL5.08/2/90 + BLZ 5.08/2
2	J2, J6	Header 2 pin, 100 mil spacing	0.100 x 2	Std	Std
1	J3	Mal. SL5.08/3/90B plus Fem. BLZ 5.08/3		Weidmuller	SL5.08/3/90 + BLZ 5.08/3
2	J4, J5	GND Connection		Std	Std
1	J7	Solder dot to connect VS to VOUTP	–	–	–
9	TP1 to TP9	Test Point		Std	Std
1	PCB	PCB 2.0 in x 2.0 in x 1.0 mm, 4 Layers		Any	TLS−P−003−C−0206−HG

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

ON Semiconductor:

NCP5810DGEVB