

Pentium® Processor Compatible Clock Synthesizer/Driver

Features

- Multiple clock outputs to meet requirements of most Pentium® motherboards
 - Four pin-selectable CPU clocks @ 66.66 MHz, 60.0 MHz, and 50.0 MHz for support of Intel Triton™ PCiset based PC
 - 55.0 MHz pin-selectable CPU clock also available (–2 option only)
 - Six PCI clocks at 1/2 CPU Clock frequency
 - One I/O clock @ 24 MHz
 - One Keyboard Controller clock @ 12 MHz (–1 option) or one Universal Serial Bus clock @ 48 MHz (–2 option)
 - Two Ref. clocks @ 14.318 MHz
 - Ref. 14.318 MHz Xtal oscillator input
- CPU clock jitter ≤ 200 ps cycle-to-cycle
- Low skew outputs
 - ≤ 250 ps between CPU clocks
 - ≤ 250 ps between PCI clocks
 - ≤ 500 ps between CPU and PCI clocks (–2 option)
 - CPU clock leads PCI clock by +1 ns min. to +4 ns max. (–1 option)

- Freq. stability = 0.01% (max.)
- Output duty cycle 45% min. to 55% max.
- Test mode support (–1 option only)
- 3.3V or 5.0V operation
- Internal pull-up resistors on S0, S1, and OE inputs

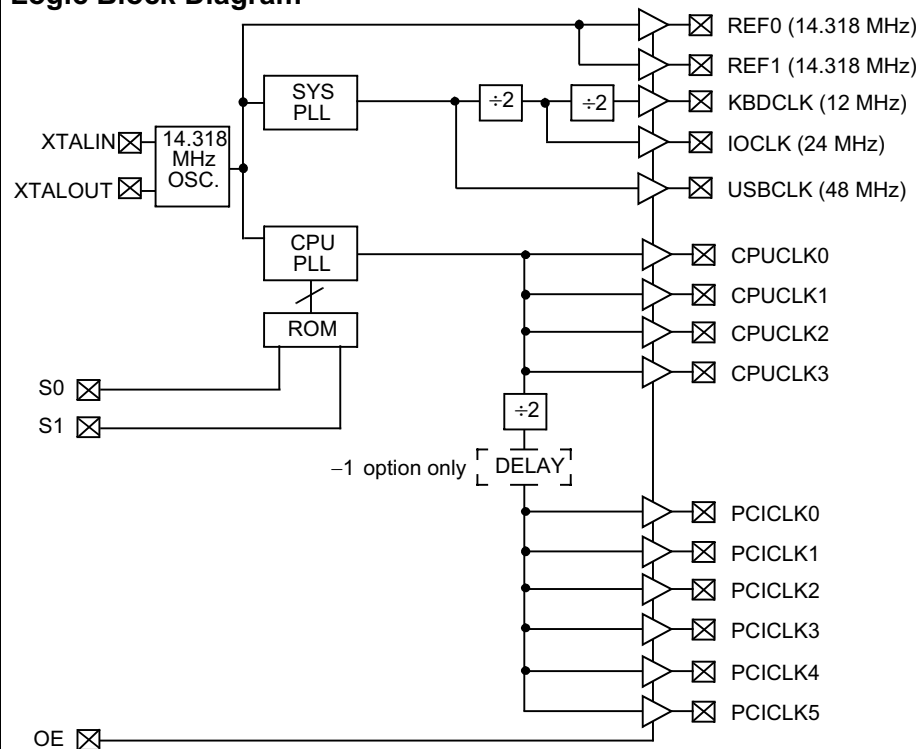
Functional Description

The CY2254A is a Clock Synthesizer/Driver that provides the multiple clocks required for a Pentium-based PC. The CY2254A has low-skew outputs (≤ 250 ps between the CPU Clocks, ≤ 250 ps between the PCI Clocks). In addition, the CY2254A CPU clock outputs have less than 200 ps cycle-to-cycle jitter. Finally, both the PCI and CPU clock outputs meet the 1 V/ns slew rate requirement of a Pentium processor-based system.

The CY2254A accepts a 14.318 MHz reference signal as its input. The CY2254A has 2 PLLs, one of which generates the CPU and PCI clocks, and the other generates the I/O and Keyboard Controller or USB clocks. The CY2254A runs off either a 3.3V or 5V supply.

The CY2254A is available in two options. The –1 option supports the Intel Triton PCiset and provides a 12 MHz keyboard clock on pin 25. The –2 option provides a 48 MHz USB clock on pin 25 and supports the Cyrix® M1 processor.

Logic Block Diagram



Pin Configuration

Top View SOIC

V _{DD}	1	28	REF0
XTALIN	2	27	REF1
XTALOUT	3	26	V _{DD}
V _{SS}	4	25	SEEBELOW
OE	5	24	IOCLK
CPUCLK0	6	23	V _{SS}
CPUCLK1	7	22	PCICLK2
V _{DD}	8	21	PCICLK3
CPUCLK2	9	20	V _{DD}
CPUCLK3	10	19	PCICLK4
V _{SS}	11	18	PCICLK5
S1	12	17	V _{SS}
S0	13	16	PCICLK1
V _{DD}	14	15	PCICLK0

OPTION	PIN 25
–1	KBDCLK 12 MHz
–2	USBCLK 48 MHz

Pin Summary

Name	-1	-2	Description
V _{DD}	1	1	Voltage supply
XTALIN ^[1]	2	2	Reference crystal input
XTALOUT ^[1]	3	3	Reference crystal feedback
V _{SS}	4	4	Ground
OE	5	5	Output Enable, Active HIGH (internal pull-up resistor to V _{DD})
CPUCLK0	6	6	CPU clock output
CPUCLK1	7	7	CPU clock output
V _{DD}	8	8	Voltage supply
CPUCLK2	9	9	CPU clock output
CPUCLK3	10	10	CPU clock output
V _{SS}	11	11	Ground
S1	12	12	CPU clock select input, bit 1 (internal pull-up resistor to V _{DD})
S0	13	13	CPU clock select input, bit 0 (internal pull-up resistor to V _{DD})
V _{DD}	14	14	Voltage supply
PCICLK0	15	15	PCI clock output
PCICLK1	16	16	PCI clock output
V _{SS}	17	17	Ground
PCICLK5	18	18	PCI clock output
PCICLK4	19	19	PCI clock output
V _{DD}	20	20	Voltage supply
PCICLK3	21	21	PCI clock output
PCICLK2	22	22	PCI clock output
V _{SS}	23	23	Ground
IOCLK	24	24	I/O clock output (24 MHz)
KBDCLK	25		Keyboard controller clock output (12 MHz)
USBCLK		25	Universal Serial Bus clock output (48 MHz)
V _{DD}	26	26	Voltage supply
REF1	27	27	Reference clock output (14.318 MHz)
REF0	28	28	Reference clock output (14.318 MHz)

Function Table

Option	OE	S0	S1	XTALIN	CPUCLK	PCICLK	Ref. Clock Output	IOCLK	KBDCLK -1 only	USBCLK -2 only
-1,-2	0	X	X	14.318 MHz	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
-1,-2	1	0	0	14.318 MHz	50.0 MHz	25.0 MHz	14.318 MHz	24 MHz	12 MHz	48 MHz
-1,-2	1	0	1	14.318 MHz	60.0 MHz	30.0 MHz	14.318 MHz	24 MHz	12 MHz	48 MHz
-1,-2	1	1	0	14.318 MHz	66.66 MHz	33.33 MHz	14.318 MHz	24 MHz	12 MHz	48 MHz
-1	1	1	1	TCLK ^[2]	TCLK/2	TCLK/4	TCLK	TCLK/4	TCLK/8	
-2	1	1	1	14.318 MHz	55.0 MHz	27.5 MHz	14.318 MHz	24 MHz		48 MHz

Note:

- For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 17 pF.
- TCLK is a test clock on XTALIN (pin 2) during test mode.

PCI Clock Driver Strength Requirements

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V
- Maximum output impedance: 40Ω measured at 1.5V

CPU Clock Driver Strength Requirements

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V
- Maximum output impedance: 40Ω measured at 1.5V

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage.....	–0.5 to +7.0V
Input Voltage	–0.5V to $V_{DD} + 0.5$
Storage Temperature (Non-Condensing)	–65°C to +150°C
Junction Temperature	+150°C
Package Power Dissipation	1W
Static Discharge Voltage.....	>2000V (per MIL-STD-883, Method 3015)

Operating Conditions^[3]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage 3.3V	3.135	3.6	V
	Supply Voltage 5.0V	4.5	5.5	V
T_A	Operating Ambient Temperature	0	70	°C
C_L	Max. Capacitive Load on CPUCLK PCICLK IOCLK KBDCLK / USBCLK REF0 REF1		20 30 20 20 30 15	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz
t_{PU}	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics $V_{DD} = 3.135V - 3.6V$, or $5.0V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$

Parameter	Description	Test Conditions			Min.	Max.	Unit
V _{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V _{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V _{OH} ^[4]	High-level Output Voltage	V _{DD} = V _{DD} Min.	I _{OH} = 6 mA	CPUCLK	2.4		V
			I _{OH} = 12 mA	PCICLK, REF0			
			I _{OH} = 4 mA	KBDCLK, USBCLK			
			I _{OH} = 8 mA	REF1			
V _{OL} ^[4]	Low-level Output Voltage	V _{DD} = V _{DD} Min.	I _{OL} = 6 mA	CPUCLK		0.4	V
			I _{OL} = 12 mA	PCICLK, REF0			
			I _{OL} = 4 mA	KBDCLK, USBCLK			
			I _{OL} = 8 mA	REF1			
I _{IH}	Input High Current	V _{IH} = V _{DD} , V _{DD} = 3.3V				5	μA
		V _{IH} = V _{DD} , V _{DD} = 5.0V				10	μA
I _{IL}	Input Low Current	V _{IL} = 0 V, V _{DD} = 3.3V				100	μA
		V _{IL} = 0 V, V _{DD} = 5.0V				250	μA
I _{OZ}	Output Leakage Current	Three-state			−10	+10	μA
I _{DD}	Power Supply Current	V _{DD} = 3.6V, V _{IN} = 0 or V _{DD}				90	mA
		V _{DD} = 5.5V, V _{IN} = 0 or V _{DD}				150	mA

Electrical Characteristics $V_{DD} = 3.135V - 3.6V$, or $5.0V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$ (continued)

Parameter	Description	Test Conditions	Min.	Max.	Unit
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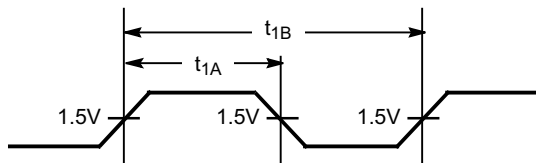
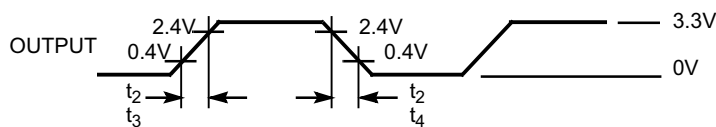
Note:

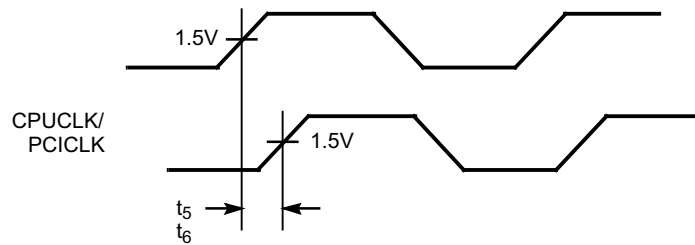
3. Electrical parameters are guaranteed with these operating conditions.

4. Guaranteed by design, not tested.

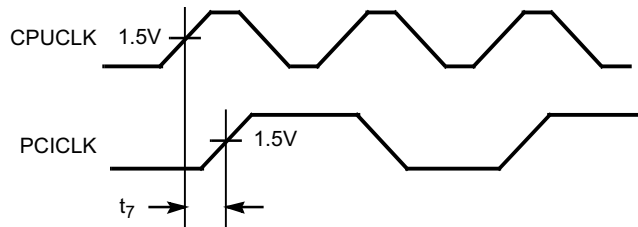
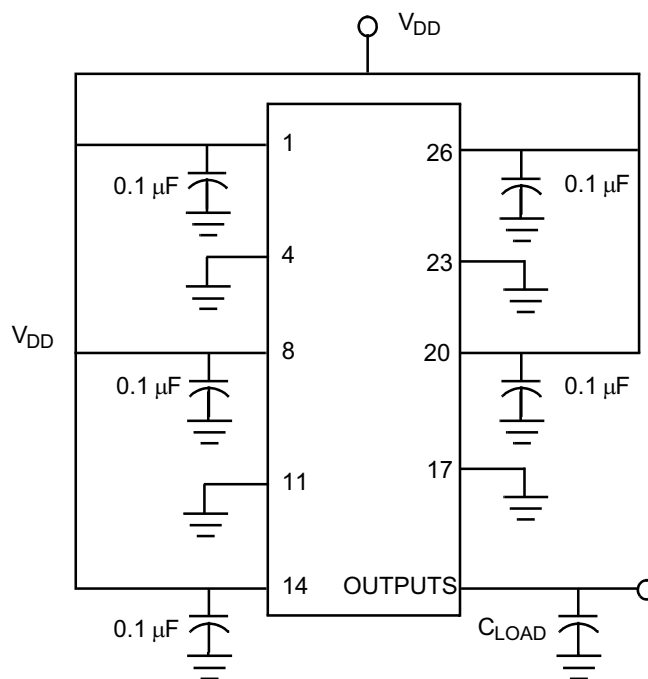
Switching Characteristics^[5]

Parameter	Output	Name	Description	Min.	Max.	Unit
t_1	All	Output Duty Cycle ^[6]	$t_1 = t_{1A} \div t_{1B}$	45%	55%	
$t_2^{[4]}$	CPUCLK, PCICLK	Output Rising and Falling Edge Rate	Measured between 0.4 and 2.4V	1		V/ns
$t_3^{[4]}$	REF, KBDCLK, USBCLK	Rise Time	Measured between 0.4 and 2.4V		4	ns
$t_4^{[4]}$	REF, KBDCLK, USBCLK	Fall Time	Measured between 2.4 and 0.4V		4	ns
$t_5^{[4]}$	CPUCLK	CPU-CPU Clock Skew	Measured at 1.5V		250	ps
$t_6^{[4]}$	PCICLK	PCI-PCI Clock Skew	Measured at 1.5V		250	ps
$t_7^{[4]}$	CPUCLK, PCICLK	CPU-PCI Skew	Measured at 1.5V (–1 option)	1	4	ns
			Measured at 1.5V (–2 option)		500	ps
$t_8^{[4]}$	CPUCLK	Cycle-Cycle Clock Jitter	CPU Clock Jitter		200	ps

Switching Waveforms
Duty Cycle Timing

All Outputs Rise/Fall Time


Switching Waveforms (continued)**Clock Skew****Note:**

5. All parameters specified with outputs fully loaded.
6. Duty cycle is measured at 1.5V.

Switching Waveforms (continued)
CPU-PCI Clock Skew

Test Circuit


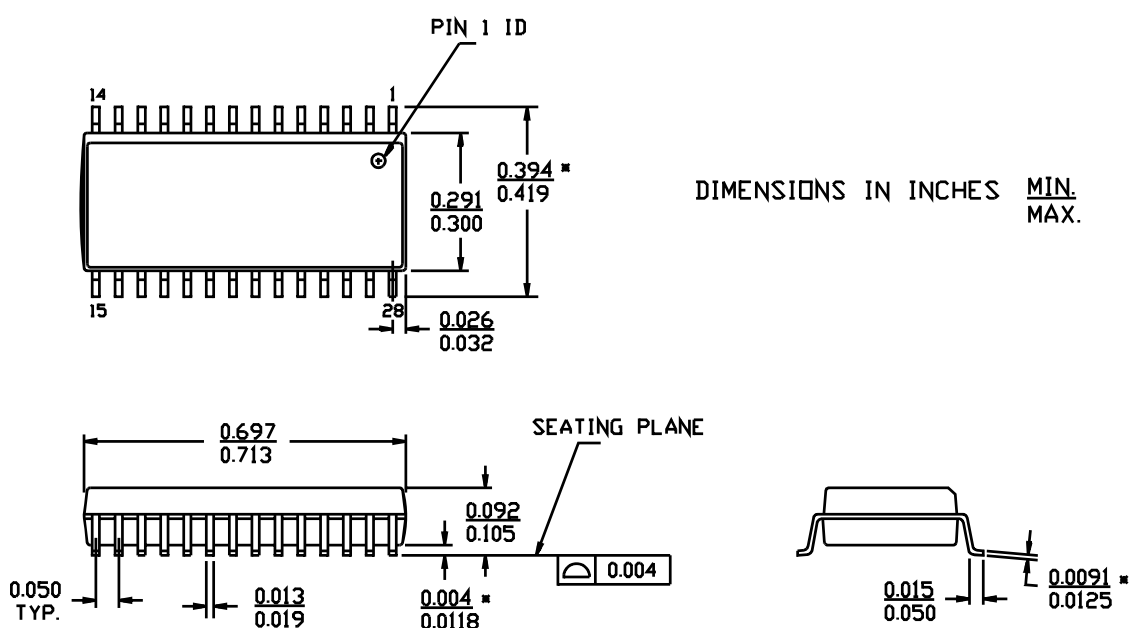
Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2254ASC-1	S21	28-Pin SOIC	Commercial
CY2254ASC-2	S21	28-Pin SOIC	Commercial

Package Drawing and Dimensions

28-Lead (300-Mil) Molded SOIC S21



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