

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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# HM628512C Series

4 M SRAM (512-kword  $\times$  8-bit)



ADE-203-1212C (Z)  
Rev. 3.0  
Aug. 5, 2002

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## Description

The Hitachi HM628512C is a 4-Mbit static RAM organized 512-kword  $\times$  8-bit. It realizes higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. The HM628512C is suitable for battery backup system.

## Features

- Single 5 V supply
- Access time: 55/70 ns (max)
- Power dissipation
  - Active: 10 mW/MHz (typ)
  - Standby: 4  $\mu$ W (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Battery backup operation

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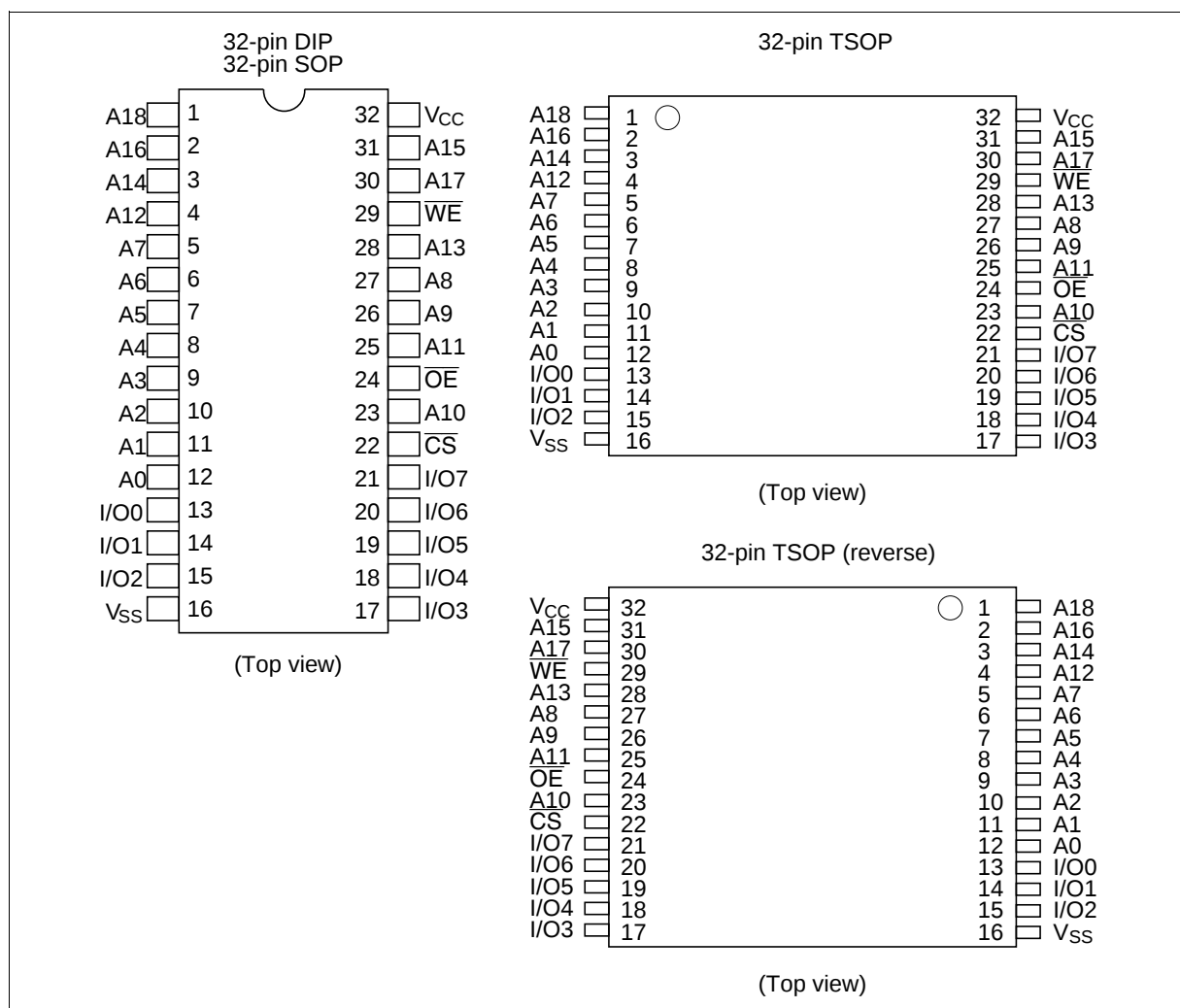
# HM628512C Series

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## Ordering Information

| Type No.         | Access time | Package                                           |
|------------------|-------------|---------------------------------------------------|
| HM628512CLP-7    | 70 ns       | 600-mil 32-pin plastic DIP (DP-32)                |
| HM628512CLP-5SL  | 55 ns       |                                                   |
| HM628512CLFP-7   | 70 ns       | 525-mil 32-pin plastic SOP (FP-32D)               |
| HM628512CLFP-5SL | 55 ns       |                                                   |
| HM628512CLTT-7   | 70 ns       | 400-mil 32-pin plastic TSOP II (TTP-32D)          |
| HM628512CLTT-5SL | 55 ns       |                                                   |
| HM628512CLRR-7   | 70 ns       | 400-mil 32-pin plastic TSOP II reverse (TTP-32DR) |
| HM628512CLRR-5SL | 55 ns       |                                                   |

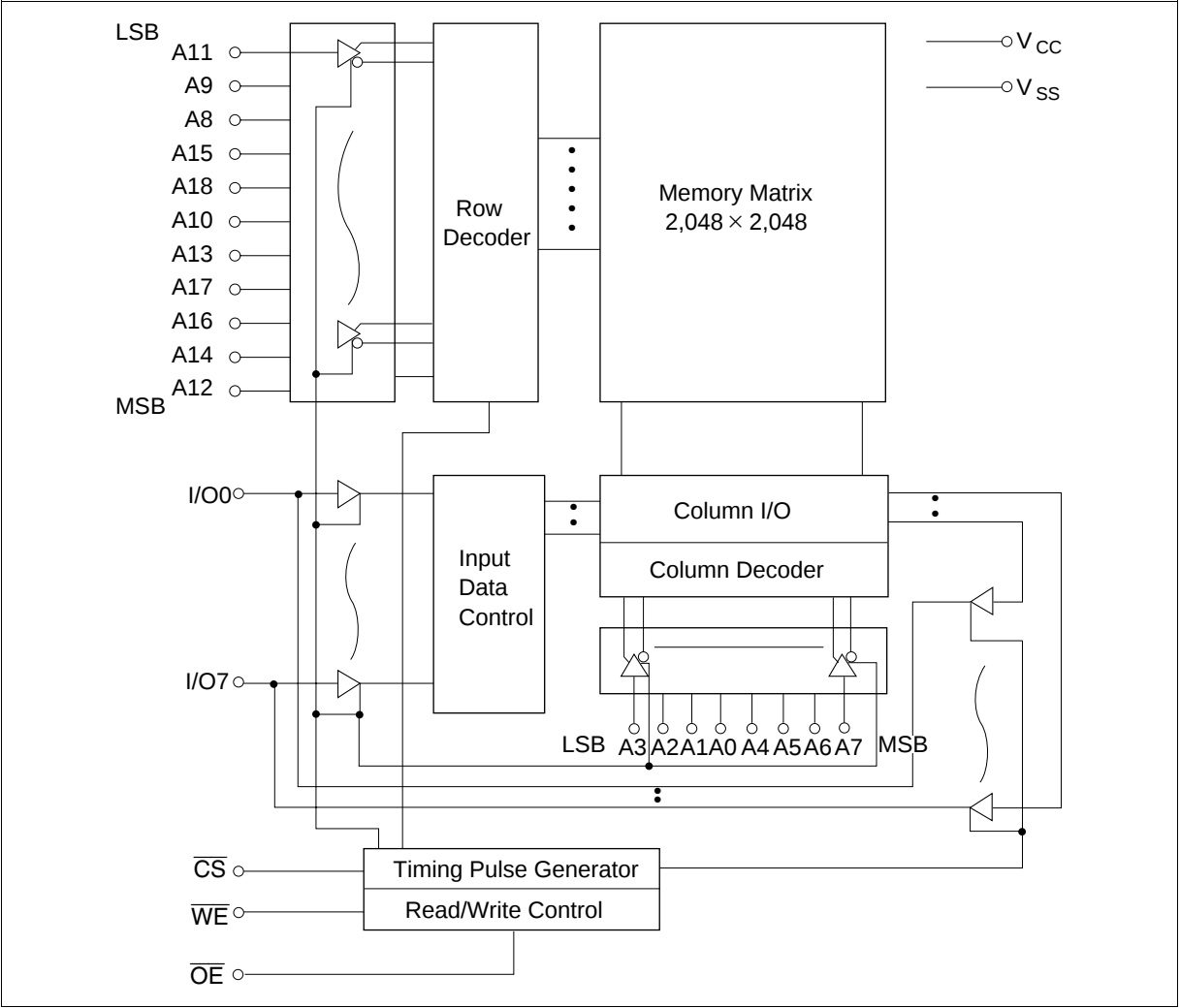
## Pin Arrangement



## Pin Description

| Pin name        | Function          |
|-----------------|-------------------|
| A0 to A18       | Address input     |
| I/O0 to I/O7    | Data input/output |
| CS              | Chip select       |
| OE              | Output enable     |
| WE              | Write enable      |
| V <sub>CC</sub> | Power supply      |
| V <sub>SS</sub> | Ground            |

Block Diagram



## Function Table

| $\overline{WE}$ | $\overline{CS}$ | $\overline{OE}$ | Mode           | $V_{CC}$ current  | Dout pin | Ref. cycle      |
|-----------------|-----------------|-----------------|----------------|-------------------|----------|-----------------|
| X               | H               | X               | Not selected   | $I_{SB}, I_{SB1}$ | High-Z   | —               |
| H               | L               | H               | Output disable | $I_{CC}$          | High-Z   | —               |
| H               | L               | L               | Read           | $I_{CC}$          | Dout     | Read cycle      |
| L               | L               | H               | Write          | $I_{CC}$          | Din      | Write cycle (1) |
| L               | L               | L               | Write          | $I_{CC}$          | Din      | Write cycle (2) |

Note: X: H or L

## Absolute Maximum Ratings

| Parameter                               | Symbol     | Value                                               | Unit |
|-----------------------------------------|------------|-----------------------------------------------------|------|
| Power supply voltage                    | $V_{CC}$   | −0.5 to +7.0                                        | V    |
| Voltage on any pin relative to $V_{SS}$ | $V_T$      | −0.5* <sup>1</sup> to $V_{CC} + 0.3$ * <sup>2</sup> | V    |
| Power dissipation                       | $P_T$      | 1.0                                                 | W    |
| Operating temperature                   | $T_{opr}$  | −20 to +70                                          | °C   |
| Storage temperature                     | $T_{stg}$  | −55 to +125                                         | °C   |
| Storage temperature under bias          | $T_{bias}$ | −20 to +85                                          | °C   |

Notes: 1.  $V_T$  min: −3.0 V for pulse half-width ≤ 30 ns.

2. Maximum voltage is 7.0 V.

## Recommended DC Operating Conditions ( $T_a = -20$ to $+70^\circ\text{C}$ )

| Parameter          | Symbol   | Min                | Typ | Max            | Unit |
|--------------------|----------|--------------------|-----|----------------|------|
| Supply voltage     | $V_{CC}$ | 4.5                | 5.0 | 5.5            | V    |
|                    | $V_{SS}$ | 0                  | 0   | 0              | V    |
| Input high voltage | $V_{IH}$ | 2.2                | —   | $V_{CC} + 0.3$ | V    |
| Input low voltage  | $V_{IL}$ | −0.3* <sup>1</sup> | —   | 0.8            | V    |

Note: 1.  $V_{IL}$  min: −3.0 V for pulse half-width ≤ 30 ns.

## DC Characteristics

| Parameter                            | Symbol                | Min | Typ* <sup>1</sup> | Max              | Unit          | Test conditions                                                                                                                                    |
|--------------------------------------|-----------------------|-----|-------------------|------------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| Input leakage current                | $I_{LI}$              | —   | —                 | 1                | $\mu\text{A}$ | $V_{in} = V_{SS}$ to $V_{CC}$                                                                                                                      |
| Output leakage current               | $I_{LO}$              | —   | —                 | 1                | $\mu\text{A}$ | $\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , $V_{I/O} = V_{SS}$ to $V_{CC}$                                  |
| Operating power supply current: DC   | $I_{CC}$              | —   | 1.5               | 3                | mA            | $\overline{CS} = V_{IL}$ ,<br>others = $V_{IH}/V_{IL}$ , $I_{I/O} = 0$ mA                                                                          |
| Operating power supply current       | HM628512C-5 $I_{CC1}$ | —   | 8                 | 25               | mA            | Min cycle, duty = 100%<br>$\overline{CS} = V_{IL}$ , others = $V_{IH}/V_{IL}$<br>$I_{I/O} = 0$ mA                                                  |
|                                      | HM628512C-7 $I_{CC1}$ | —   | 7                 | 25               | mA            |                                                                                                                                                    |
| Operating power supply current       | $I_{CC2}$             | —   | 2                 | 5                | mA            | Cycle time = 1 $\mu\text{s}$ ,<br>duty = 100%<br>$I_{I/O} = 0$ mA, $\overline{CS} \leq 0.2$ V<br>$V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V |
| Standby power supply current: DC     | $I_{SB}$              | —   | 0.1               | 0.5              | mA            | $\overline{CS} = V_{IH}$                                                                                                                           |
| Standby power supply current (1): DC | $I_{SB1}$             | —   | 0.8* <sup>2</sup> | 20* <sup>2</sup> | $\mu\text{A}$ | $V_{in} \geq 0$ V, $\overline{CS} \geq V_{CC} - 0.2$ V                                                                                             |
|                                      |                       | —   | 0.8* <sup>3</sup> | 10* <sup>3</sup> | $\mu\text{A}$ |                                                                                                                                                    |
| Output low voltage                   | $V_{OL}$              | —   | —                 | 0.4              | V             | $I_{OL} = 2.1$ mA                                                                                                                                  |
| Output high voltage                  | $V_{OH}$              | 2.4 | —                 | —                | V             | $I_{OH} = -1.0$ mA                                                                                                                                 |

Notes: 1. Typical values are at  $V_{CC} = 5.0$  V,  $T_a = +25^\circ\text{C}$  and specified loading, and not guaranteed.

2. This characteristics is guaranteed only for L version.

3. This characteristics is guaranteed only for L-SL version.

## Capacitance ( $T_a = +25^\circ\text{C}$ , $f = 1$ MHz)

| Parameter                              | Symbol    | Typ | Max              | Unit | Test conditions |
|----------------------------------------|-----------|-----|------------------|------|-----------------|
| Input capacitance* <sup>1</sup>        | $C_{in}$  | —   | 8                | pF   | $V_{in} = 0$ V  |
| Input/output capacitance* <sup>1</sup> | $C_{I/O}$ | —   | 10* <sup>2</sup> | pF   | $V_{I/O} = 0$ V |

Notes: 1. This parameter is sampled and not 100% tested.

2.  $C_{I/O}$  max = 12 pF only for HM628512CLP Series.

**AC Characteristics** ( $T_a = -20$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ , unless otherwise noted.)

**Test Conditions**

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate +  $C_L$  (100 pF) (HM628512C-7)  
1 TTL Gate +  $C_L$  (50 pF) (HM628512C-5)  
(Including scope & jig)

**Read Cycle**

|                                      |                  | HM628512C |     |     |     |      |       |
|--------------------------------------|------------------|-----------|-----|-----|-----|------|-------|
|                                      |                  | -5        |     | -7  |     |      |       |
| Parameter                            | Symbol           | Min       | Max | Min | Max | Unit | Notes |
| Read cycle time                      | t <sub>RC</sub>  | 55        | —   | 70  | —   | ns   |       |
| Address access time                  | t <sub>AA</sub>  | —         | 55  | —   | 70  | ns   |       |
| Chip select access time              | t <sub>CO</sub>  | —         | 55  | —   | 70  | ns   |       |
| Output enable to output valid        | t <sub>OE</sub>  | —         | 25  | —   | 35  | ns   |       |
| Chip selection to output in low-Z    | t <sub>LZ</sub>  | 10        | —   | 10  | —   | ns   | 2     |
| Output enable to output in low-Z     | t <sub>OLZ</sub> | 5         | —   | 5   | —   | ns   | 2     |
| Chip deselection to output in high-Z | t <sub>HZ</sub>  | 0         | 20  | 0   | 25  | ns   | 1, 2  |
| Output disable to output in high-Z   | t <sub>OHZ</sub> | 0         | 20  | 0   | 25  | ns   | 1, 2  |
| Output hold from address change      | t <sub>OH</sub>  | 10        | —   | 10  | —   | ns   |       |

## Write Cycle

|                                     |                  | HM628512C |     |     |     |      |         |
|-------------------------------------|------------------|-----------|-----|-----|-----|------|---------|
|                                     |                  | -5        |     | -7  |     |      |         |
| Parameter                           | Symbol           | Min       | Max | Min | Max | Unit | Notes   |
| Write cycle time                    | t <sub>WC</sub>  | 55        | —   | 70  | —   | ns   |         |
| Chip selection to end of write      | t <sub>CW</sub>  | 50        | —   | 60  | —   | ns   | 4       |
| Address setup time                  | t <sub>AS</sub>  | 0         | —   | 0   | —   | ns   | 5       |
| Address valid to end of write       | t <sub>AW</sub>  | 50        | —   | 60  | —   | ns   |         |
| Write pulse width                   | t <sub>WP</sub>  | 40        | —   | 50  | —   | ns   | 3, 12   |
| Write recovery time                 | t <sub>WR</sub>  | 0         | —   | 0   | —   | ns   | 6       |
| $\overline{WE}$ to output in high-Z | t <sub>WHZ</sub> | 0         | 20  | 0   | 25  | ns   | 1, 2, 7 |
| Data to write time overlap          | t <sub>DW</sub>  | 25        | —   | 30  | —   | ns   |         |
| Data hold from write time           | t <sub>DH</sub>  | 0         | —   | 0   | —   | ns   |         |
| Output active from output in high-Z | t <sub>OW</sub>  | 5         | —   | 5   | —   | ns   | 2       |
| Output disable to output in high-Z  | t <sub>OHZ</sub> | 0         | 20  | 0   | 25  | ns   | 1, 2, 7 |

Notes: 1.  $t_{HZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the later transition of  $\overline{CS}$  going low or  $\overline{WE}$  going low. A write ends at the earlier transition of  $\overline{CS}$  going high or  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.

4.  $t_{CW}$  is measured from  $\overline{CS}$  going low to the end of write.

5.  $t_{AS}$  is measured from the address valid to the beginning of write.

6.  $t_{WR}$  is measured from the earlier of  $\overline{WE}$  or  $\overline{CS}$  going high to the end of write cycle.

7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.

8. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, the output remain in a high impedance state.

9. Dout is the same phase of the write data of this write cycle.

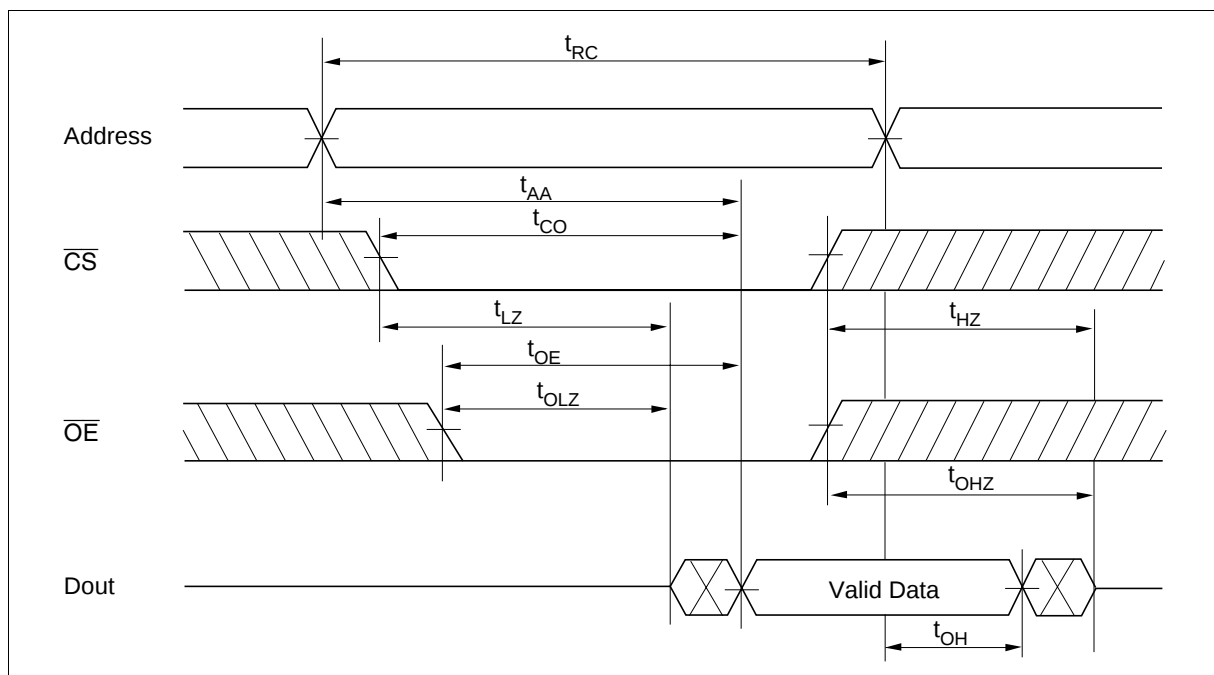
10. Dout is the read data of next address.

11. If  $\overline{CS}$  is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.

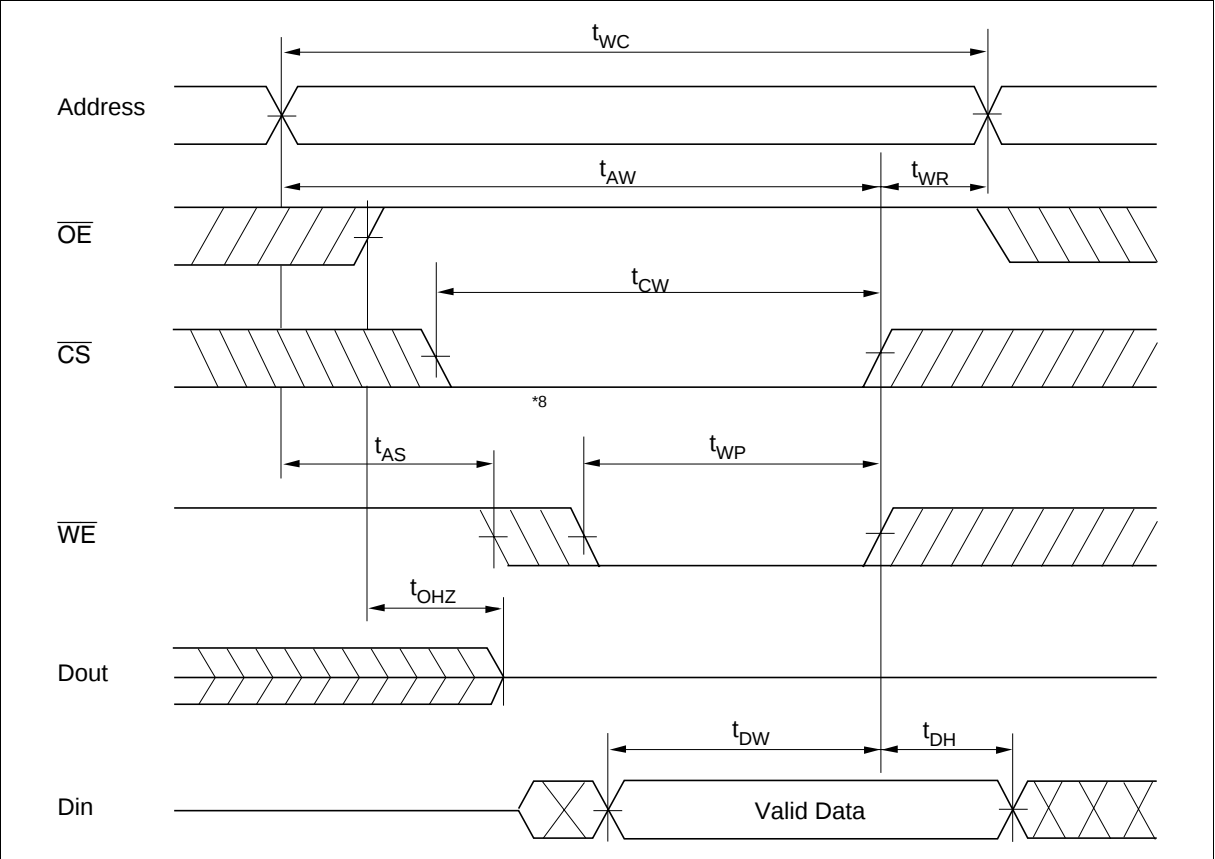
12. In the write cycle with  $\overline{OE}$  low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.  $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

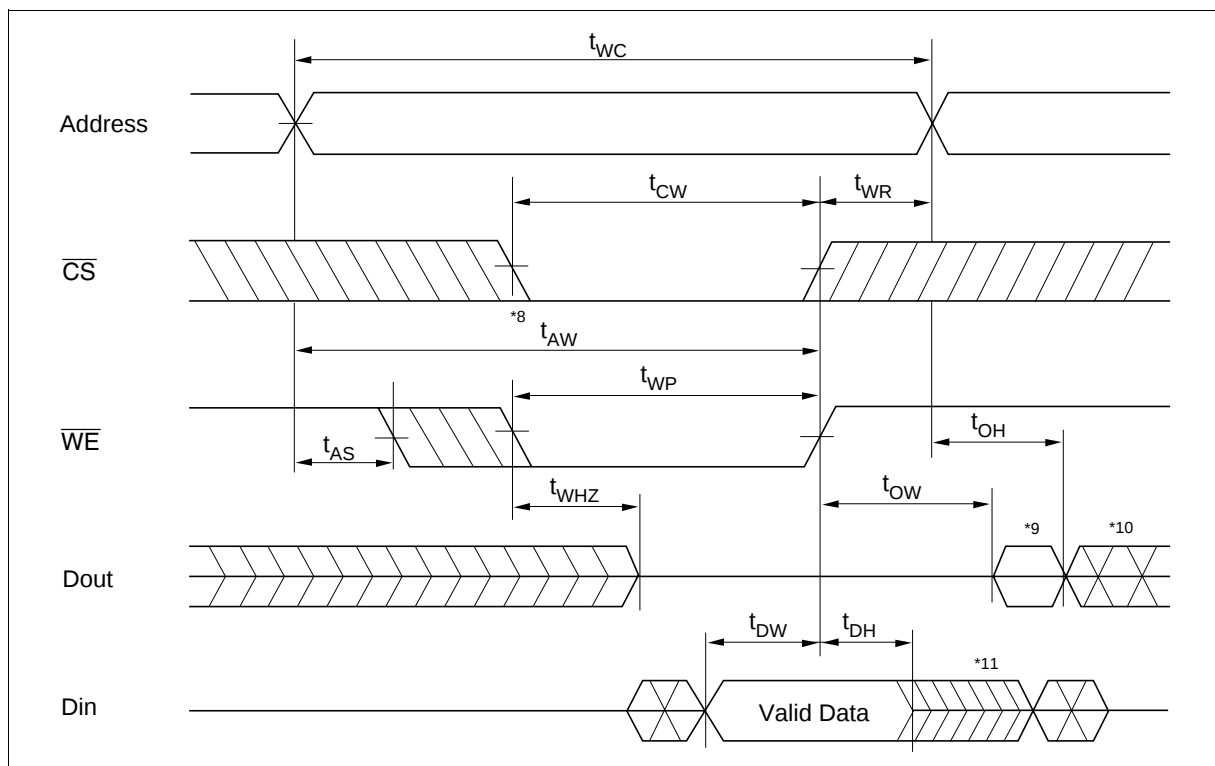
## Timing Waveforms

### Read Timing Waveform ( $\overline{WE} = V_{IH}$ )



Write Timing Waveform (1) ( $\overline{\text{OE}}$  Clock)



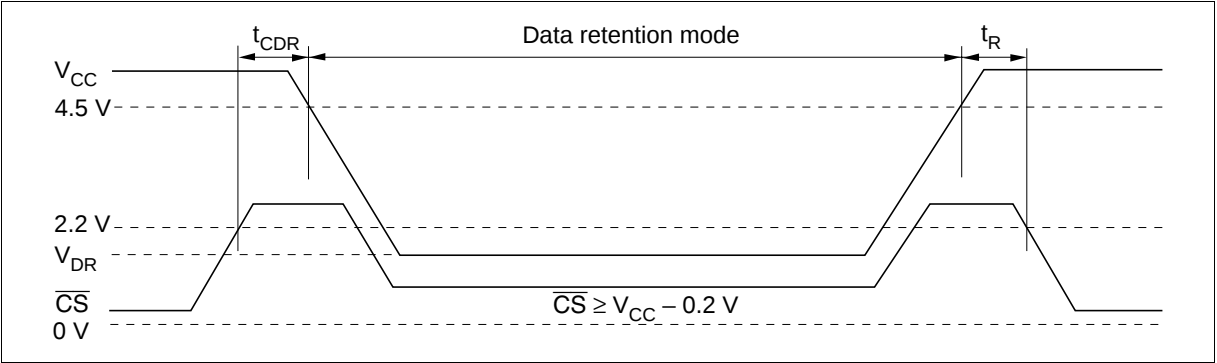
Write Timing Waveform (2) ( $\overline{\text{OE}}$  Low Fixed)

Low V<sub>CC</sub> Data Retention Characteristics (Ta = -20 to +70°C)

| Parameter                            | Symbol            | Min                | Typ   | Max  | Unit | Test conditions*3                                                                 |
|--------------------------------------|-------------------|--------------------|-------|------|------|-----------------------------------------------------------------------------------|
| V <sub>CC</sub> for data retention   | V <sub>DR</sub>   | 2                  | —     | —    | V    | $\overline{CS} \geq V_{CC} - 0.2\text{ V}$ , Vin ≥ 0 V                            |
| Data retention current               | I <sub>CCDR</sub> | —                  | 0.8*4 | 20*1 | μA   | $V_{CC} = 3.0\text{ V}$ , Vin ≥ 0 V<br>$\overline{CS} \geq V_{CC} - 0.2\text{ V}$ |
|                                      |                   | —                  | 0.8*4 | 10*2 | μA   |                                                                                   |
| Chip deselect to data retention time | t <sub>CDR</sub>  | 0                  | —     | —    | ns   | See retention waveform                                                            |
| Operation recovery time              | t <sub>R</sub>    | t <sub>RC</sub> *5 | —     | —    | ns   |                                                                                   |

Notes: 1. For L-version and 10 μA (max.) at Ta = -20 to +40°C.  
2. For L-SL-version and 3 μA (max.) at Ta = -20 to +40°C.  
3.  $\overline{CS}$  controls address buffer,  $\overline{WE}$  buffer,  $\overline{OE}$  buffer, and Din buffer. In data retention mode, Vin levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.  
4. Typical values are at V<sub>CC</sub> = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.  
5. t<sub>RC</sub> = read cycle time.

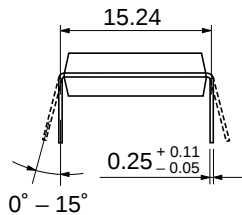
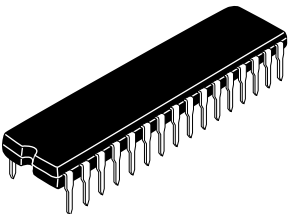
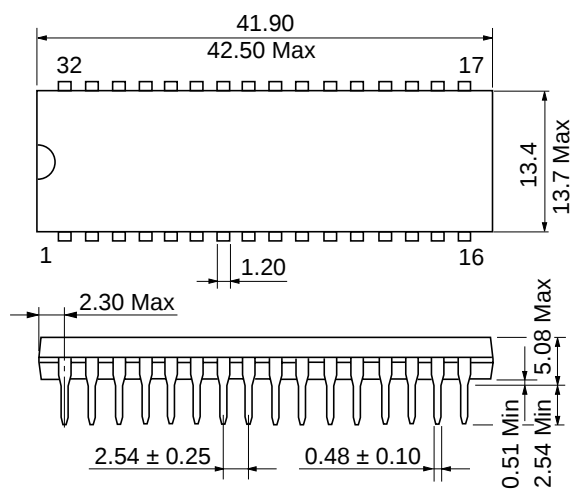
Low V<sub>CC</sub> Data Retention Timing Waveform ( $\overline{CS}$  Controlled)



Package Dimensions

HM628512CLP Series (DP-32)

As of January, 2002  
Unit: mm



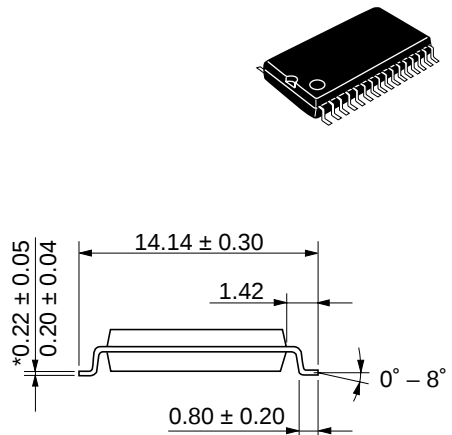
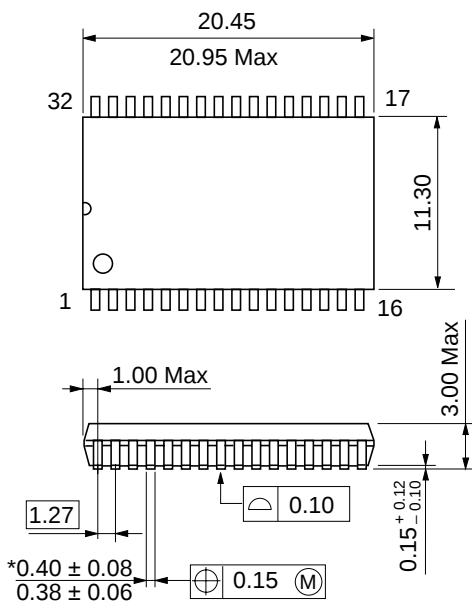
|                        |          |
|------------------------|----------|
| Hitachi Code           | DP-32    |
| JEDEC                  | —        |
| JEITA                  | Conforms |
| Mass (reference value) | 5.1 g    |

HM628512C Series

Package Dimensions (cont.)

HM628512CLFP Series (FP-32D)

As of January, 2002  
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

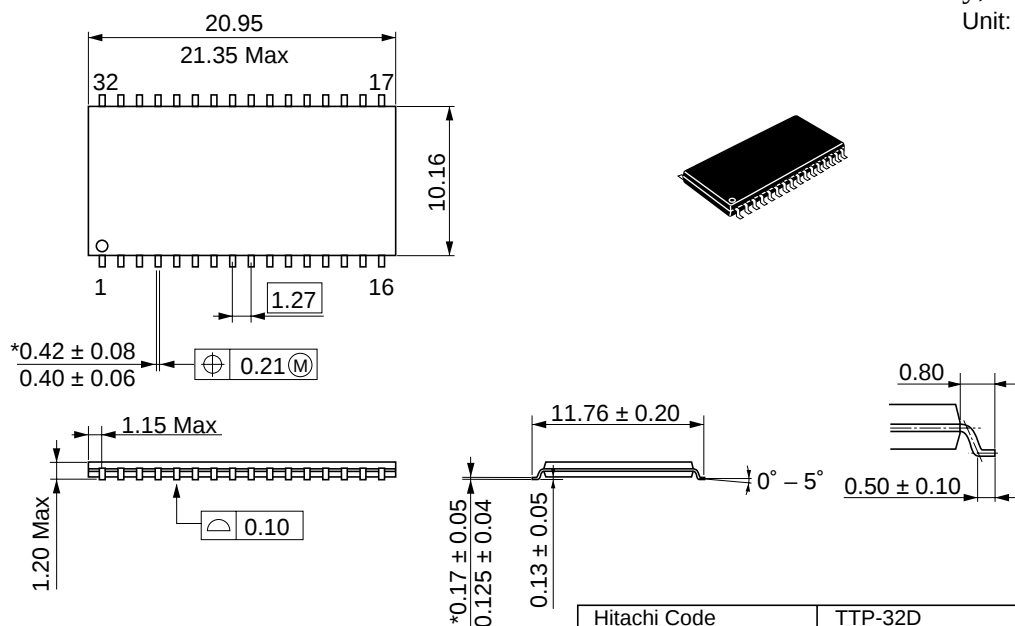
|                        |          |
|------------------------|----------|
| Hitachi Code           | FP-32D   |
| JEDEC                  | Conforms |
| JEITA                  | —        |
| Mass (reference value) | 1.3 g    |

# Package Dimensions (cont.)

## HM628512CLTT Series (TTP-32D)

As of January, 2002

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

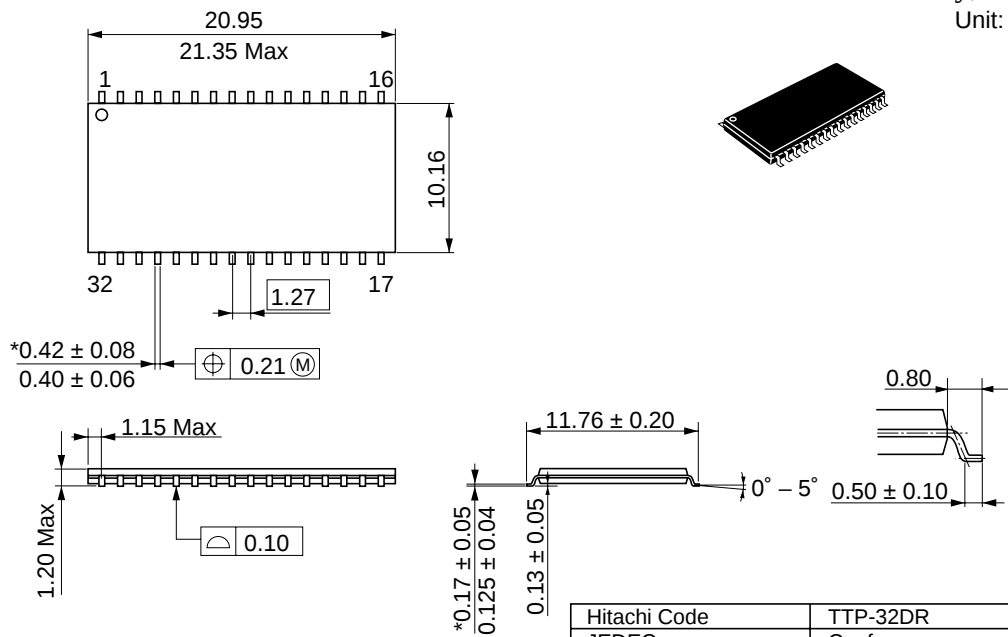
|                        |          |
|------------------------|----------|
| Hitachi Code           | TTP-32D  |
| JEDEC                  | Conforms |
| JEITA                  | —        |
| Mass (reference value) | 0.51 g   |

HM628512C Series

Package Dimensions (cont.)

HM628512CLRR Series (TTP-32DR)

As of January, 2002  
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

|                        |          |
|------------------------|----------|
| Hitachi Code           | TTP-32DR |
| JEDEC                  | Conforms |
| JEITA                  | —        |
| Mass (reference value) | 0.51 g   |

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Semiconductor & Integrated Circuits  
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Tel: (03) 3270-2111 Fax: (03) 3270-5109

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### For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1> (408) 433-0223

Hitachi Europe Ltd.  
Electronic Components Group  
Whitebrook Park  
Lower Cookham Road  
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World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon Hong Kong  
Tel: <852>-2735-9218  
Fax: <852>-2730-0281  
URL: <http://semiconductor.hitachi.com.hk>

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