DD-00429

ARINC 429 MICROPROCESSOR INTERFACE

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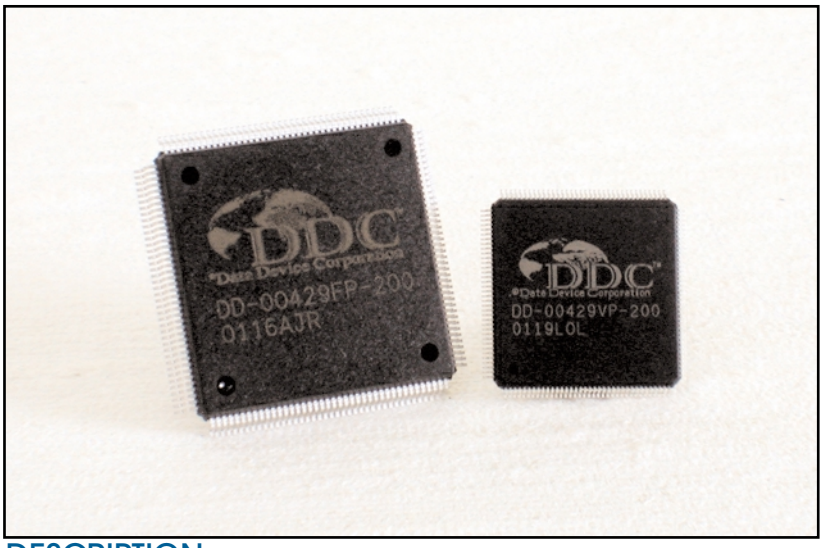

DESCRIPTION

DDC's DD-00429 provides a complete and flexible interface between a microprocessor and an ARINC 429 data bus. The DD-00429 interfaces to a processor through a 128 x 32 bit static ram as well as four 32 x 32 receive FIFOs and two 32 x 32 transmit FIFOs. The DD-00429 can be easily interfaced to 8- or 16-bit processors via a buffered shared RAM configuration.

The DD-00429, when configured with two Transceivers, supports four ARINC 429 Receive channels (Rx0, Rx1, Rx2 and Rx3) each receiving data independently. The receive data rates (high or low speed) for channel Rx0 and Rx1 can be programmed independently from Rx2 and Rx3. The DD-00429 can decode and sort data based on the ARINC 429 Label and SDI bits via the Data Match Processor, and store it in RAM and/or FIFOs via the Data Store Processor.

The DD-00429, when configured with two Line Drivers, supports two ARINC 429 Transmit channels (Tx0 and Tx1) and can transmit data independently. The transmit data rate can also be programmed independently. There are two 32 x 32 bit FIFOs for each of the transmitters that send out data.

The DD-00429 has the capability of programming three general purpose interrupts as well as generating an interrupt based on an error condition. The general purpose interrupts can be programmed to trigger other external hardware. They can either be LEVEL or PULSE driven.

The features built into the DD-00429 enable the user to off-load the host processor and use that processing time to implement operations other than polling the ARINC 429 Bus. The decoding and sorting of data allows the user to gather data much quicker than past designs. If the user requires a microprocessor in the avionics box, this device will facilitate a clean and quick design.

FEATURES

- Four ARINC 429 Receive Channels, (configured with Transceivers)
- Two ARINC 429 Transmit Channels (configured with Drivers)
- 128 x 32 Shared RAM Interface
- Label and Destination Decoding and Sorting
- Two 32 x 32 Transmit FIFO's
- Four 32 x 32 Receive FIFO's
- Interfaces Easily to 8- or 16-Bit Microprocessor
- Built-in Fault Detection Circuitry
- Free "C" Library Software
- Application Note AN/A-6 "FAQ's"

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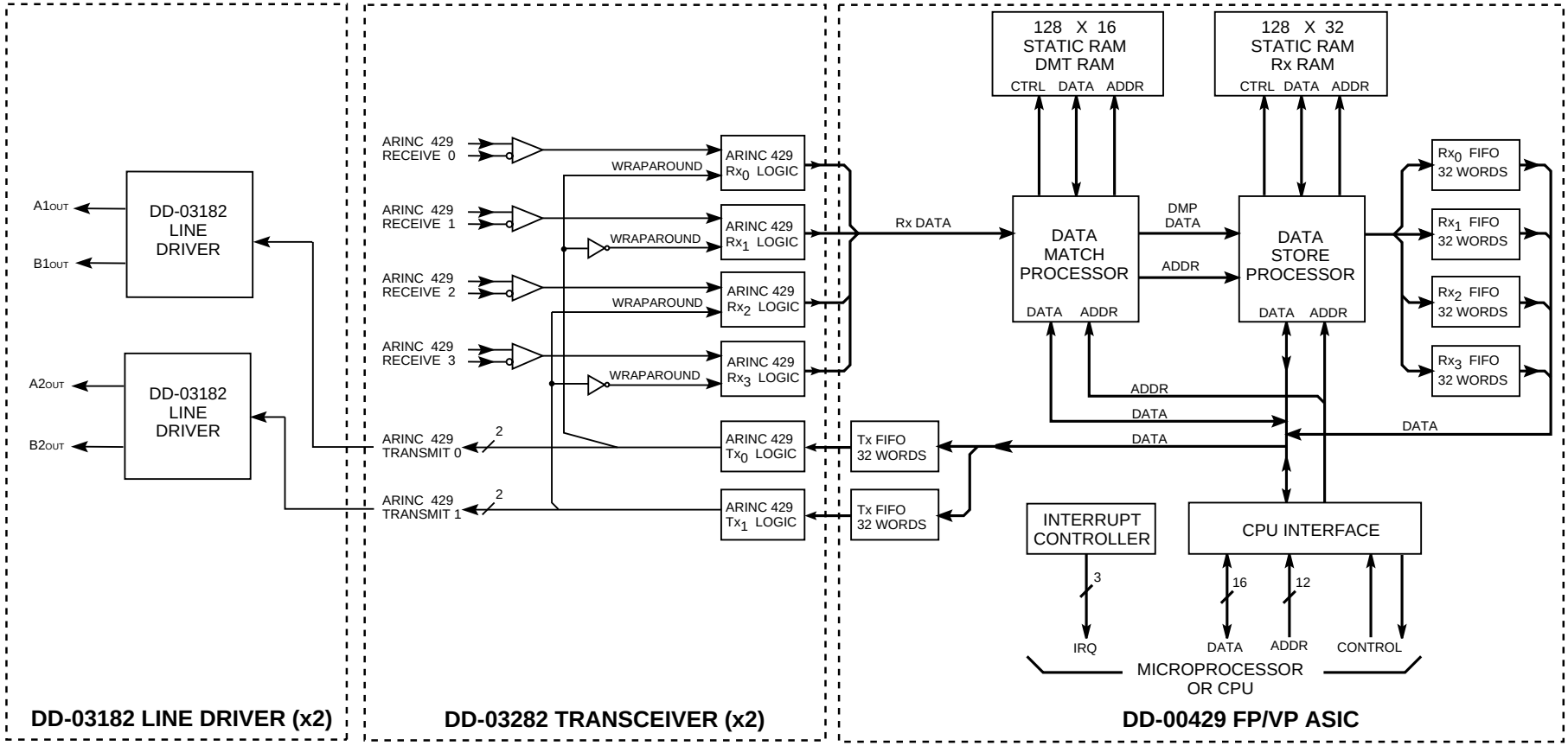


FIGURE 1. CHIP SET BLOCK DIAGRAM

TABLE 1. DD-00429 ABSOLUTE MAXIMUM RATINGS (TC = +25°C UNLESS OTHERWISE SPECIFIED)			
PARAMETER	**MIN**	**MAX**	**UNITS**
DC Supply Voltage	-0.3	7.0	Vdc
Signal Input Voltage (logic inputs)	-0.3	Vdd+0.3	Vdc
Storage Temperature	-85	125	°C
Operating Temperature	-40	85	°C
Lead Temperature (soldering)		280 (for 3 sec)	°C
Body Temperature (soldering)		210 (for 30 sec)	°C

TABLE 2. DD-00429 SPECIFICATIONS (TC = +25°C UNLESS OTHERWISE SPECIFIED)					
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**COMMENTS**
LOGIC INPUTS/OUTPUTS					
DC Supply Voltage	Vdd	4.5	5.5	Vdc	
DC Supply Current	Idd		42.2	mA	Device operation @ 16 MHz, Typical Idd = 38.4 mA @ 5.0V. (@85°C)
Schmitt “0” Threshold	Vt-		0.2*Vdd	Vdc	RESET RC*, 16 MHZ CLOCK
Schmitt “1” Threshold	Vt+	0.8*Vdd		Vdc	RESET RC*, 16 MHZ CLOCK
Schmitt Hysteresis	Vh	1		Vdc	RESET RC*, 16 MHZ CLOCK
Input Logic Voltage Low	Vil		0.8	Vdc	All other Inputs. (See Note 1).
Input Logic Voltage High	Vih	2.0		Vdc	All other Inputs. (See Note 1).
Input Logic Current Low	Iil	-25.3	-137	µA	Input pins with internal pull-up logic: INT/MOT*, 8/16*, ZERO WAIT MODE and MASTER RESET* @ Vdd = 5.5V
Input Logic Current Low	Iil	-1.0	1.0	µA	All other Inputs. (See Note 1).
Input Logic Current High	Iih	-1.0	1.0	µA	All other Inputs. (See Note 1).
Output Voltage Logic Low	Vol		0.4	Vdc	Io1=3.84 mA minimum @Vdd= 4.5V. (See note 2)
Output Voltage Logic High	Voh	2.4		Vdc	Ioh=3.84 mA minimum @Vdd= 4.5V. (See note 2)
Output Leakage Current, Hi-Z	Ioz	-10	10	µA	For TXDB0-TXDB15, D0-D15, READY, DTACK*, ERROR*, IRQ3*, IRQ2* and IRQ1 @ vdd = 5.5V

NOTES:
1. TTL compatible input logic voltage levels at CMOS input logic current levels.
2. CMOS output logic voltage at current levels.

ARINC 429 RECEIVERS

The DD-00429 supports four ARINC 429 inputs, designated Receive channels 0 through 3 (Rx0, Rx1, Rx2 and Rx3). The architecture of each of the four receiver circuits is identical and each receives data independently. ARINC 429 data is directly received into the ARINC 429 transceiver. Input protection, in accordance with the ARINC 429 specification, is provided along with voltage level translation from +5 V bipolar, nonreturn-to-zero data to conventional, +5 V logic levels.

Receive Data Rates: Data rates can be programmed for channels 0 and 1 independently of channels 2 and 3 via bits 2 and 3 of Arinc Control Register 2. The receiver circuitry will successfully decode an incoming ARINC 429 data stream as long as the data rate is within ±5% of the nominal rate as determined by the Hi Speed/Low Speed Bit and the associated ARINC Clock input (ARINC CLK 0 or ARINC CLK 1). The two 1 MHz ARINC clock inputs may be tied to the 1 MHz clock output or may be connected to another clock source.

The ARINC CLK input should nominally be 10 times (for High-Speed Mode) or 80 times (for Low-Speed mode) the desired ARINC Data Rate. ARINC CLK 0 is used to synchronize channels Rx0 and Rx1 while ARINC CLK 1 is used to synchronize channels Rx2 and Rx3.

Filtering and Sorting Rx Data: The receiver circuitry converts the serial data stream into a 32-bit-wide parallel data word. The 32-bit word is processed internally by a Data Match Processor (DMP). It compares the incoming data to a table of data initialized by the processor. This determines what incoming data is to be saved, where it is going to be saved, and if any interrupts are to be generated. The table of data is stored in a 128 word x 16 bit Data Match Table (DMT) RAM. When a match between the received ARINC 429 data and the criteria stored in a DMT entry is found, the received data, the storage address and modes, and interrupt parameters are passed to the Data Store Processor (DSP). The storage address in the Receive RAM is the address of the first matching DMT entry minus 200 hex.

There are three requirements that must be met in order to match incoming ARINC 429 data to each DMT entry:

1) **System Address Label:** Bits 0-7 of the DMT are compared to the System Address Label (SAL) of the incoming ARINC 429 data word. If the DMT SAL entry is zero then the SAL of the incoming data word is ignored (or considered a match).

2) **Source/Destination Bits:** Bits 8 and 9 of each DMT entry are compared to the Source/Destination (S/D) bits of the incoming ARINC 429 data word. If these bits match, or if Bit 10 of the DMT entry is set to a 1, then the S/D bit comparison is considered a match. It is also possible, through DMP Control Register 1, to enable “All Call Mode” as defined in the ARINC 429 specification. When enabled for a particular receive channel, the S/D bits will be considered a match when the incoming ARINC 429 data contains a 00 in its S/D bit pair.

3) **Receive Channel Number:** Bits 12 and 13 of each DMT entry are compared to the number of the channel which received the ARINC 429 data.

A Data Match has occurred when all of the previous conditions are satisfied; the data will then be stored in a RAM location whose address equals the matching DMT entry minus 200 hex.

Bit 11 of each DMT entry, when set, will cause the incoming ARINC 429 data to be stored in the corresponding receive channel FIFO (as well as the Rx RAM) when the data match conditions are met.

Bits 14 and 15 of each DMT entry provide the ability to cause one of three general purpose interrupts upon a data match condition. If set to “00” then no interrupt will occur upon a data match condition (more information on interrupts is described later).

ARINC 429 TRANSMITTER(S)

The DD-00429 supports two ARINC 429 transmitters. Each of these channels transmits data independently and are designated Tx0 and Tx1. The transmit output of the DD-00429 is a TTL encoded digital data stream which can be connected directly to the ARINC 429 line driver.

Transmit Data Rates: Data rates can be programmed for Channels 0 and 1 independently. The transmit data rate is determined by the High-Speed/Low-Speed Bit for each of the Tx channels in Arinc Control Register 1 and the associated ARINC Clock input (ARINC CLK 0 or ARINC CLK 1). The two, 1 MHz ARINC clock inputs may be tied to the 1 MHz clock output or they may be connected to another clock source to achieve transmit data rates other than 100 kHz or 12.5 kHz. The transmit clock input should be 10 times (for High-Speed Mode) or 80 times (for Low-Speed mode) the desired ARINC transmit data rate.

Transmit FIFOs: Each transmitter channel is provided with an output FIFO which is 32 words deep by 32 bits wide. When writing data to the Tx FIFO, the associated Disable Tx(n) bit in ARINC Control Register 2 can be set to a logic zero until the FIFO is loaded with the desired data. Upon setting the Disable Tx(n) low the transmit channel will send the 32-bit message words with appropriate interword gaps on the ARINC 429 output. A status bit indicating that the FIFO is empty is supplied for each transmitter in the ARINC Status Register.

Wraparound testing can be performed from Tx0 to Rx0 and Rx1, and from Tx1 to Rx2 and Rx3. The data received on Rx1 and Rx3 in wraparound test mode is inverted. Wraparound testing is enabled by setting the appropriate bits in Arinc Control Register 1. The parity of the transmitted word can be altered to no parity (instead of the usual odd parity) by setting the associated Tx(n) Parity bit in the Arinc Control Register 1. This is useful to verify proper operation of the parity check circuitry for each of the receive circuits during wraparound test mode.

PROCESSOR INTERFACE

The processor interface allows for the use of either an 8- or 16-bit data bus. Intel or Motorola control signal formats can also be used.

INTERRUPT OPERATIONAL MODES

The DD-00429 provides four interrupt outputs. Three of these interrupt outputs (IRQ1, IRQ2, and IRQ3) are general purpose programmable interrupts. The fourth interrupt is an Error interrupt output which is specifically used to provide indications of various error conditions and is nonmaskable.

ERROR INTERRUPT OPERATION

When an error condition occurs, the $\overline{\text{ERROR}}$ output pin goes low to indicate the presence of an error. The error pin will go high again when the Error Status Register is clear. Each of these bits is cleared by either reading the Error Status Register or removing the error condition.

GENERAL PURPOSE INTERRUPTS

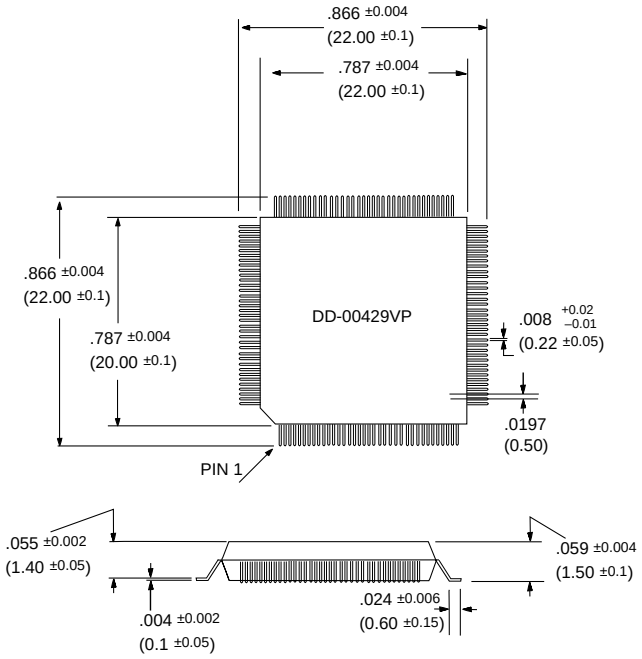
The three general purpose interrupt outputs can be used for multilevel interrupts or to trigger other external hardware for various conditions. Each condition can be mapped to any one of the three general purpose interrupts or disabled (by mapping to IRQ0 which does not exist). Each interrupt output can be programmed to be either a LEVEL interrupt or PULSE interrupt via the associated IRQ Control Register 2. When programmed for pulse interrupt mode, the associated interrupt pin will go low for 1 µS and return high again. When programmed for LEVEL interrupt mode, the interrupt will remain until the associated IRQ Status Register is read, thus clearing the associated bits in each interrupt register.

Each of the individual interrupt registers can be masked by setting their corresponding bit in IRQ Control Register 1. It should be noted that the masking function only prevents the associated IRQ pin from becoming active. When the mask bit is cleared, an interrupt can occur in LEVEL IRQ mode if one or more interrupt conditions occurred during the time when the mask was set. If the user needs to ensure the interrupt will not occur upon clearing the mask bit, the CPU should be programmed to read the associated interrupt status register immediately prior to clearing the IRQ mask bit.

ZERO WAIT MODE OPERATION

When Zero Wait Mode is enabled by not grounding the ZERO WAIT pin, the host microprocessor may read data from the DD-00429 shared memory resources (DMT and Rx RAM) without using the READY or DTACK signals to insert wait states into the microprocessor cycle. This is accomplished by an additional “dummy read” of the desired address. This dummy read causes the DD-00429 to fetch the data from the source and place it in a latch. The data can then be read from the latch (word-by-word or byte-by-byte) by reading the same addresses. Thus for a 32-bit read in 8-bit mode, the microprocessor would perform a total of five read operations. The first read would be the dummy read; subsequent reads would transfer the data.

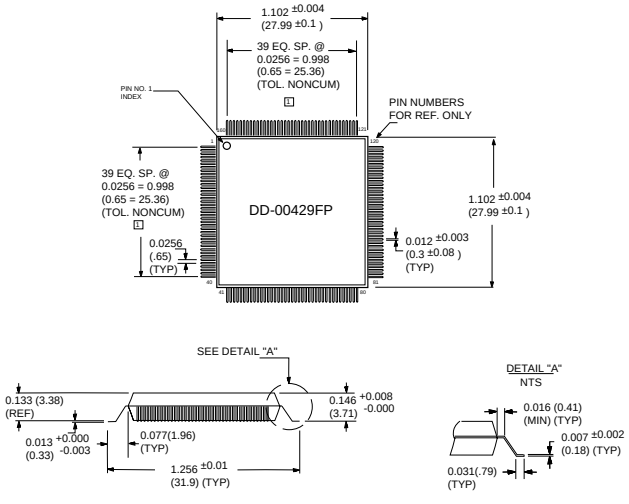
TABLE 3. DD-00429VP (144-PIN TQFP) ASIC PINOUTS							
PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	+5V	37	+5V	73	+5V	109	+5V
2	TX DB11	38	XTAL1 (N/C)	74	OSC CLK OUT (N/C)	110	$\overline{\text{RESET 1}}$
3	TX DB12	39	GND	75	BIST DMT (N/C)	111	$\overline{\text{CW STRB1}}$
4	TX DB13	40	TSB2 (N/C)	76	BIST RAM 7 (N/C)	112	EN TX1 OUT
5	TX DB14	41	TSB3 (N/C)	77	BIST RAM 24 (N/C)	113	TX1 EMPTY
6	TX DB15	42	TSA0 (N/C)	78	D0	114	$\overline{\text{LD TX1 HI}}$
7	$\overline{\text{EN RX1}}$	43	TSA1 (N/C)	79	D1	115	$\overline{\text{LD TX1 LOW}}$
8	$\overline{\text{EN RX0}}$	44	TSA2 (N/C)	80	D2	116	+5V
9	SELECT	45	TSA3 (N/C)	81	D3	117	GND
10	$\overline{\text{RX RDY1}}$	46	TMA0 (N/C)	82	D4	118	+5V
11	$\overline{\text{RX RDY0}}$	47	TMA1 (N/C)	83	D5	119	16 MHZ CLOCK
12	GND	48	TMA2 (N/C)	84	D6	120	$\overline{\text{EN RX3}}$
13	GND	49	TMA3 (N/C)	85	D7	121	$\overline{\text{EN RX2}}$
14	GND	50	TMA4 (N/C)	86	GND	122	$\overline{\text{RX RDY3}}$
15	INT/ $\overline{\text{MOTO}}$	51	TMA5 (N/C)	87	+5V	123	$\overline{\text{RX RDY2}}$
16	8/$\overline{16}$	52	TMA6 (N/C)	88	GND	124	+5V
17	+5V	53	TMA7 (N/C)	89	+5V	125	GND
18	GND	54	TSB0 (N/C)	90	D8	126	$\overline{\text{RESET 0}}$
19	A0	55	TSB1 (N/C)	91	D9	127	$\overline{\text{CW STRB 0}}$
20	A1	56	+5V	92	D10	128	EN TX0 OUT
21	A2	57	GND	93	D11	129	TX0 EMPTY
22	A3	58	TMB4 (N/C)	94	D12	130	$\overline{\text{LD TX0 HI}}$
23	A4	59	TMB5 (N/C)	95	D13	131	$\overline{\text{LD TX0 LOW}}$
24	A5	60	TMB6 (N/C)	96	D14	132	GND
25	A6	61	TMB7 (N/C)	97	D15	133	TX DB0
26	A7	62	ZERO WAIT MODE	98	GND	134	TX DB1
27	A8	63	READY	99	GND	135	TX DB2
28	A9	64	$\overline{\text{RD}}$ or $\overline{\text{DS}}$	100	$\overline{\text{IRQ3}}$	136	TX DB3
29	A10	65	$\overline{\text{WR}}$ or RD/$\overline{\text{WR}}$	101	$\overline{\text{IRQ2}}$	137	TX DB4
30	$\overline{\text{CS0}}$	66	$\overline{\text{DTACK}}$	102	$\overline{\text{IRQ1}}$	138	TX DB5
31	$\overline{\text{CS1}}$	67	$\overline{\text{ERROR}}$	103	$\overline{\text{RESET RC}}$	139	TX DB6
32	CS2	68	$\overline{\text{MASTER RESET}}$	104	ARINC CLK OUT	140	TX DB7
33	BIST R3 (N/C)	69	+5V	105	ARINC CLK 1	141	TX DB8
34	GND	70	BIST TOA (N/C)	106	ARINC CLK 0	142	TX DB9
35	+5V	71	BIST TOB (N/C)	107	BIST R2 (N/C)	143	TX DB10
36	GND	72	GND	108	GND	144	GND



DIMENSIONS IN INCHES (MILLIMETERS).

FIGURE 2. DD-00429VP MECHANICAL OUTLINE (144-PIN TQFP)

TABLE 4. DD-00429FP (160-PIN PQFP) ASIC PINOUTS							
PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	+5V	41	+5V	81	+5V	121	+5V
2	TX DB11	42	XTAL1 (N/C)	82	OSC CLK OUT (N/C)	122	$\overline{\text{RESET 1}}$
3	TX DB12	43	GND	83	BIST T1A (N/C)	123	$\overline{\text{CW STRB1}}$
4	TX DB13	44	TSB2 (N/C)	84	BIST T1B (N/C)	124	EN TX1 OUT
5	TX DB14	45	TSB3 (N/C)	85	BIST DMT (N/C)	125	TX1 B IN
6	TX DB15	46	TSA0 (N/C)	86	BIST RAM7 (N/C)	126	TX1 A IN
7	$\overline{\text{EN RX1}}$	47	TSA1 (N/C)	87	BIST RAM24 (N/C)	127	TX1 EMPTY
8	$\overline{\text{EN RX0}}$	48	TSA2 (N/C)	88	D0	128	$\overline{\text{LD TX1 HI}}$
9	SELECT	49	TSA3 (N/C)	89	D1	129	$\overline{\text{LD TX1 LOW}}$
10	$\overline{\text{RX RDY1}}$	50	TMA0 (N/C)	90	D2	130	+5V
11	$\overline{\text{RX RDY0}}$	51	TMA1 (N/C)	91	D3	131	GND
12	GND	52	TMA2 (N/C)	92	D4	132	+5V
13	GND	53	TMA3 (N/C)	93	D5	133	16 MHZ CLOCK
14	GND	54	TMA4 (N/C)	94	D6	134	$\overline{\text{EN RX3}}$
15	INT/ $\overline{\text{MOTO}}$	55	TMA5 (N/C)	95	D7	135	$\overline{\text{EN RX2}}$
16	8/$\overline{16}$	56	TMA6 (N/C)	96	GND	136	$\overline{\text{RX RDY 3}}$
17	+5V	57	TMA7 (N/C)	97	+5V	137	$\overline{\text{RX RDY 2}}$
18	TX0 A	58	TSB0 (N/C)	98	GND	138	+5V
19	TX0 B	59	TSB1 (N/C)	99	+5V	139	GND
20	TX1 A	60	+5V	100	D8	140	$\overline{\text{RESET 0}}$
21	TX1 B	61	GND	101	D9	141	$\overline{\text{CW STRB0}}$
22	GND	62	TMB0 (N/C)		D10	142	EN TX0 OUT
23	A0	63	TMB1 (N/C)	103	D11	143	TX0B IN
24	A1	64	TMB2 (N/C)	104	D12	144	TX0A IN
25	A2	65	TMB3 (N/C)	105	D13	145	TX0 EMPTY
26	A3	66	TMB4 (N/C)	106	D14	146	$\overline{\text{LOAD TX0 HI}}$
27	A4	67	TMB5 (N/C)	107	D15	147	$\overline{\text{LD TX0 LOW}}$
28	A5	68	TMB6 (N/C)	108	GND	148	GND
29	A6	69	TMB7 (N/C)	109	GND	149	TX DB0
30	A7	70	ZERO WAIT MODE	110	$\overline{\text{IRQ3}}$	150	TX DB1
31	A8	71	READY	111	$\overline{\text{IRQ2}}$	151	TX DB2
32	A9	72	$\overline{\text{RD}}$ or $\overline{\text{DS}}$	112	$\overline{\text{IRQ1}}$	152	TX DB3
33	A10	73	$\overline{\text{WR}}$ or RD/ $\overline{\text{WR}}$	113	$\overline{\text{RESET RC}}$	153	TX DB4
34	$\overline{\text{CS0}}$	74	$\overline{\text{DTACK}}$	114	ARINC CLK OUT	154	TX DB5
35	$\overline{\text{CS1}}$	75	$\overline{\text{ERROR}}$	115	ARINC CLK 1	155	TX DB6
36	CS2	76	$\overline{\text{MASTER RESET}}$	116	ARINC CLK 0	156	TX DB7
37	BIST R3 (N/C)	77	+5V	117	BIST R0 (N/C)	157	TX DB8
38	GND	78	BIST TOA (N/C)	118	BIST R1 (N/C)	158	TX DB9
39	+5V	79	BIST TOB (N/C)	119	BIST R2 (N/C)	159	TX DB10
40	GND	80	GND	120	GND	160	GND



Notes:
1. LEAD CLUSTER TO BE CENTRALIZED ABOUT CASE CENTERLINE WITHIN ±0.010 (±0.25).
2. DIMENSIONS IN INCHES (MILLIMETERS).

FIGURE 3. DD-00429FP ASIC MECHANICAL OUTLINE (160-PIN PQFP)

ORDERING INFORMATION

Chip Set:
DD-00429XP - X00

Temperature Range:
2 = -40 - +85°C

ASIC Package Type:
P = Plastic

Lead Type:
F = 160-Pin Quad Flat Pack
V = 144-Pin TQFP

Note: The Line Drivers AND Transceivers are required to complete the ARINC 429 Interface (see additional ordering information). The DD-00429 is only the Microprocessor Interface/RAM/FIFO and Interrupt Controller.

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