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NN30421A

8A Synchronous DC-DC Step down Regulator
(V_{IN} = 4.75 V to 24 V, V_{OUT} = 0.75 V to 3.6 V)

FEATURES

- High-Speed Response DC-DC Step Down Regulator Circuit that employs Hysteretic Control System
- Skip (discontinuous) mode for Light Load Efficiency
- Up to 8 A Output Current
- Input VoltageRange : AV_{IN} : 4.75 V to 24 V
    PV_{IN} : 4.75 V to 24 V
    V_{REG} : 4.5 V to 5.5 V
- Output Voltage Range : 0.75 V to 3.6 V
- Selectable Switching Frequency
    : 220 kHz, 410 kHz, 580 kHz
- Adjustable Soft Start
- Low Operating and Standby Quiescent Current
- Power Good Indication for Output Over and Under Voltage
- Built-in Under Voltage Lockout (UVLO),
    Thermal Shut Down (TSD),
    Over Voltage Detection (OVD),
    Under Voltage Detection (UVD),
    Over Current Protection (OCP),
    Short Circuit Protection (SCP)
- 24pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)
    (Size : 4 mm × 4 mm × 0.7 mm, 0.5 mm pitch)

DESCRIPTION

NN30421A is a synchronous DC-DC Step down Regulator (1-ch) comprising of a Controller IC and two power MOSFETs employing hysteretic control system.

By this system, when load current changes suddenly, it responds at high speed and minimizes the changes of output voltage.

Since it is possible to use capacitors with small capacitance and it is unnecessary to add external parts for system phase compensation, this IC realizes downsizing of set and reducing in the number of external parts. Output voltage is adjustable by user. Maximum current is 8 A.

APPLICATIONS

High Current Distributed Power Systems such as
- ・ HDDs (Hard Disk Drives)
- ・ SSDs (Solid State Drives)
- ・ PCs
- ・ Game consoles
- ・ Servers
- ・ Security Cameras
- ・ Network TVs
- ・ Home Appliances
- ・ OA Equipment etc.

TYPICAL APPLICATION EXAMPLE
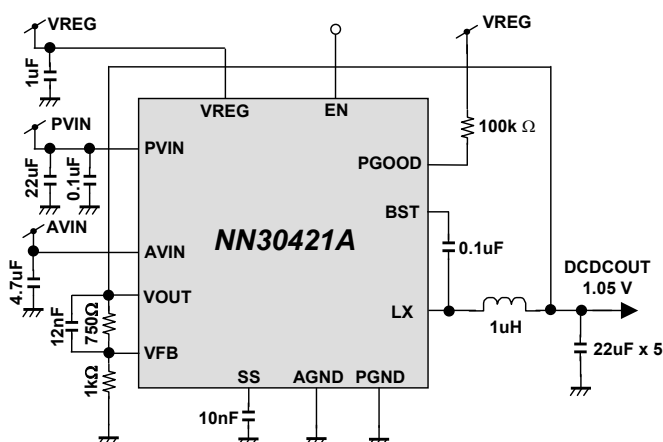
Notes) The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

EFFICIENCY CURVE
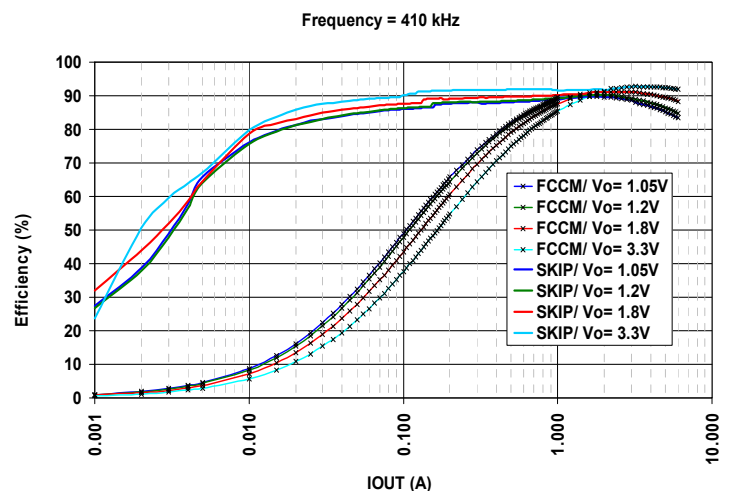
Frequency = 410 kHz

Condition :
    V_{IN} = 12V, V_{REG} = 5V, V_{OUT} Setting = 1.05V, 1.2 V, 1.8 V, 3.3 V,
    Switching Frequency = 410kHz, FCCM / Skip mode,
    L_O = 1 μH, C_O = 110 μF (22 μF x 5)

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ORDERING INFORMATION

Order Number	Feature	Package	Output Supply
NN30421A-VB	Maximum Output Current : 8A	24 pin HQFN	Emboss Taping

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V_{IN}	30	V	*1
	V_{REG}	6	V	*1
Operating free-air temperature	T_{opr}	-40 to $+85$	°C	*2
Operating junction temperature	T_{j}	-40 to $+150$	°C	*2
Storage temperature	T_{stg}	-55 to $+150$	°C	*2
Input Voltage Range	$V_{MODE},V_{FSEL},V_{OUT},V_{FB}, V_{EN}$	-0.3 to 6.0	V	*1
Output Voltage Range	V_{PGOOD}	-0.3 to 6.0	V	*1
	V_{LX}	-0.3 to $(V_{IN} + 0.3)$	V	*1 *3
ESD	HBM	2	kV	—

Notes) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute
maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it
is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
V_{IN} is voltage for AVIN, PVIN. $AV_{IN} = PV_{IN}$. VREG is voltage for VREG.
Do not apply external currents and voltages to any pin not specifically mentioned.
*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25 °C.
*3 : (V_{IN} + 0.3) V must not exceed 30 V.

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POWER DISSIPATION RATING

Package	$\theta_{j\text{-}a}$	$\theta_{j\text{-}C}$	PD (Ta = 25 °C)	PD (Ta = 85 °C)	Notes
24pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)	58.0 °C /W	7.2 °C / W	2.155 W	1.120 W	*1
	35.7 °C /W	4.7 °C / W	3.501 W	1.820 W	*2

Notes) For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

*1:Glass Epoxy Substrate (4 Layers) [Glass-Epoxy: 50 X 50 X 0.8 t (mm)]

*2:Glass Epoxy Substrate (4 Layers) [Glass-Epoxy: 50 X 50 X 1.57 t (mm)]

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Min.	Typ.	Max.	Unit	Notes
Supply voltage range	AV_{IN}	4.75	12	24	V	—
	PV_{IN}	4.75	12	24	V	—
	V_{REG}	4.5	5.0	5.5	V	—
Input Voltage Range	V_{MODE}	− 0.3	—	6.0	V	—
	V_{FSEL}	− 0.3	—	6.0	V	—
	V_{EN}	− 0.3	—	5.0	V	—
Output Voltage Range	V_{PGOOD}	− 0.3	—	6.0	V	—
	V_{LX}	− 0.3	—	V_{IN} + 0.3	V	*1

Note) Voltage values, unless otherwise specified, are with respect to GND.

GND is voltage for AGND, PGND. AGND = PGND

V_{IN} is voltage for AVIN, PVIN. V_{IN} = AV_{IN} = PV_{IN}.

Do not apply external currents and voltages to any pin not specifically mentioned.

*1 : (V_{IN} + 0.3) V must not exceed 30 V.

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ELECTRICAL CHARACTERISTICS

Co = 22 µF x 5, Lo= 1 µH, V_{OUT} Setting = 1.05 V, V_{IN} = AV_{IN} = PV_{IN} = 12 V, V_{REG} = 5 V,

Switching Frequency = 410 kHz, V_{MODE} = V_{REG} (FCCM), T_a = 25 °C $\pm$ 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current Consumption							
V_{IN} consumption current at active	I_{VDDACT}	V_{EN}= 5 V, I_{OUT} = 0 A V_{RFB1} = 750 Ω V_{RFB2} = 1k Ω V_{MODE} = GND (Skip mode)	—	220	300	µA	—
V_{REG} consumption current at active	$I_{VREGACT}$	V_{EN}= 5 V, I_{OUT} = 0 A V_{RFB1} = 750 Ω V_{RFB2} = 1k Ω V_{MODE} = GND (Skip mode)	—	430	550	µA	—
V_{IN} consumption current at standby	I_{VDDSTB}	V_{EN} = 0 V	—	2	4	µA	—
V_{REG} consumption current at standby	$I_{VREGSTB}$	V_{EN} = 0 V	– 1	—	1	µA	—
Logic Pin							
EN pin Low-level input voltage	V_{ENL}	—	—	—	0.3	V	—
EN pin High-level input voltage	V_{ENH}	—	1.5	—	5.0	V	—
EN pin leak current	I_{LEAKEN}	V_{EN} = 5 V	—	6.25	12.5	µA	—
MODE pin Low-level input voltage	V_{MODEL}	—	—	—	V_{REG} x 0.3	V	—
MODE pin High-level input voltage	V_{MODEH}	—	V_{REG} x 0.7	—	V_{REG}	V	—
MODE pin leak current	$I_{LEAKMODE}$	V_{MODE} = 5 V	—	3.25	6.5	µA	—
FSEL pin Low-level input voltage	V_{FSELL}	—	—	—	0.3	V	—
FSEL pin High-level input voltage	V_{FSELH}	—	—	V_{REG} – 0.1	—	V	*1
FSEL pin leak current	$I_{LEAKFSEL}$	V_{FSEL} = 5 V	—	15.0	25.0	µA	—

*1 : Typical design value.

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ELECTRICAL CHARACTERISTICS (Continued)

Co = 22 μF x 5, Lo= 1 μH, V_{OUT} Setting = 1.05 V, V_{IN} = AV_{IN} = PV_{IN} = 12 V, V_{REG} = 5 V,
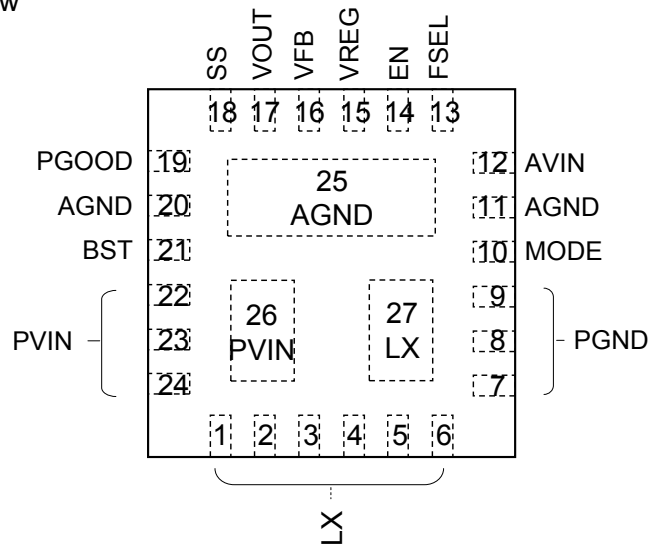
Switching Frequency = 410 kHz, V_{MODE} = V_{REG} (FCCM), T_a = 25 °C $\pm$ 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
VFB Characteristics							
VFB comparator threshold	V_{FBTH}	—	0.594	0.600	0.606	V	—
VFB pin leak current 1	$I_{LEAKFB1}$	V_{FB} = 0 V	– 1	—	1	μA	—
VFB pin leak current 2	$I_{LEAKFB2}$	V_{FB} = 6 V	– 1	—	1	μA	—
Under Voltage Lock Out							
VIN UVLO start voltage	$V_{IUVLODET}$	V_{IN} = 5 V to 0 V	3.05	3.75	4.45	V	—
VIN UVLO recover voltage	$V_{IUVLORMV}$	V_{IN} = 0 V to 5 V	3.2	3.9	4.6	V	—
VREG UVLO start voltage	$V_{RUVLODET}$	V_{IN} = 5 V to 0 V	3.5	3.8	4.1	V	—
VREG UVLO recover voltage	$V_{RUVLORMV}$	V_{IN} = 0 V to 5 V	3.9	4.2	4.5	V	—
PGOOD							
PGOOD Threshold 1 (V_{FB} ratio for UVD detect)	V_{THPG1}	V_{PGOOD} : High to Low	77	85	93	%	—
PGOOD Hysteresis 1 (V_{FB} ratio for UVD release)	V_{HYSPG1}	V_{PGOOD} : Low to High	3.5	5.0	6.5	%	—
PGOOD Threshold 2 (V_{FB} ratio for OVP detect)	V_{THPG2}	V_{PGOOD} : High to Low	107	115	123	%	—
PGOOD Hysteresis 2 (V_{FB} ratio for OVP release)	V_{HYSPG2}	V_{PGOOD} : Low to High	3.5	5.0	6.5	%	—
PGOOD ON resistance	R_{PGOOD}	—	—	10	15	Ω	—

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ELECTRICAL CHARACTERISTICS (Continued)

Co = 22 µF x 5, Lo= 1 µH, V_{OUT} Setting = 1.05 V, V_{IN} = AV_{IN} = PV_{IN} = 12 V, V_{REG} = 5 V,

Switching Frequency = 410 kHz, V_{MODE} = V_{REG} (FCCM), T_a = 25 °C $\pm$ 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DC-DC							
Line regulation	DD_{REGIN}	PV_{IN} = 6 V to 20 V I_{OUT} = 4 A	—	0.25	0.75	%/V	—
Load regulation	DD_{REGLD}	I_{OUT} = 10 mA to 4 A	—	3.5	—	%	*1
Efficiency 1	DD_{EFF1}	I_{OUT} = 100 mA V_{MODE}=GND (Skip mode) Measure V_{IN} Current.	—	81	—	%	*1
Efficiency 2	DD_{EFF2}	I_{OUT} = 4 A V_{MODE}=GND (Skip mode) Measure V_{IN} Current.	—	84	—	%	*1
Output ripple voltage 1	DD_{VRPL1}	I_{OUT} = 100 mA	—	20	—	mV [p-p]	*1
Output ripple voltage 2	DD_{VRPL2}	I_{OUT} = 4 A	—	20	—	mV [p-p]	*1
Load transient response	DD_{DVAC}	I_{OUT} = 100 mA to 4 A Δt = 0.5 A / µs	—	20	—	mV	*1
MIN Input and output voltage difference	DV	DV = PV_{IN} − V_{OUT}	—	2.5	—	V	*1

*1 : Typical design value.

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ELECTRICAL CHARACTERISTICS (Continued)

Co = 22 µF x 5, Lo= 1 µH, V_{OUT} Setting = 1.05 V, V_{IN} = AV_{IN} = PV_{IN} = 12 V, V_{REG} = 5 V,

Switching Frequency = 410 kHz, V_{MODE} = V_{REG} (FCCM), T_a = 25 °C $\pm$ 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
PROTECTION							
DC-DC output current limit	DD_{ILMT}	—	—	11	—	A	*1
DC-DC Output GND Short Protection Threshold	DD_{SHPTH}	V_{FB} = 0.6 V to 0.0 V	50	60	70	%	—
Soft-Start Timing							
SS Charge Current	I_{SSCHG}	V_{SS} = 0.3 V	—	2	4	µA	—
SS Discharge Resistance (Shut-down)	R_{SSDIS}	V_{EN} = 0 V	—	5	10	kΩ	—
Switching Frequency Adjustment							
DC-DC Switching Frequency 1	DD_{FSW1}	I_{OUT} = 4 A	—	220	—	kHz	*1
DC-DC Switching Frequency 2	DD_{FSW2}	I_{OUT} = 4 A	—	410	—	kHz	*1
DC-DC Switching Frequency 3	DD_{FSW3}	I_{OUT} = 4 A	—	580	—	kHz	*1

*1 : Typical design value.

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PIN CONFIGURATION

Top View

PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1			Power MOSFET output pin
2			An inductor is connected and switching operation is carried out
3			between V_{IN} and GND.
4	LX	Output	Due to high current and large amplitude at this terminal,
5			the parasitic inductance and impedance of the routing path
6			can cause an increase in noise and a degradation in the efficiency. Routing path should be kept as short as possible.
7			
8	PGND	Ground	Ground pin for Power MOSFET
9			
10	MODE	Input	Skip (discontinuous) mode / FCCM (Forced Continuous Conduction Mode) select pin Skip mode is set at Low level input, FCCM is set at High level input.
11	AGND	Ground	Ground pin
20			
12	AVIN	Power supply	Power supply pin Recommended rise time (time to reach 90 % of set value) setting is greater than or equal to 10 µs and less than or equal to 1 s.
13	FSEL	Input	Frequency selection pin This is set to 410 kHz at Low level input, 220 kHz at High level input, and 580 kHz at open.
14	EN	Input	ON/OFF control pin DC-DC is stopped at Low level input, and it is started at High level input.

Note : Detailed pin descriptions are provided in the OPERATION and APPLICATION INFORMATION section.

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PIN FUNCTIONS

Pin No.	Pin name	Type	Description
15	VREG	Power supply	Power supply pin 　Recommended rise time (time to reach 90 % of set value) setting is 　greater than or equal to 10 µs and less than or equal to 1 s.
16	VFB	Input	Comparator negative input pin 　VFB terminal voltage is regulated to REF output (internal reference voltage). 　Since VFB is a high impedance terminal, it should not be routed near 　other noisy path (LX, BST, etc.) or an inductor 　Routing path should be kept as short as possible.
17	VOUT	Input	Output voltage sense pin 　Switching frequency is controlled by monitoring output voltage.
18	SS	Output	Soft start capacitor connect pin 　The output voltage at a start up is smoothly controlled 　by adjusting Soft Start time. 　Please connect capacitor between SS and GND.
19	PGOOD	Output	Power good open drain pin 　A pull up resistor between PGOOD and VREG terminal is necessary. 　Output is low during Over or Under Voltage Detection conditions.
20	AGND	Ground	Ground pin
21	BST	Output	Supply input pin for high side MOSFET gate driver 　Bootstrap operation is carried out in order to drive the gate voltage of High 　side Power MOSFET. Please connect a capacitor between BST and LX. 　Routing path should be kept as short as possible to minimize noise.
22 23 24	PVIN	Power supply	Power supply pin for Power MOSFET 　Recommended rise time (time to reach 90 % of set value) setting is 　greater than or equal to 10 µs and less than or equal to 1 s.
25	AGND	Ground	Ground pin for radiation of heat
26	PVIN	Power supply	Power supply pin for radiation of heat
27	LX	Output	Power MOSFET output pin for radiation of heat

Note : Detailed pin descriptions are provided in the OPERATION and APPLICATION INFORMATION section.

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FUNCTIONAL BLOCK DIAGRAM
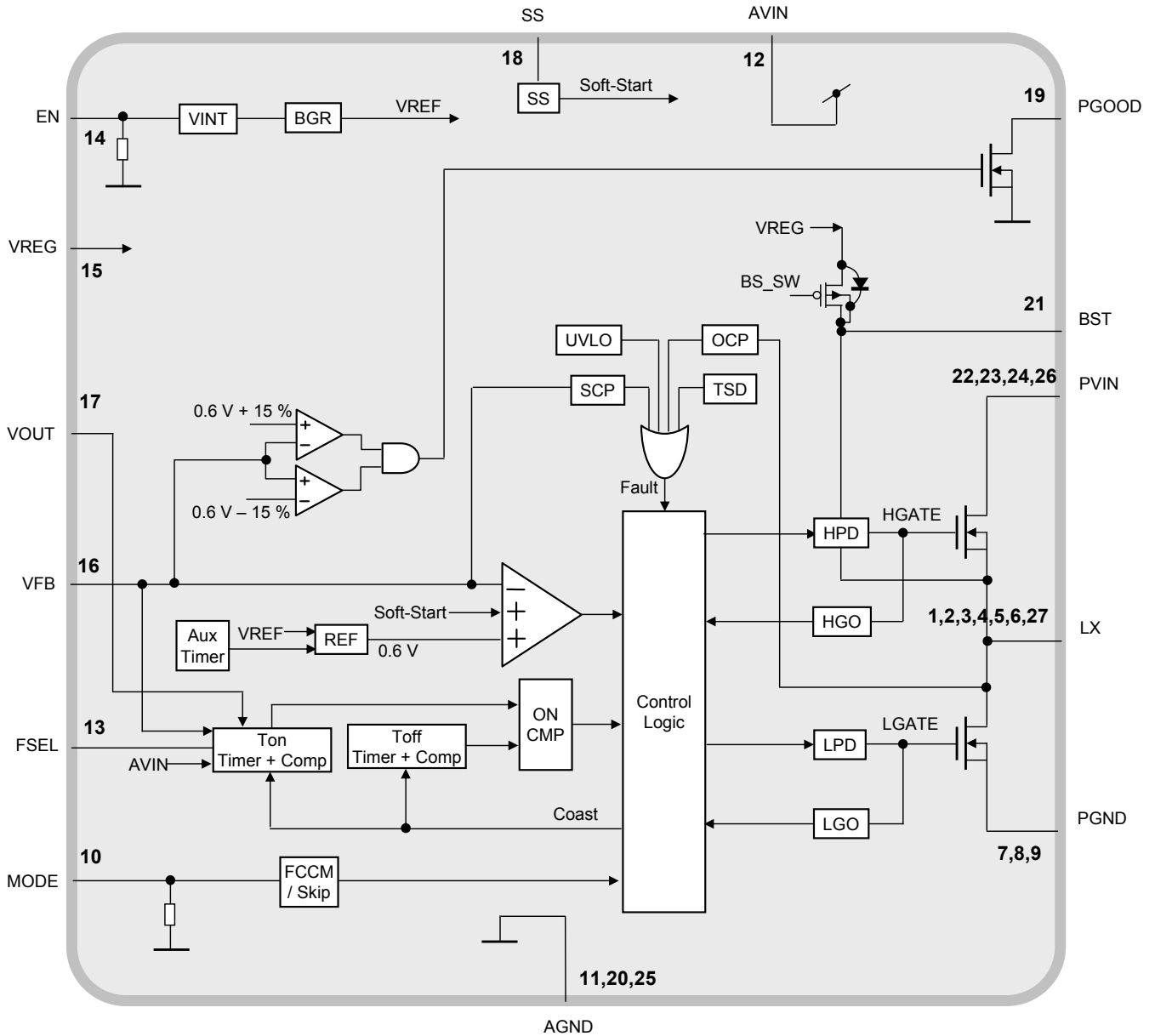
Notes) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

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OPERATION

1. Protection

(1) Over Current Protection (OCP) and
    Short Circuit Protection (SCP)

1) The Over Current Protection is activated at about 11 A
    (Typ.) This device uses pulse–by–pulse valley
    current protection method. When the low side
    MOSFET is turned on, the voltage across the drain
    and source is monitored which is proportional to the
    inductor current. The high side MOSFET is only
    allowed to turn on when the current flowing in the low
    side MOSFET falls below the OCP level.
    Hence, during the OCP, the output voltage continues
    to drop at the specified current. OCP is a non–latch
    type protection.

2) The Short-Circuit Protection function is implemented
    when the output voltage decreases and the VFB pin
    reaches to about 60 % of the set voltage (0.6 V).
    If the VFB voltage stays below 60 % of the set
    voltage over 250 μs after SCP triggers, both
    high side and low side MOSFET will be latched
    off and the output will be discharged by internal
    MOSFET. Power reset or EN pin reset is necessary to
    activate the device again.
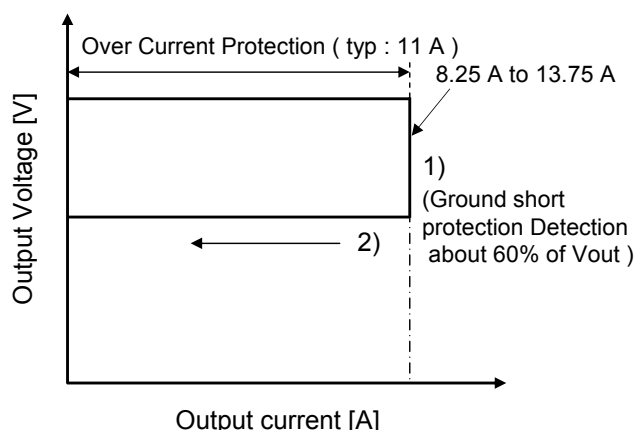
Figure : OCP and SCP Operation

(2) Over Voltage Detection (OVD)

If the VFB pin voltage exceeds 115 % of the set
voltage (0.6 V) and lasts more than 10 ns, Over
Voltage Detection will be triggered and PGOOD pin will
be pulled down. Furthermore, in an over voltage
condition, high side power MOSFET is turned off to
stop PWM operation, and low side power MOSFET is
turned on and held on until the inductor current starts to
flow back to the device (for both Skip mode and FCCM
settings). If the VFB pin voltage drops below 110 % of
the set voltage within 30 μs after Over Voltage
Detection triggers, PGOOD pin will be pulled up again
and PWM operation will resume. Otherwise, both high
side and low side MOSFET will be latched off and the
output will be discharged by internal MOSFET.
Power reset or EN pin reset is necessary to activate
the device again.

Note: PGOOD Pin is pulled up to VREG pin
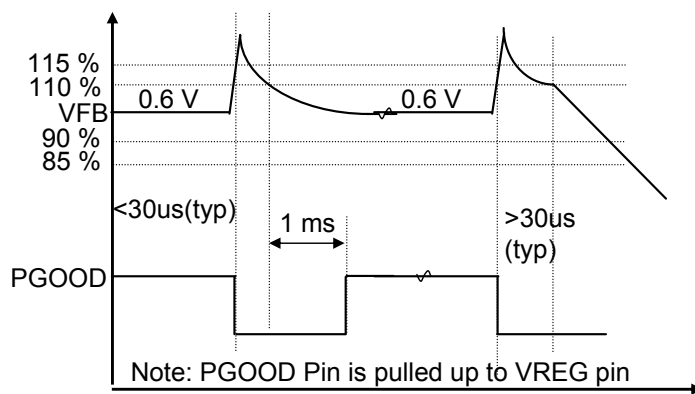
Figure : OVD Operation

(3) Output discharging function

When EN is low, the output is discharged by an internal
MOSFET. When EN is high, if the controller is turned off
by under-voltage-lock-out (UVLO), or the controller is
latched off by over-voltage-protection (OVP) or short-
circuit protection (SCP), the output is discharged by the
above said internal MOSFET.
The on resistance of the internal MOSFET is about 50 Ω.

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OPERATION (Continued)

1. Protection (Continued)

(4) Under voltage detection (UVD)

During the operation, if output voltage drops and the VFB pin voltage reaches 85 % of its set voltage (0.6 V), the MOSFET, the drain of which is connected to PGOOD pin, will turn on and pull the voltage of PGOOD to be low.
If the output voltage continues to drop and VFB pin voltage reaches 60 % of its set value (0.6 V), Short Circuit Protection (SCP) will be triggered.
If the output voltage returns to 90 % of its set value (0.6 V) before triggering Short Circuit Protection, the MOSFET that is connected to PGOOD pin will turn off after 1 ms and PGOOD voltage will become logic high.

Note: PGOOD Pin is pulled up to VREG pin
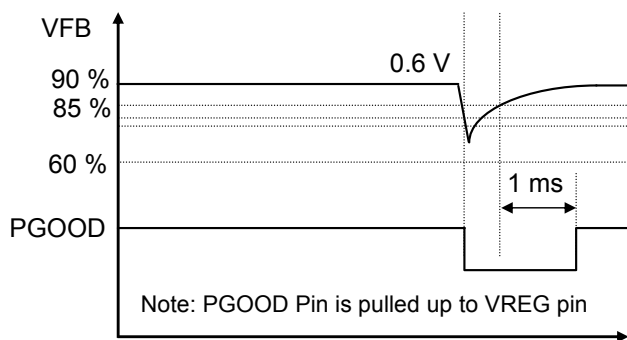
Figure : UVD Operation

(5) Thermal Shut Down (TSD)

When the IC internal temperature becomes more than about 140°C, TSD operates and DC-DC turns off.

2. Pin Setting

(1).Operating Mode Setting

The IC can operate at two different modes :
Skip (discontinuous) mode and
Forced Continuous Conduction Mode (FCCM).
In Skip mode, the IC is working under pulse skipping mechanism to improve efficiency at light load condition.
In FCCM, the IC is working at fixed frequency to avoid EMI issues.
The Operating Mode can be set by MODE pin as follows.

MODE pin	Mode
Low	Skip
High	FCCM

(2).Switching Frequency Setting

The IC can operate at three different frequency :
580kHz, 410 kHz and 220 kHz.
The Switching Frequency can be set by FSEL pin as follows.

FSEL pin	Frequency [kHz]
Low	410
High	220
Open	580

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OPERATION (Continued)

3.Output Voltage Setting

The Output Voltage can be set by external resistance of FB pin, and its calculation is as follows.

$$V_{OUT} = \left(1 + \frac{R_{FB1}}{R_{FB2}} \right) \times 0.6$$
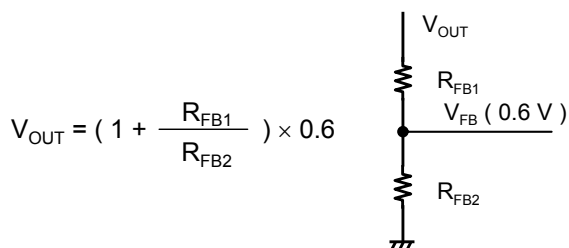
Below resistors are recommended for following typical output voltages

V_{OUT} [V]	R_{FB1} [Ω]	R_{FB2} [Ω]
3.3	4.5 k	1.0 k
1.8	2.0 k	1.0 k
1.2	1.5 k	1.5 k
1.05	750	1.0 k

Note: R_{FB2} can be set to a maximum value of 10 kΩ.
A larger R_{FB2} value will be more susceptible to noise.

VFB comparator threshold is adjusted to ± 1 %, but the actual output voltage accuracy becomes more than ±1 % due to the influence from the circuits other than VFB comparator.

4. Soft Start Setting

Soft Start function maintains the smooth control of the output voltage during start up by adjusting soft start time. When the EN pin becomes High, the current (2 µA) begin to charge toward the external capacitor (Css) of SS pin, and the voltage of SS pin increases linearly.
Because the voltage of VFB pin is controlled by the voltage of SS pin during start up, the voltage of VFB increase linearly to the regulation voltage (0.6 V) together with the voltage of SS pin and keep the regulation voltage after that. On the other hand, the voltage of SS pin increases to about 2.8 V and keep the voltage. The calculation of Soft Start Time is as follows.

$$Soft\ Start\ Time(\sec) = \frac{0.6}{2\mu} \times Css$$

C_{SS} : External capacitor value of SS pin
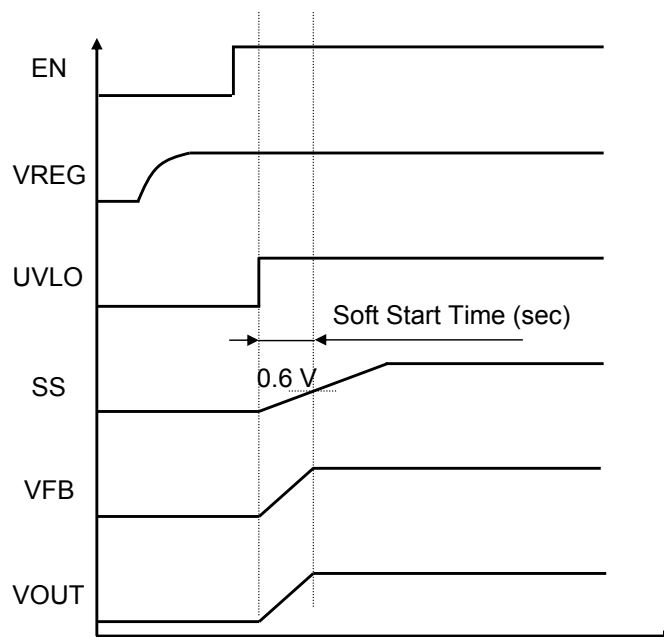
Figure : Soft Start Operation

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OPERATION (Continued)

5. Start-up / Shut-down Settings

The Start-up / Shut-down is enabled by the EN pin.
The EN pin can be set by either applying voltage from
an external voltage source or through a resistor
connected to the AVIN pin.

Case 1: Setting up the EN pin using an external
　　　　voltage source. When an external voltage
　　　　source is used, the EN pin input voltage
　　　　(V_{ENH}, V_{ENL}) should satisfy the conditions as
　　　　defined in the electrical characteristics

Figure : Internal circuit with EN pin

R_{EN2} : 800 kΩ ± 50 %

Vd　: 5.7 V ± 0.3 V
Id　: more than 100 µA
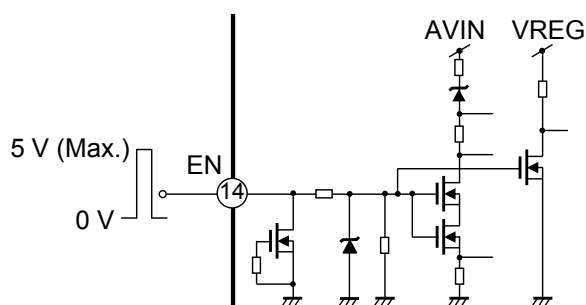
Figure : Internal circuit with EN pin

Case 2: Setting up the EN pin through a resistor
　　　　connected to AVIN pin. When setting up the
　　　　EN pin through a resistor connected to the
　　　　AVIN pin, refer to equations (1) and (2) to
　　　　calculate the optimal resistor settings.

[Equation]

$$(1) : \quad R_{EN1} > \frac{AV_{IN} - Vd}{Id}$$

$$(2) : \quad R_{EN1} < \frac{(AV_{IN} - V_{ENH}) \times R_{EN2}}{V_{ENH}}$$

[Example]

$$(1) : \quad R_{EN1} > \frac{12\,V - 6\,V}{100\,µA} = 60\,kΩ$$

$$(2) : \quad R_{EN1} < \frac{(12\,V - 5\,V) \times 400\,kΩ}{5\,V} = 560\,kΩ$$

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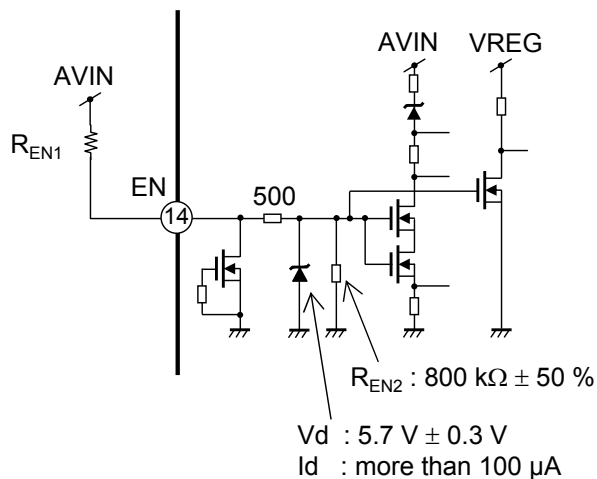
OPERATION (Continued)

6. Power ON / OFF sequence

(1) When the EN pin is set to High after the V_{IN}
and V_{REG} settle, the BGR starts up. (Recommended
V_{IN} rise time setting and V_{REG} rise time setting are
greater than or equal to 10 μs and less than or equal
to 1 s.)
(2) When the VREG pin exceeds its threshold value,
the UVLO is released and the SOFT START sequence
is enabled.
The capacitor connected to the SS pin begins to
charge and the SS pin voltage increases linearly.
(3) The VOUT pin (DC-DC Output) voltage increases at
the same rate as the SS pin.
Normal operation begins after the VOUT pin
reaches the set voltage.
(4) When the EN pin is set to Low, the BGR and UVLO
stop operation. The VOUT pin / SS pin Voltage starts
to drop and the VOUT pin discharge time depends on
the value of the Feedback resistors and the output load
current.

Note: The SS pin capacitor should be discharged
completely before restarting the startup
sequence.
An incomplete discharge process might result
in an overshoot of the output voltage.

greater than or equal to 10 μs and less than or equal to 1 s.

V_{IN} 90%

EN

greater than or equal to 10 μs and less than or equal to 1 s.

VREG   90%

UVLO

Soft Start Time (s) $= \dfrac{0.6}{2\,\mu} \times Css$

SS   0.6 V

VFB

VOUT

Delay Time (s) $= \dfrac{0.09}{2\,\mu} \times Css + 1\,m$

PGOOD

(1) (2) (3)   (4)
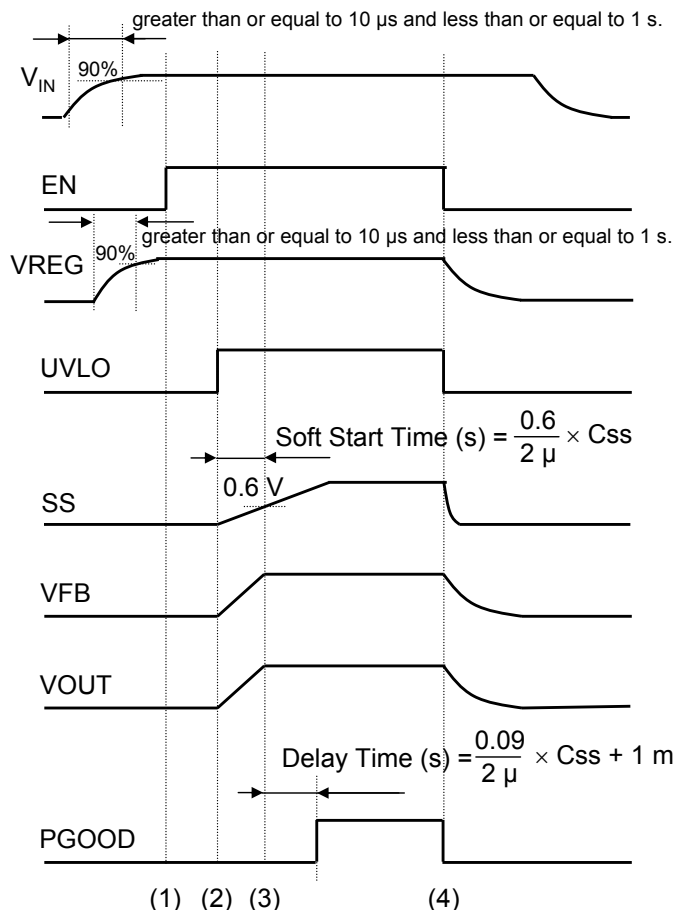
Figure : Power ON/OFF sequence

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OPERATION (Continued)

7. Inductor and Output Capacitor Setting
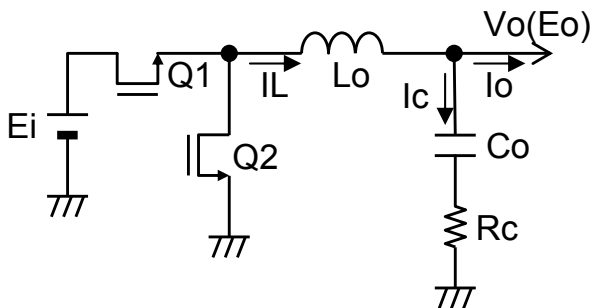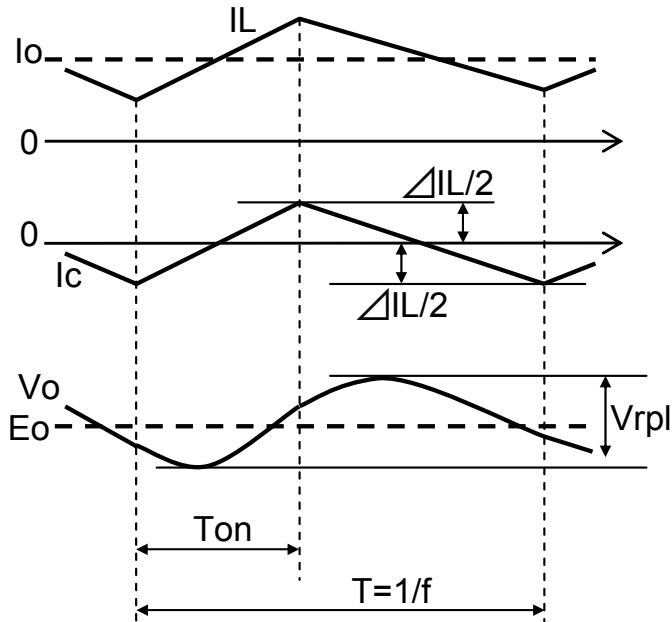
Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current.

$$\Delta IL = \frac{Eo \cdot (Ei - Eo)}{Ei \cdot Lo \cdot f}$$

$$Iox = \frac{\Delta IL}{2}$$

Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade off among component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 40 % of I_O (Max). The largest ripple current occurs at the Highest Ei. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$Lo \geq \frac{Eo \cdot (Ei - Eo)}{2Ei \cdot Iox \cdot f} \quad @ \, Ei = Ei\_max$$

And its maximum current rating is

$$IL\_max = Io\_max + \frac{\Delta IL}{2} \quad (@ \, Ei = Ei\_max)$$

The selection of C_O is primarily determined by the ESR (R_c) required to minimize voltage ripple and load transients. The output ripple V_{RPL} is approximately bounded by:

$$Vrpl = Vop - Vob = Ei \cdot \frac{Co \cdot Rc^2}{2Lo} + \frac{\Delta IL}{8Co \cdot f}$$

$$= Ei \cdot \frac{Co \cdot Rc^2}{2Lo} + \frac{Eo \cdot (Ei - Eo)}{8Ei \cdot Lo \cdot Co \cdot f^2}$$

From the above equation, to achieve desired output ripple, low ESR ceramic capacitors are recommended, and its required RMS current rating is:

$$Ic(\text{rms})\_max = \frac{\Delta IL}{2\sqrt{3}} \quad (@ \, Ei = Ei\_max)$$

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TYPICAL CHARACTERISTICS CURVES

1. Output Ripple Voltage

Condition : V_{IN} = 12 V, V_{REG}=5V, V_{OUT} Setting = 1.05 V, Switching Frequency = 410 kHz, Skip mode,
L_O = 1 µH, C_O = 110uF (22 µF x 5)

I_{OUT} = 0A

I_{OUT} = 1A

I_{OUT} = 4A

I_{OUT} = 8A

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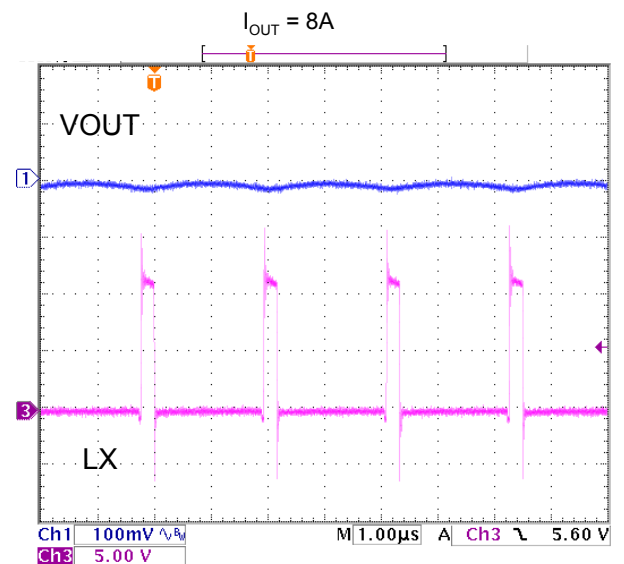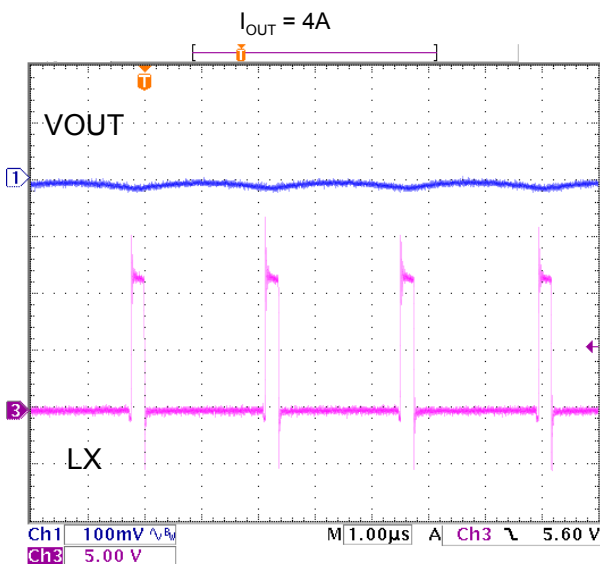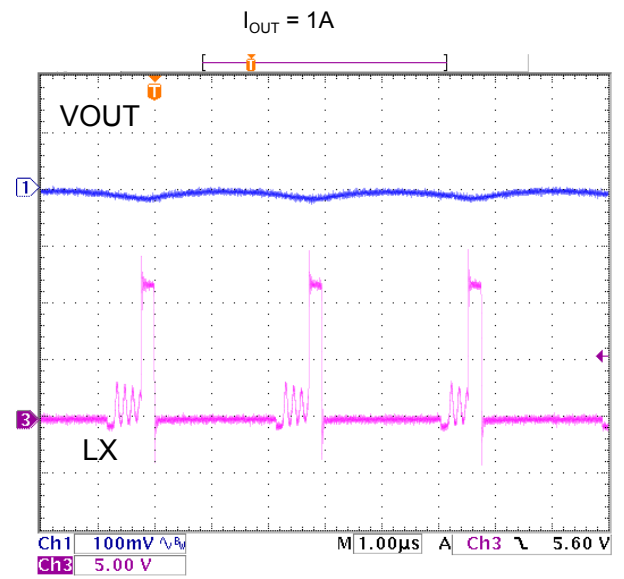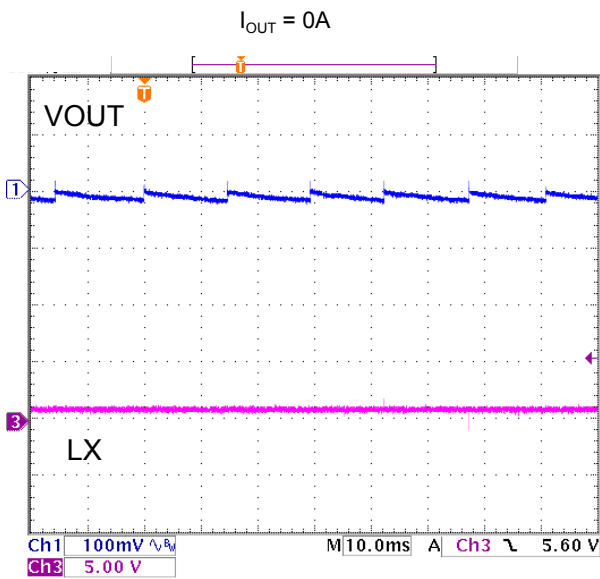
TYPICAL CHARACTERISTICS CURVES (Continued)

1. Output Ripple Voltage (Continued)

Condition : V_{IN} = 12 V, V_{REG}=5V, V_{OUT} Setting = 1.05 V, Switching Frequency = 410 kHz, FCCM,
L_O = 1 µH, C_O = 110uF (22 µF x 5)

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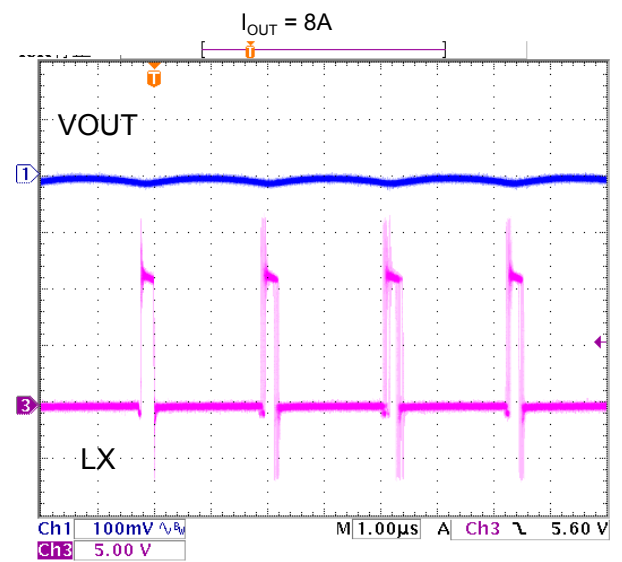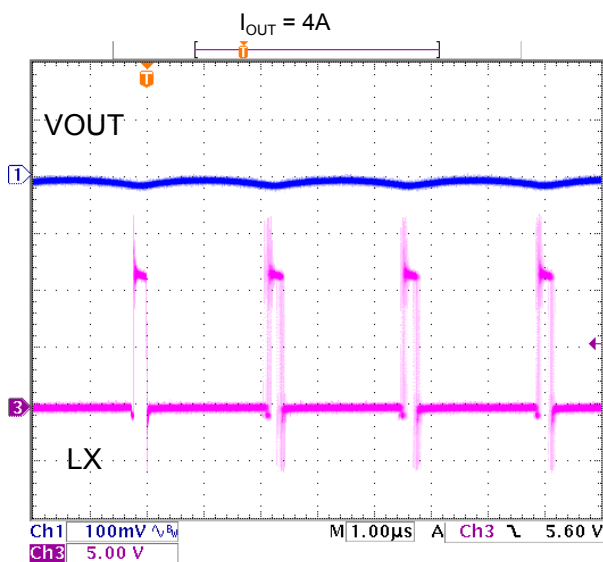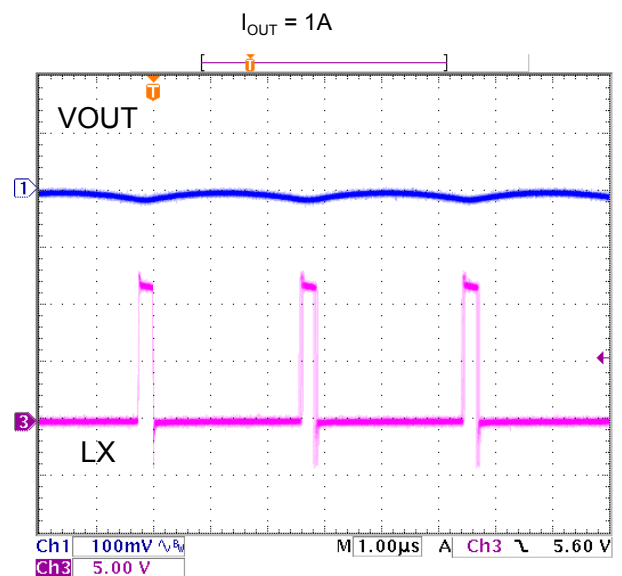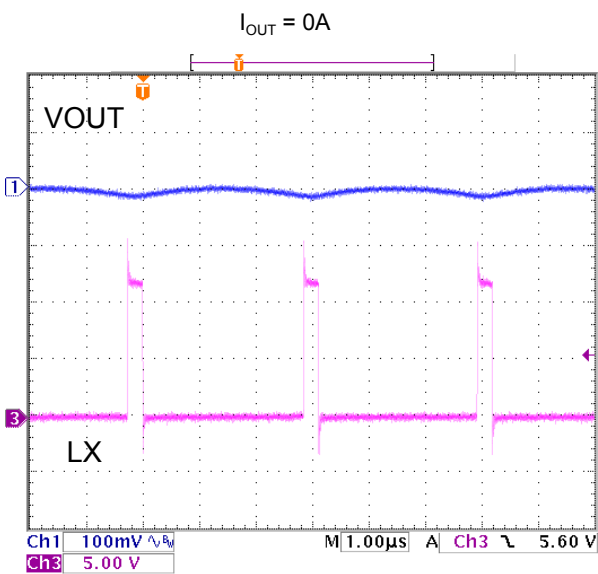
TYPICAL CHARACTERISTICS CURVES (Continued)

2. Load transient response

Condition : V_{IN} = 12 V, V_{REG} = 5V, V_{OUT} Setting = 1.05 V, Switching Frequency = 410 kHz,
I_{OUT} = 100 mA to 4 A (0.5 A / μs), L_O = 1 μH, C_O = 110uF (22 μF x 5)

Skip mode

VOUT (50 mV/div)   38.61mV

36.25mV

IOUT (2 A/div)

Time (100 us/div)

FCCM

VOUT (50 mV/div)   23.5mV

21.03mV

IOUT (2 A/div)

Time (100 us/div)
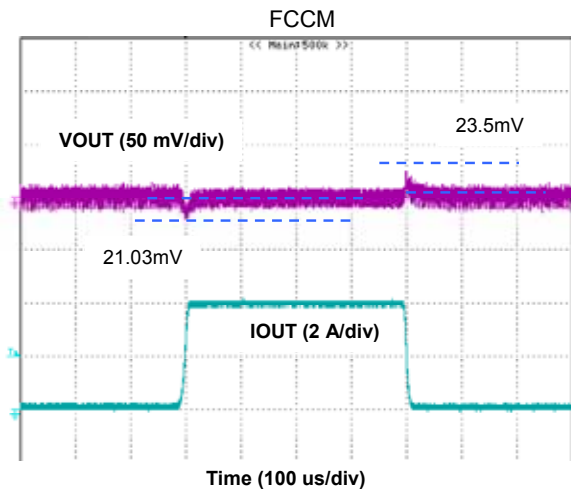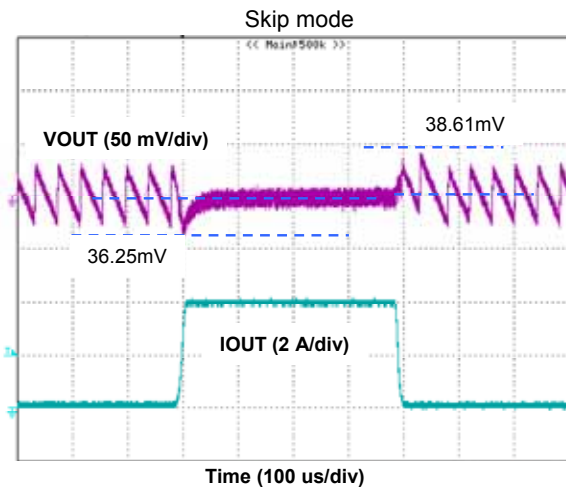
Condition : V_{IN} = 12 V, V_{REG} = 5V, V_{OUT} = 1.05 V, Switching Frequency = 410 kHz,
I_{OUT} = 2 A to 6 A (0.15 A / μs), L_O = 1 μH, C_O = 110uF (22 μF x 5)

Skip mode

VOUT (50 mV/div)   14.69mV

13.78mV

IOUT (2 A/div)

Time (100 us/div)

FCCM

VOUT (50 mV/div)   14.69mV

13.54mV

IOUT (2 A/div)

Time (100 us/div)

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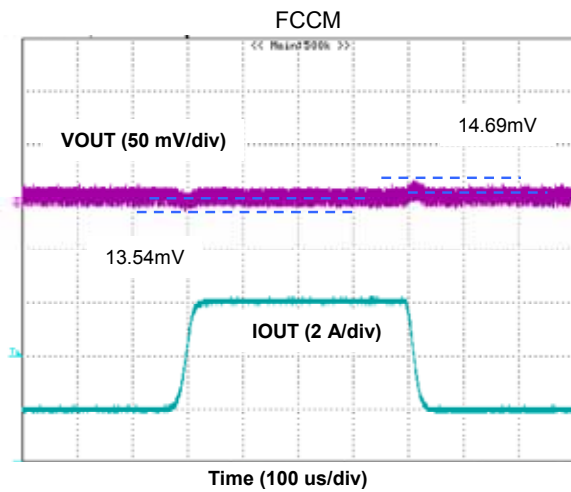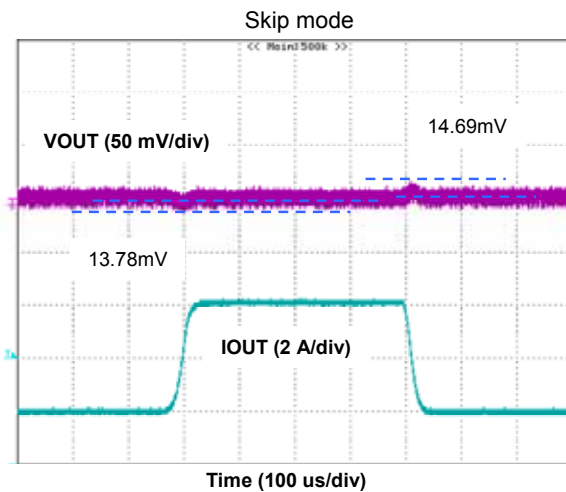
TYPICAL CHARACTERISTICS CURVES (Continued)

3. Efficiency

Condition : V_{IN} = 12 V, V_{REG} = 5V, V_{OUT} Setting = 1.05 V / 1.2 V / 1.8 V / 3.3 V,
Switching Frequency = 220 kHz, L_O = 3.3 µH, C_O = 110 µF (22 µF x 5)

Condition : V_{IN} = 12 V, V_{REG} = 5V, V_{OUT} Setting = 1.05 V / 1.2 V / 1.8 V / 3.3 V,
Switching Frequency = 410 kHz, L_O = 1 µH, C_O = 110 µF (22 µF x 5)

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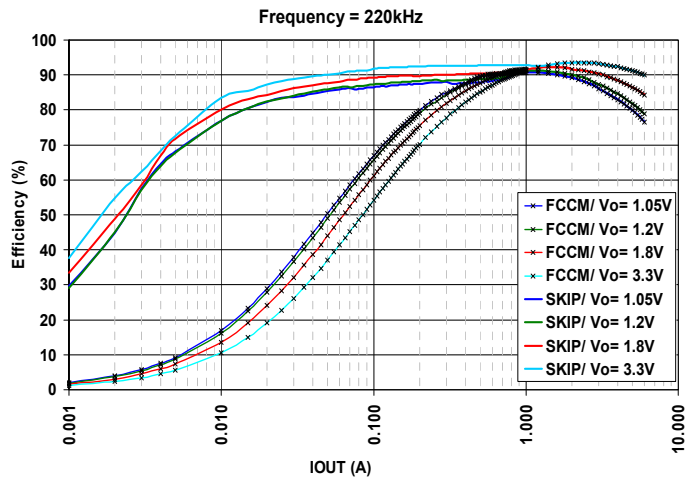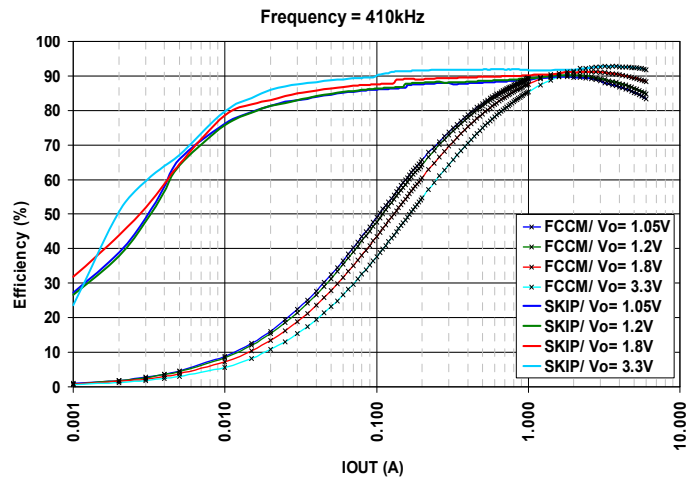
TYPICAL CHARACTERISTICS CURVES (Continued)

4. Load Regulation

Condition : V_{IN} = 12 V, V_{REG} = 5V, V_{OUT} Setting = 1.05 V, Switching Frequency = 220 kHz,
L_O = 3.3 µH, C_O = 110uF (22 µF x 5)
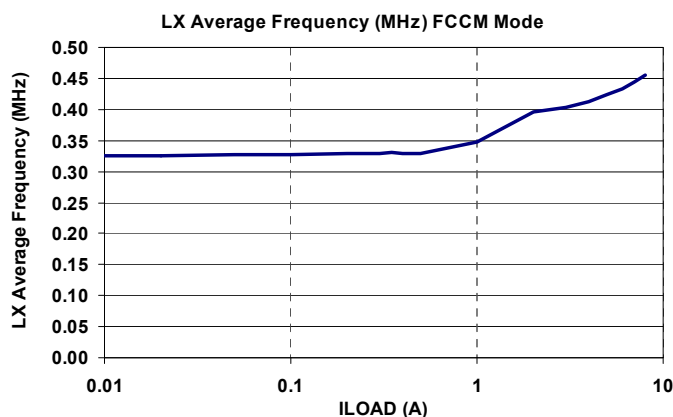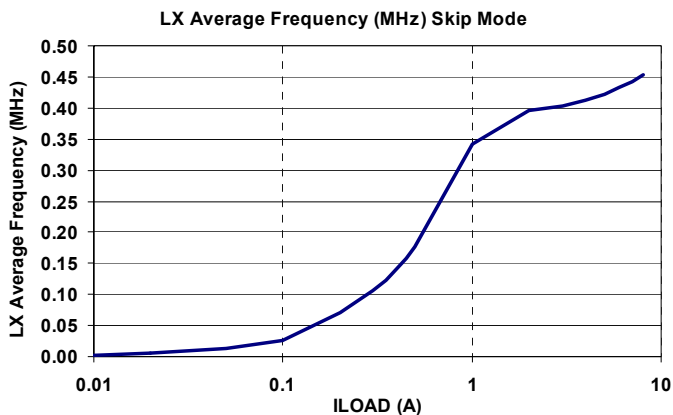

Condition : V_{IN} = 12 V, V_{REG} = 5V, V_{OUT} Setting = 1.05 V, Switching Frequency = 410 kHz,
L_O = 1 µH, C_O = 110 µF (22 µF x 5)

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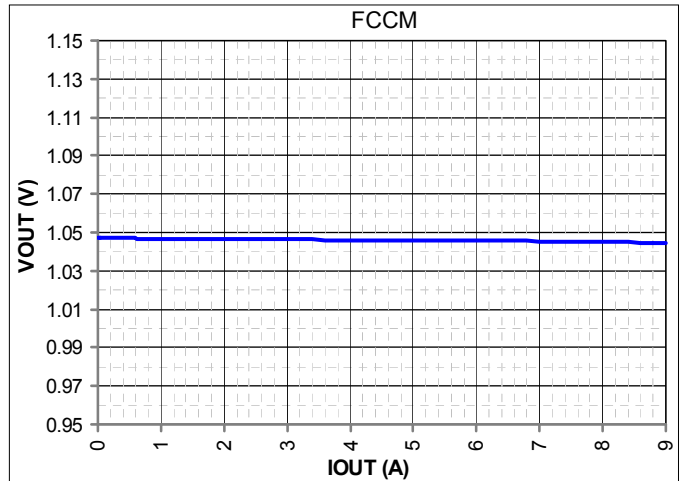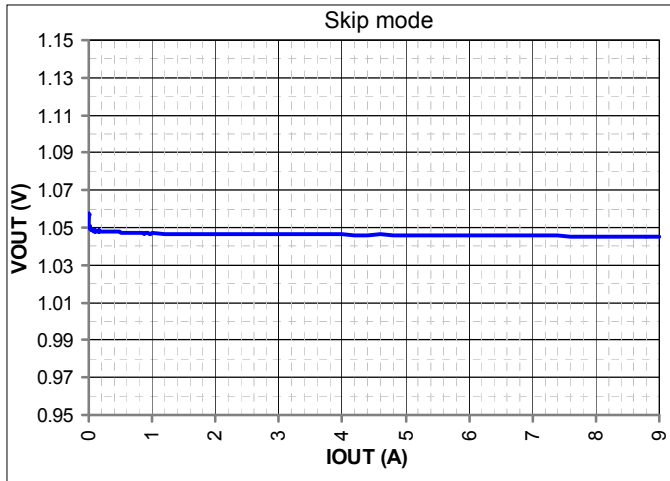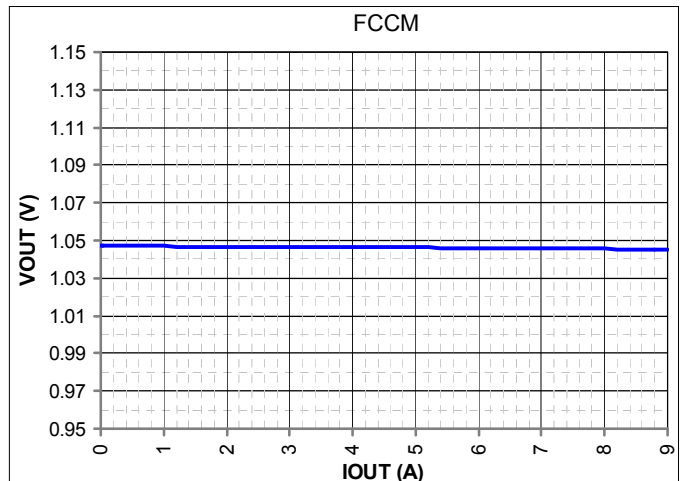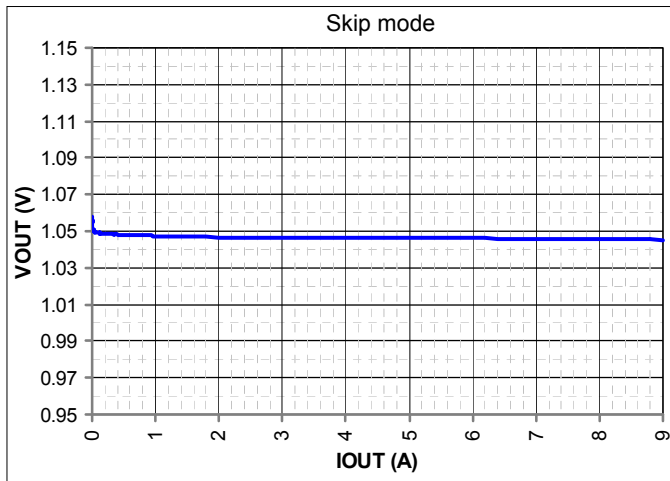
TYPICAL CHARACTERISTICS CURVES (Continued)

5. Line Regulation

Condition : V_{OUT} Setting = 1.05 V, Switching Frequency = 410 kHz, I_{OUT} = 1.5 A,
L_O = 1 µH, C_O = 110 µF (22 µF x 5)

Line Regulation_f = 410kHz (skip mode)

Line Regulation_f = 410kHz (FCCM mode)

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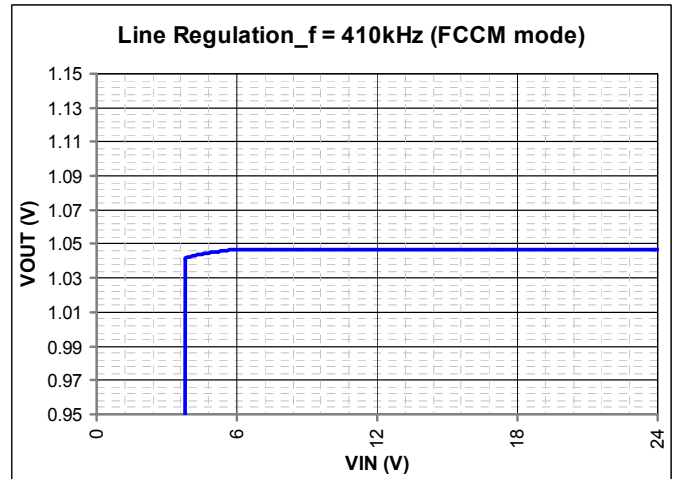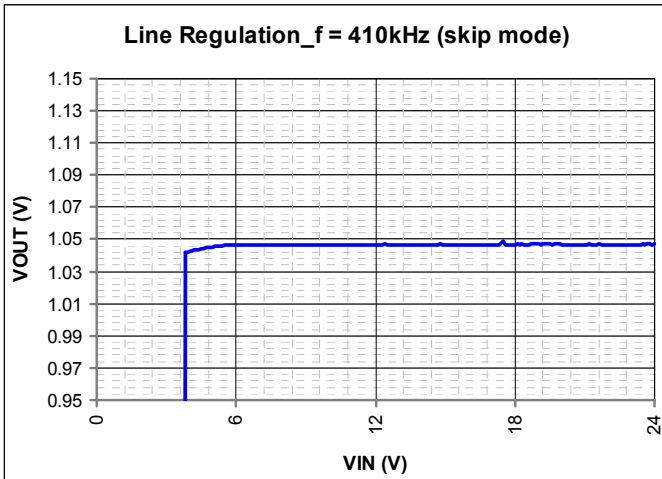
TYPICAL CHARACTERISTICS CURVES (Continued)

6. Start / Shut Down

Condition : V_{IN} = 12 V, V_{REG} = 5V, V_{OUT} Setting = 1.05 V, Switching Frequency = 410 kHz, Skip mode, I_{OUT} = 0 A, L_O = 1 µH, C_O = 110 µF (22 µF x 5)

EN (2 V/div)

SS (2 V/div)

VOUT (0.5 V/div)

Time (10 ms/div)

EN (2 V/div)

SS (2 V/div)

VOUT (0.5 V/div)

Time (10 ms/div)
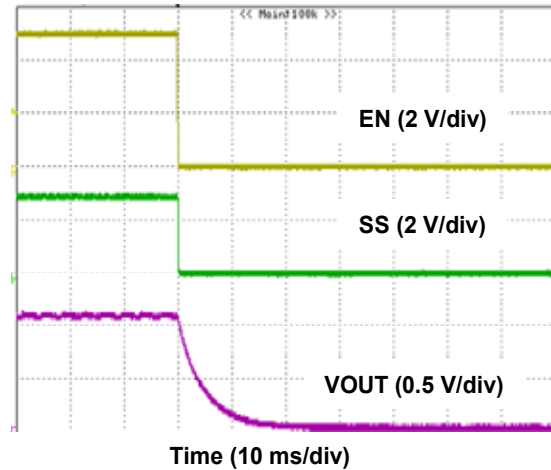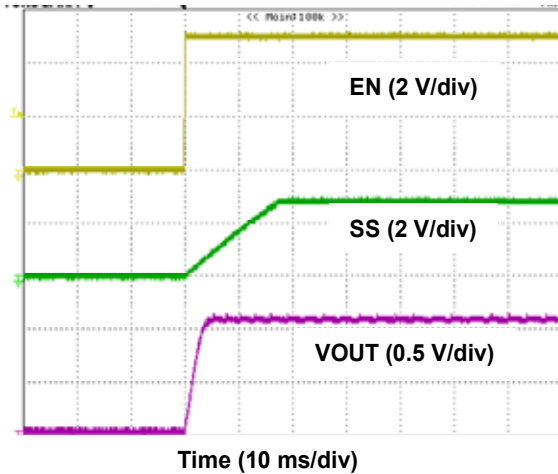
Condition : V_{IN} = 12 V, V_{REG} = 5V, V_{OUT} Setting = 1.05 V, Switching Frequency = 410 kHz, FCCM, I_{OUT} = 0 A, L_O = 1 µH, C_O = 110 µF (22 µF x 5)

EN (2 V/div)

SS (2 V/div)

VOUT (0.5 V/div)

Time (10 ms/div)

EN (2 V/div)

SS (2 V/div)

VOUT (0.5 V/div)

Time (10 ms/div)

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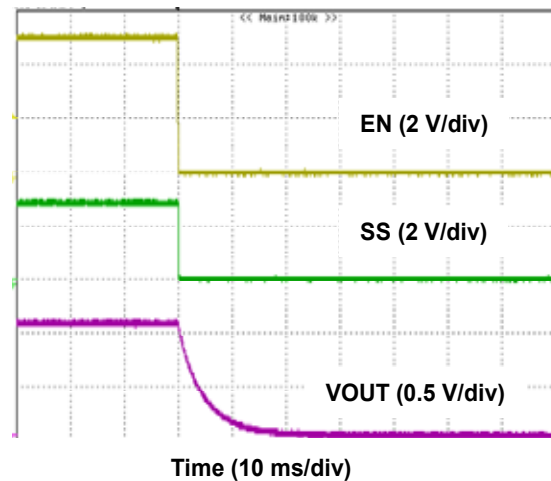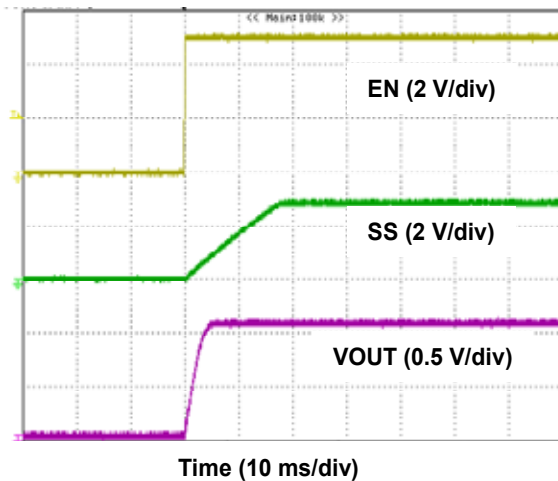
TYPICAL CHARACTERISTICS CURVES (Continued)

6. Start / Shut Down (Continued)

Condition : V_{IN} = 12 V, V_{REG} = 5V, V_{OUT} Setting = 1.05 V, Switching Frequency = 410 kHz, Skip mode, R_{LOAD} = 0.5 Ω, L_O = 1 µH, C_O = 44 µF (22 µF x 2)
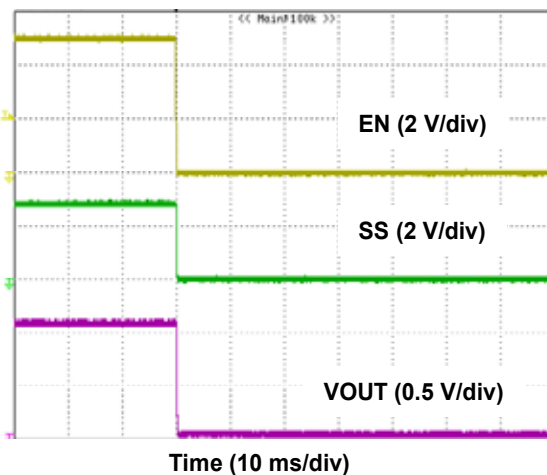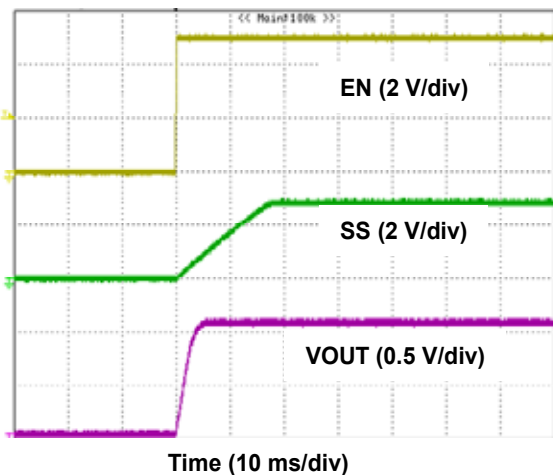
Condition : V_{IN} = 12 V, V_{REG} = 5V, V_{OUT} Setting = 1.05 V, Switching Frequency = 410 kHz, FCCM, R_{LOAD} = 0.5 Ω, L_O = 1 µH, C_O = 110 µF (22 µF x 5)

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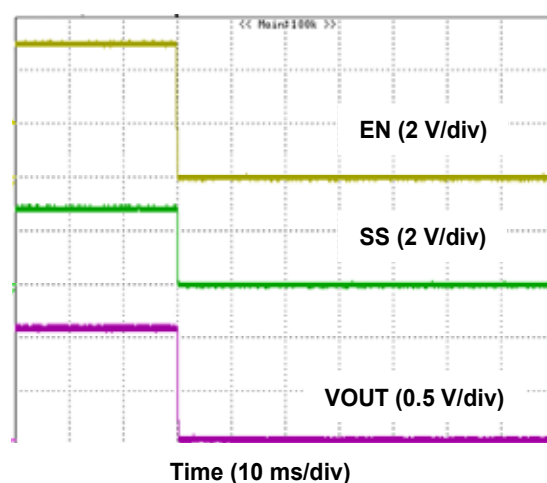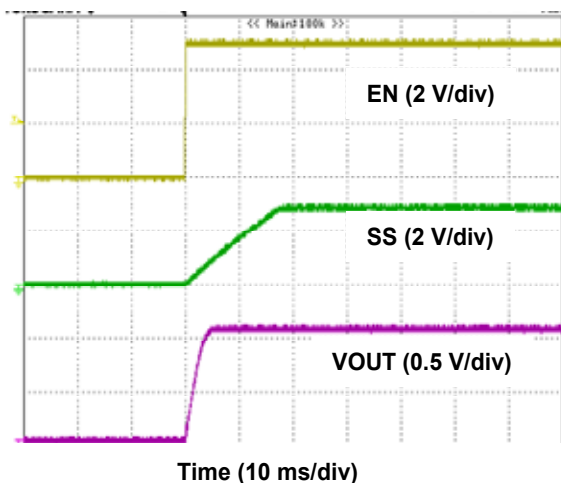
TYPICAL CHARACTERISTICS CURVES (Continued)

7. Short Circuit Protection

Condition : V_{IN} = 12 V, V_{REG} = 5V, V_{OUT} Setting = 1.05 V, Switching Frequency = 410 kHz,
   L_O = 1 μH, C_O = 110 μF (22 μF x 5)

Skip mode

LX (10 V/div)

SS (2 V/div)

VOUT (1 V/div)

IOUT (10 A/div)

Time (10 ms/div)

FCCM

LX (10 V/div)

SS (2 V/div)

VOUT (1 V/div)

IOUT (10 A/div)

Time (10 ms/div)

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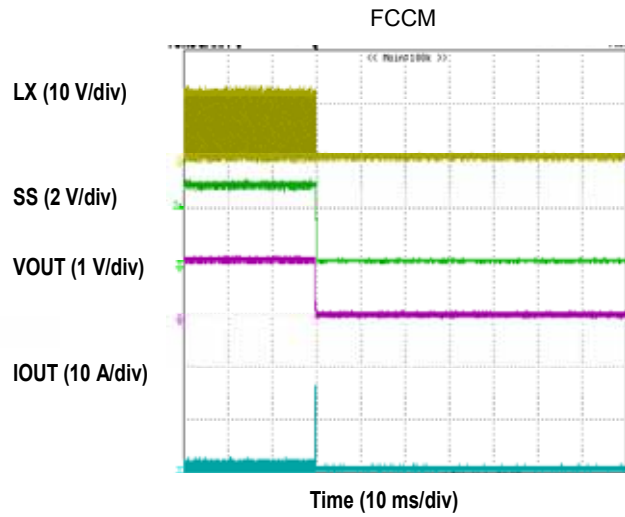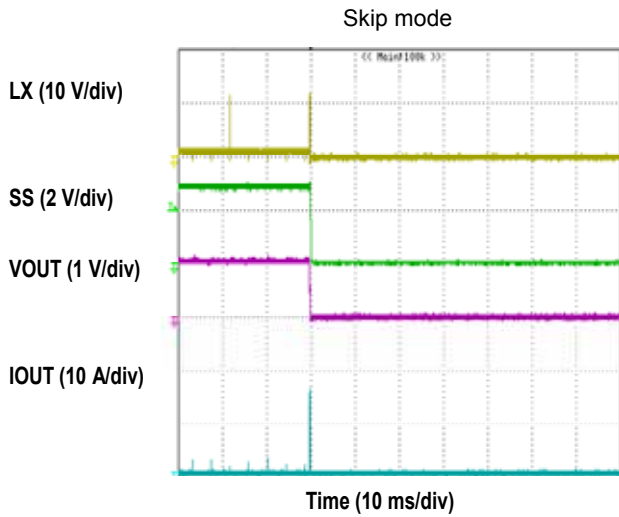
TYPICAL CHARACTERISTICS CURVES (Continued)

8. Switching Frequency

Condition : V_{IN} = 12 V, V_{REG} = 5V, V_{OUT} Setting = 1.05 V, Switching Frequency = 410 kHz, I_{OUT} = 10 mA to 8 A,
L_O = 1 µH, C_O = 110 µF (22 µF x 5)

Condition : V_{OUT} Setting = 1.05 V, Switching Frequency = 410 kHz, I_{OUT} = 4 A, L_O = 1 µH, C_O = 110 µF (22 µF x 5)

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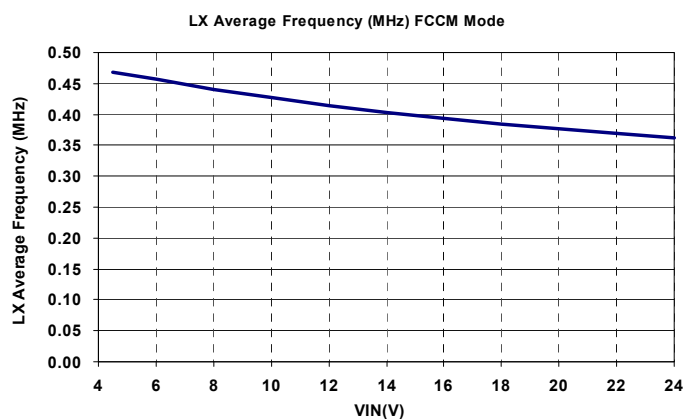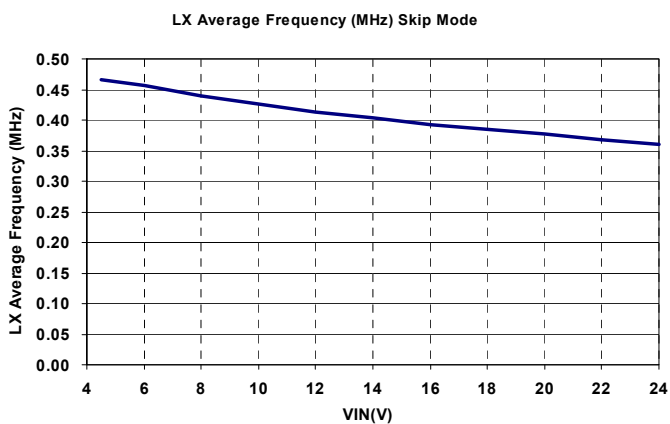
TYPICAL CHARACTERISTICS CURVES (Continued)

9. Thermal Performance

Condition : V_{IN} = 12 V, V_{REG} = 5V, V_{OUT} Setting = 1.05 V, Switching Frequency = 410 kHz, Skip mode, I_{OUT} = 8 A,
L_O = 1 µH, C_O = 110 µF (22 µF x 5)

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APPLICATIONS INFORMATION

1. Evaluation Board Information

Condition : V_{OUT} Setting = 1.05 V, Switching Frequency = 410 kHz, Skip mode

Application circuit

Layout

Figure : Top Layer with silk screen
(Top View) with Evaluation board

Figure : Bottom Layer with silk screen
(Bottom View) with Evaluation board
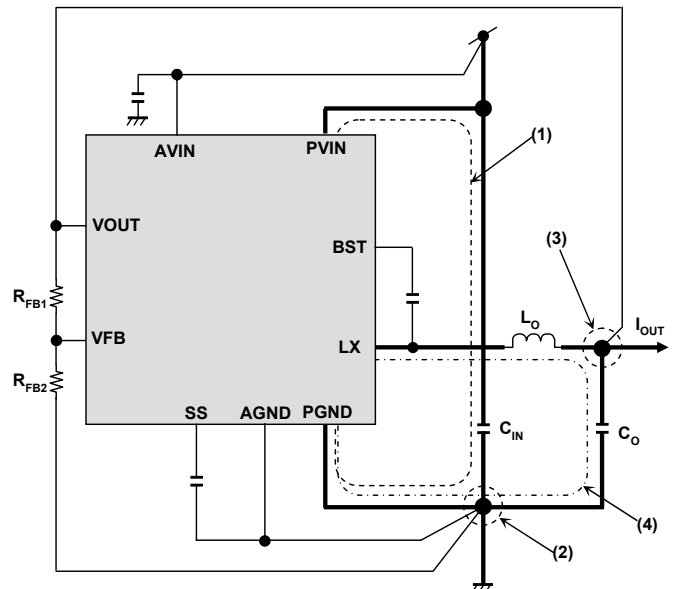
Notes: The application circuit diagram and layout diagram explained in this section, should be used as reference examples. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit and the information attached with it, in the design of the equipment.

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APPLICATIONS INFORMATION (Continued)

2. Layout Recommendations

Board layout considerations are necessary for stable operation of the DC-DC regulator. The following precautions must be used when designing the board layout.

(a) The Input capacitor C_{IN} must be placed in such a way that the distance between PVIN and PGND is minimum, in order to suppress the switching noise. Stray inductance and impedance should be reduced as indicated by loop (1) in the figure below.

(b) A single point ground connection (2) must be used to connect PGND and AGND to improve operation stability.

(c) Output current line I_{OUT} and the output sense line VOUT must have small common impedance to reduce output load variations. Output sense line VOUT must be close to the output condenser C_O as indicated by (3) below.

(d) Power Loss and output ripple voltage can be reduced by placing the inductor L_O and output capacitor C_O such that the stray inductance and the impedance of loop (4) is minimum. This is realized by :
   i) Minimizing distance between inductor L_O and LX pin.
   ii) Reducing distance between output capacitor C_O and (2) / (3)

(e) Thick lines in the application circuit example represent lines with large current flow. These lines should be designed as thick as possible.

(f) VFB / SS lines should be placed far away from LX line, BST line and inductor L_O to reduce the effects of switching noise. These lines should be designed as short as possible. This is especially true for the VFB line, which is a high impedance line.

(g) R_{FB1} / R_{FB2} should also be placed as far away as possible from LX line, BST line and inductor L_O to minimize the effects of switching noise. R_{FB1} / R_{FB2} should be placed close to the VFB pin.

(h) LX / BST lines are noisy lines. They should be designed as short as possible.

Figure : Application circuit diagram

Note : The application circuit diagram and layout diagram explained in this section, should be used as reference examples. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit and the information attached with it, in the design of the equipment.

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APPLICATIONS INFORMATION (Continued)

3. Recommended component

Reference Designator	QTY	Value	Manufacturer	Part Number	Note
C-AVIN1	1	4.7 µF	Murata	GRM31CB31H475KA12L	—
C-AVIN2	1	0.1 µF	Murata	GRM188R72A104KA35L	Optional
C-BST	1	0.1 µF	Murata	GRM188R72A104KA35L	—
C-DCDCOUT	5	22 µF	Murata	GRM32ER71E226KE15L	—
C-PVIN5	2	10 µF	TAIYO YUDEN	UMK325AB7106MM-T	—
C-PVIN6	1	0.1 µF	Murata	GRM188R72A104KA35L	—
C-SS	1	10 nF	Murata	GRM188R72A103KA01L	—
C-VREG	1	1.0 µF	Murata	GRM188R71E105KA12L	—
L-LX	1	1.0 µH	Panasonic	ETQP3W1R0WFN	FSEL GND (410 kHz) OPEN (580 kHz)
		3.3 µH	Panasonic	ETQP3W3R3WFN	FSEL VREG (220 kHz)
C-FB	1	12 nF	YAGEO (PHYCOMP)	CC0603KRX7R9BB123	—
R-FB1	1	750	Panasonic	ERJ3GEYJ561Y	—
R-FB2	1	0	Panasonic	ERJ3GEY0R00V	—
R-RB3	1	0	Panasonic	ERJ3GEYJ510V	—
R-FB4	1	1 kΩ	Panasonic	ERJ3GEYJ681V	—
R-PG	1	100 kΩ	Panasonic	ERJ3EKF1003V	—

Special attention and precaution in using

This IC is intended to be used for general electronic equipment. Ensure that the IC is used within the recommended safe operating region illustrated by the reference graph below. Do take note that thermal performance may varies with PCB design and PCB materials. You are encourage to use the graph only as a reference for your design and discuss further with our application engineer.

It is to be understood that our company shall not be held responsible for any damage incurred as a result of application beyond the recommended safe operating region.

VIN (V) V.S. ILOAD (A)
PKG Surface Temperature=80deg, Fsw=410kHz

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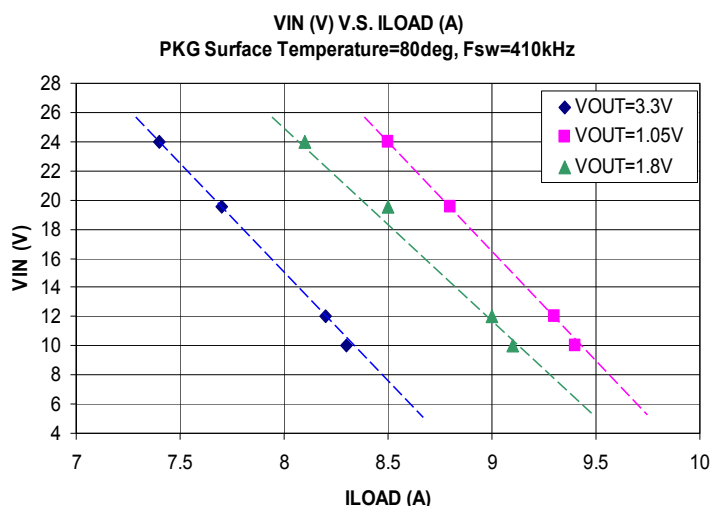
PACKAGE INFORMATION

Outline Drawing

Package Code: HQFN024-A3-0404BZF

Unit : mm

Detail *A (Reference)
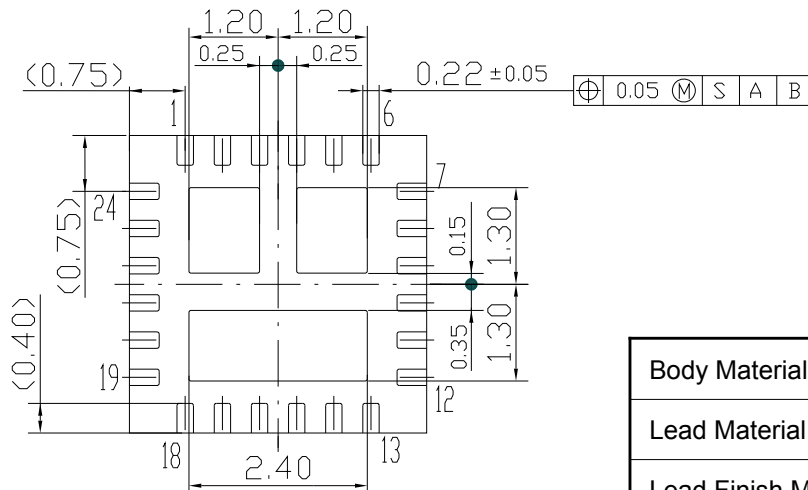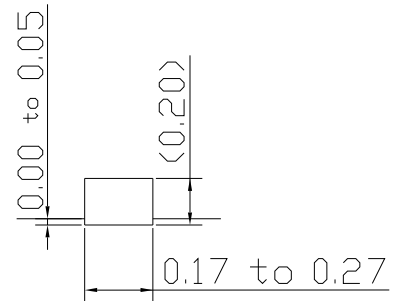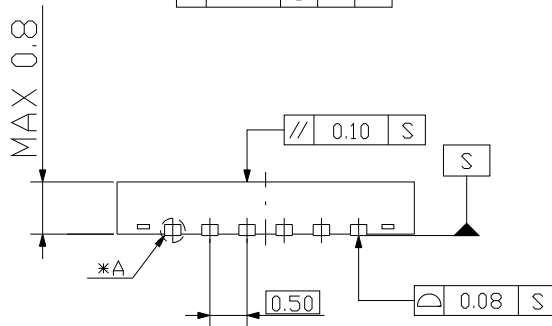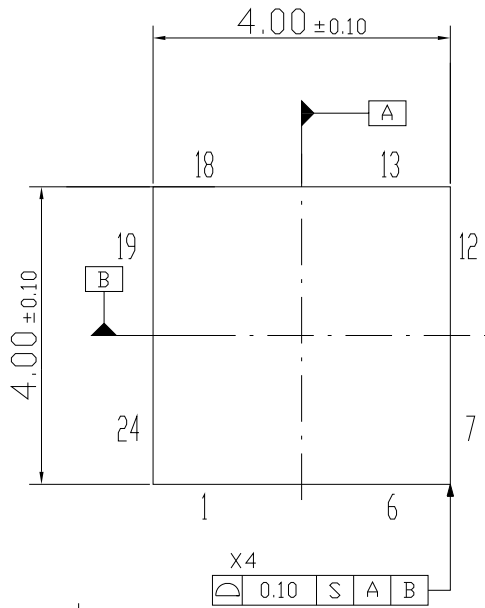
| Body Material : Br/Sb Free Epoxy Resin |
| Lead Material : Cu Alloy |
| Lead Finish Method : Pd Plating |

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IMPORTANT NOTICE

1. When using the IC for new models, verify the safety including the long-term reliability for each product.

2. When the application system is designed by using this IC, please confirm the notes in this book.
    Please read the notes to descriptions and the usage notes in the book.

3. This IC is intended to be used for general electronic equipment.
    Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body. Any applications other than the standard applications intended.
    (1) Space appliance (such as artificial satellite, and rocket)
    (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
    (3) Medical equipment for life support
    (4) Submarine transponder
    (5) Control equipment for power plant
    (6) Disaster prevention and security device
    (7) Weapon
    (8) Others : Applications of which reliability equivalent to (1) to (7) is required
    Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
    However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.

4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
    Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.

5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.

6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might be damaged.

7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.

9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.

10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.

11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the IC might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

12. Product which has specified ASO (Area of Safe Operation) should be operated in ASO

13. Verify the risks which might be caused by the malfunctions of external components.

14. Connect the metallic plates (fins) on the back side of the LSI with their respective potentials (AGND, PVIN, LX). The thermal resistance and the electrical characteristics are guaranteed only when the metallic plates (fins) are connected with their respective potentials.