

Features

- Single-Supply Operation (+2V to +6V)
- Rail-to-Rail Analog Signal Dynamic Range
- Low On-Resistance (6 Ω typ. with 5V supply)
Minimizes Distortion and Error Voltages
- On-Resistance Flatness, 3 Ω typ.
- Low Charge Injection Reduces Glitch Errors. Q = 4pC typ.
- High Speed. t_{ON} = 10ns typ.
- Wide -3dB Bandwidth: 326 MHz (typ.)
- High-Current Channel Capability: >100mA
- TTL/CMOS Logic Compatible
- Low Power Consumption (0.5 μ W typ)
- Small outline transistor package minimizes board area
- Packaging (Pb-free & Green available):
 - 5-pin 65-mil wide SOT23 (T) for PI5A121 and PI5A122
 - 6-pin 65-mil wide SOT23 (T) for PI5A124
 - 5-pin 50-mil wide SC70 (C) for PI5A121/PI5A122

Applications

- Audio, Video Switching, and Routing
- Battery-Powered Communication Systems
- Computer Peripherals
- Telecommunications
- Portable Instrumentation
- Mechanical Relay Replacement
- Cell Phones
- PDAs

Description

The PI5A121/PI5A122/PI5A124 are analog switches designed for single-supply operation. These high-precision devices are ideal for low-distortion audio, video, signal switching and routing.

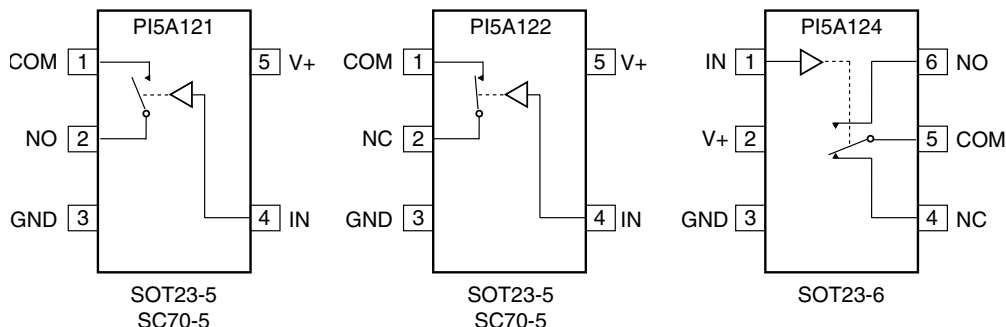
The PI5A121 is a single-pole throw (SPST) normally open (NO) switch. The switch is open when IN is LOW. The PI5A122 is a single-pole single-throw (SPST) normally closed (NC) switch.

Each switch conducts current equally well in either direction when on. When off, they block voltages up to V+.

These switches are fully specified with +5V, and +3.3V supplies. With +5V, they guarantee <10 Ω On-Resistance. On-Resistance matching between channels is within 2 Ω . On-Resistance flatness is less than 55 Ω over the specified range. These switches also guarantee fast switching speeds (t_{ON} <20ns).

These products are available in 5-pin SC70 and/or 6-pin SOT23 plastic packages for operation over the industrial (-40°C to +85°C) temperature range.

Functional Diagrams, Pin Configurations and Truth Tables



Switches shown for Logic "0" input

IN	PI5A121	PI5A122
0	OFF	ON
1	ON	OFF

LOGIC	PI5A124	
	NC	NO
0	ON	OFF
1	OFF	ON

Absolute Maximum Ratings

Voltages Referenced to Gnd

V+ -0.5V to +7V

V_{IN}, V_{COM}, V_{NC}, V_{NO} (Note 1) -0.5V to V_{CC} +2V
or 30mA, whichever occurs first

Current (any terminal) ±25mA

Peak Current, COM, NO, NC

(Pulsed at 1ms, 10% duty cycle) ±25mA

Thermal Information

Continuous Power Dissipation

SOT23-6 (derate 7mW/°C above +70°C) 550mW

Storage Temperature -65°C to +150°C

Lead Temperature (soldering, 10s) +300°C

Note 1:

Signals on NC, NO, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to 30mA.

Caution: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Electrical Specifications - Single +5V Supply

(V+ = +5V ± 10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp.(°C)	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Analog Switch							
Analog Signal Range ⁽³⁾	V _{ANALOG}		Full	0		V+	V
On-Resistance	R _{ON}	V+ = 4.5V, I _{COM} = -30mA, V _{NO} or V _{NC} = +2.5V	25		7.2	10	Ω
			Full			12	
On-Resistance Match Between Channels ⁽⁴⁾	ΔR _{ON}		25		0.2	2	
			Full			4	
On-Resistance Flatness ⁽⁵⁾	R _{FLAT(ON)}	V+ = 5V, I _{COM} = -30mA, V _{NO} or V _{NC} = 1V, 2.5V, 4V	25		2.72	3.5	
			Full			4	
NO or NC Off Leakage Current ⁽⁶⁾	I _{NO(OFF)} or I _{NC(OFF)}	V+ = 5.5V, V _{COM} = 0V, V _{NO} or V _{NC} = 4.5V	25		0.18		nA
			Full	-80		80	
COM Off Leakage Current ⁽⁶⁾	I _{COM(OFF)}	V+ = 5.5V, V _{COM} = +4.5V, V _{NO} or V _{NC} = ±0V	25		0.20		
			Full	-80		80	
COM On Leakage Current ⁽⁶⁾	I _{COM(ON)}	V+ = 5.5V, V _{COM} = +4.5V V _{NO} or V _{NC} = +4.5V	25		0.20		
			Full	-80		80	

Electrical Specifications - Single +5V Supply (continued)

(V+ = + 5V ± 10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp(°C)	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Logic Input							
Input High Voltage	V _{IH}	Guaranteed logic High Level	Full	2			V
Input Low Voltage	V _{IL}	Guaranteed logic Low Level				0.8	
Input Current with Voltage High	I _{INH}	V _{IN} = 2.4V, all others = 0.8V		-1	0.005	1	μA
Input Current with Voltage Low	I _{INL}	V _{IN} = 0.8V, all others = 2.4V		-1	0.005	1	
Dynamic							
Turn-On Time	t _{ON}	V _{CC} = 5V, Figure 1	25		7	15	ns
			Full			20	
Turn-Off Time	t _{OFF}		25		1	7	
			Full			10	
Charge Injection ⁽³⁾	Q	C _L = 1nF, V _{GEN} = 0V, R _{GEN} = 0Ω, Figure 2	25		1.6	10	pC
Off Isolation	O _{IRR}	R _L = 50Ω, C _L = 5pF, f = 10MHz, Figure 3			-43		dB
Crosstalk ⁽⁸⁾	X _{TALK}	R _L = 50Ω, C _L = 5pF, f = 10MHz, Figure 4			-43		
NC or NO Capacitance	C _(OFF)	f = 1kHz, Figure 5			5.5		pF
COM Off Capacitance	C _{COM(OFF)}				5.5		
COM On Capacitance	C _{COM(ON)}			f = 1kHz, Figure 6		13	
-3dB Bandwidth	BW	R _L = 50Ω, Figure 7	Full		326		MHz
Supply							
Power-Supply Range	V+		Full	2		6	V
Positve Supply Current	I+	V _{CC} = 5.5V, V _{IN} = 0V or V+				1	μA

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. ΔR_{ON} = R_{ON} max - R_{ON} min
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
7. Off Isolation = 20log₁₀ [V_{COM} / (V_{NO} or V_{NC})]. See Figure 3.
8. Between any two switches. See Figure 4.

Electrical Specifications - Single +3.3V Supply

(V+ = +3.3V ± 10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp.(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
Analog Signal Range ⁽³⁾	V _{ANALOG}			0		V+	V
On-Resistance	R _{ON}	V+ = 3V, I _{COM} = -30mA, V _{NO} or V _{NC} = 1.5V	25		12	18	Ω
			Full			22	
On-Resistance Match Between Channels ⁽⁴⁾	ΔR _{ON}	V+ = 3.3V, I _{COM} = -30mA, V _{NO} or V _{NC} = 0.8V, 2.5V	25		1	1	
			Full			2	
On-Resistance Flatness ^(3,5)	R _{FLAT(ON)}		25		0.5	4	
			Full			5	
Dynamic							
Turn-On Time	t _{ON}	V+ = 3.3V, V _{NO} or V _{NC} = 1.5V, Figure 1	25		15	25	ns
			Full			40	
Turn-Off Time	t _{OFF}		25		1.5	12	
			Full			20	
Charge Injection ⁽³⁾	Q	C _L = 1nF, V _{GEN} = 0V, R _{GEN} = 0V, Figure 2	25		1.3	10	pC
Supply							
Positive Supply Current	I+	V+ = 3.6V, V _{IN} = 0V or V+ All Channels on or off	Full			1	μA
Logic Input							
Input High Voltage	V _{IH}	Guaranteed logic high level	Full	2			V
Input Low Voltage	V _{IL}	Guaranteed logic low level	Full			0.8	
Input High Current	I _{INH}	V _{IN} = 2.4V, all others = 0.8V	Full	-1		1	μA
Input Low Current	I _{INL}	V _{IN} = 0.8V, all others = 2.4V	Full	-1		1	

The circuit diagram shows a logic switch component with a +5V supply connected to the V+ pin. The COM pin is connected to the output V_{OUT}, which is loaded with a 100ohm resistor R_L and a 15pF capacitor C_L to ground. The NO or NC pin is connected to a +3V* supply. The IN pin is connected to a logic input through an inverter. The logic input is also connected to ground through a switch symbol.

The timing diagram shows the Logic Input (inverted) and Switch Output waveforms. The Logic Input transitions from 0V to +3V and back to 0V. The Switch Output transitions from 0V to V_{OUT} (90% level) and back to 0V. Key timing parameters are indicated: t_r < 20ns, t_f < 20ns, t_{OFF}, t_{ON}, and 50% and 90% voltage levels.

CL INCLUDES FIXTURE AND STRAY CAPACITANCE

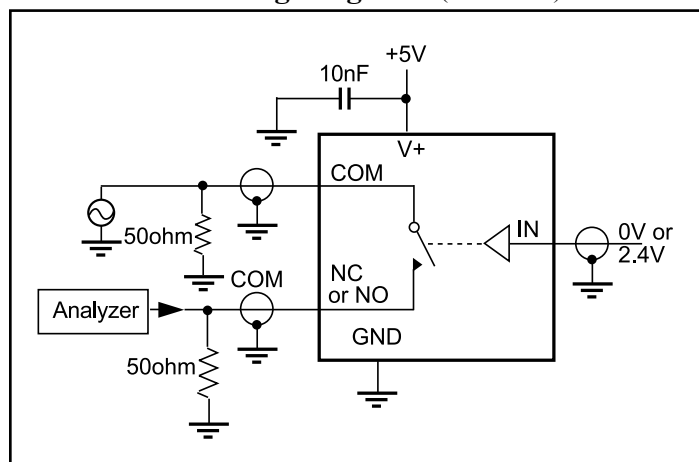
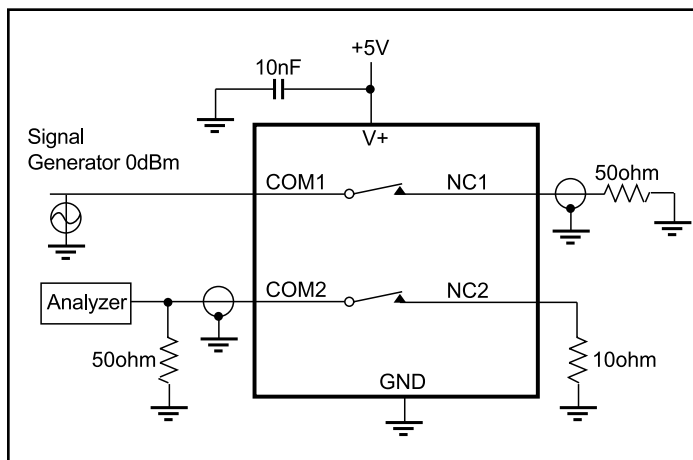
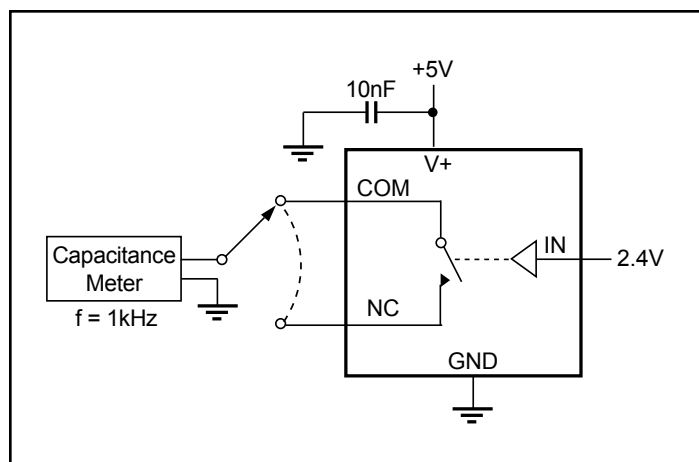
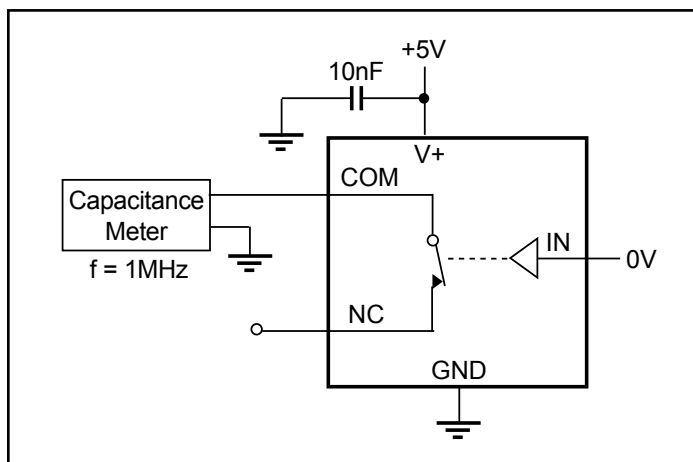
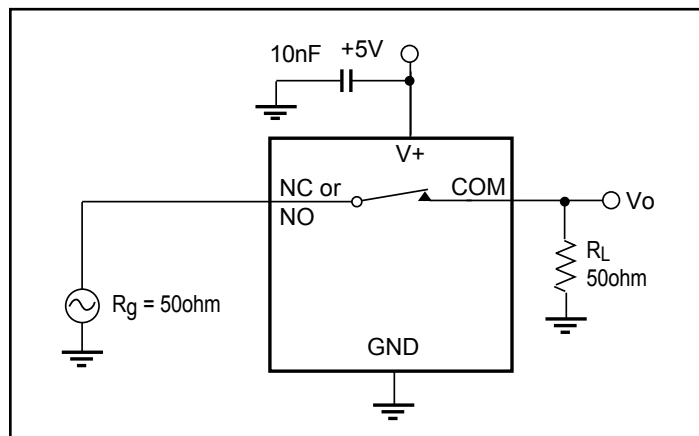
$$V_{OUT} = V_{NO} \left(\frac{R_L}{R_L + R_{ON}} \right)$$

LOGIC INPUT WAVEFORMS INVERTED FOR SWITCHES THAT HAVE OPPOSITE LOGIC
* 1.5V FOR 3.3V SUPPLY

The circuit diagram shows a DAC0808 configured as a 1-bit D/A converter. The V_{CC} pin is connected to +5V, and the V_{EE} pin is connected to GND. The COM pin is connected to a voltage divider consisting of V_{GEN} and a $0.1\mu F$ capacitor. The IN pin is connected to a logic input. The NO or NC pin is connected to the output V_{OUT} , which is also connected to a load capacitor C_L (1nF). The timing diagram shows the output voltage V_{OUT} and the input signal IN . The output voltage is high when IN is ON and low when IN is OFF. The output voltage change is labeled DV_{OUT} .

$Q = (DV_{OUT})(C_L)$

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Test Circuits/Timing Diagrams (continued)

Figure 3. Off Isolation

Figure 4. Crosstalk (124 only)

Figure 5. Channel-Off Capacitance

Figure 6. Channel-On Capacitance

Figure 7. Bandwidth

Technical drawing of a rectangular component with four mounting tabs. The drawing includes top, side, and end views with various dimensions in inches and millimeters. Key dimensions include a top width of 1.90 inches (48.26 mm) BSC, a top length of 2.60 inches (66.04 mm) BSC, and a bottom width of 1.75 inches (44.28 mm) BSC. A side view shows a height of 1.50 inches (38.10 mm) BSC. An end view shows a width of 0.35 inches (8.89 mm) BSC. A detail view of a mounting tab shows a width of 0.10 inches (2.54 mm) BSC and a height of 0.04 inches (1.02 mm) BSC. A note indicates that dimensions in boxes are in millimeters.

Technical drawing of a component with dimensions and views.

Top View:

- Overall width: $.079 \begin{matrix} 2.00 \\ \text{BSC} \end{matrix}$
- Distance from center to feature 5: $.051 \begin{matrix} 1.30 \\ \text{BSC} \end{matrix}$
- Distance from center to feature 4: $.051 \begin{matrix} 1.30 \\ \text{BSC} \end{matrix}$
- Feature 5 height: $.049 \begin{matrix} 1.25 \\ \text{BSC} \end{matrix}$
- Feature 4 height: $.083 \begin{matrix} 2.10 \\ \text{BSC} \end{matrix}$
- Feature 1 width: $.026 \begin{matrix} 0.65 \\ \text{BSC} \end{matrix}$
- Feature 2 width: $.006 \begin{matrix} 0.11 \\ \text{BSC} \end{matrix}$
- Feature 3 width: $.006 \begin{matrix} 0.15 \\ \text{BSC} \end{matrix}$
- Feature 3 height: $.006 \begin{matrix} 0.15 \\ \text{BSC} \end{matrix}$

Bottom View:

- Overall width: $.079 \begin{matrix} 2.00 \\ \text{BSC} \end{matrix}$
- Feature 1 width: $.026 \begin{matrix} 0.65 \\ \text{BSC} \end{matrix}$
- Feature 2 width: $.006 \begin{matrix} 0.11 \\ \text{BSC} \end{matrix}$
- Feature 3 width: $.006 \begin{matrix} 0.15 \\ \text{BSC} \end{matrix}$
- Feature 3 height: $.006 \begin{matrix} 0.15 \\ \text{BSC} \end{matrix}$

Side View (Left):

- Overall height: 1.10 MAX
- Feature 1 height: $.004 \begin{matrix} 0 \\ \text{BSC} \end{matrix}$
- Feature 2 height: $.004 \begin{matrix} 0 \\ \text{BSC} \end{matrix}$
- Feature 3 height: $.004 \begin{matrix} 0 \\ \text{BSC} \end{matrix}$

Side View (Right):

- Overall height: $.321 \begin{matrix} 0.15 \\ \text{BSC} \end{matrix}$
- Feature 1 height: $.010 \begin{matrix} 0.18 \\ \text{BSC} \end{matrix}$
- Feature 2 height: $.010 \begin{matrix} 0.18 \\ \text{BSC} \end{matrix}$
- Feature 3 height: $.010 \begin{matrix} 0.18 \\ \text{BSC} \end{matrix}$

Notes:

- Controlling dimensions in millimeters
- Ref: JEDEC MO-203AA

Ordering Information

Ordering Code	Packaging Code	Package Type	Top Marking
PI5A121TX	T	5-pin, 65-mil wide SOT-23	ZV
PI5A121TEX	T	Pb-free & Green, 5-pin, 65-mil wide SOT-23	$\bar{Z}V$
PI5A121CX	C	5-pin, 50-mil wide SOT-23	ZV
PI5A121CEX	C	Pb-free & Green, 5-pin, 50-mil wide SOT-23	$\bar{Z}V$
PI5A122TX	T	5-pin, 65-mil wide SOT-23	ZU
PI5A122TEX	T	Pb-free & Green, 5-pin, 65-mil wide SOT-23	$\bar{Z}U$
PI5A122CX	C	5-pin, 50-mil wide SOT-23	ZU
PI5A122CEX	C	Pb-free & Green, 5-pin, 50-mil wide SOT-23	$\bar{Z}U$
PI5A124TX	T	5-pin, 65-mil wide SOT-23	ZT
PI5A124TEX	T	Pb-free & Green, 5-pin, 65-mil wide SOT-23	$\bar{Z}T$

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. X = Tape/Reel