INTERSIL

ICM7211 (LCD)
ICM7212 (LED)
Four Digit CMOS Display Decoder/Drivers

ICM7211 (LCD) FEATURES

- **Four digit non-multiplexed 7 segment LCD display oututs with backplane driver**
- **Complete onboard RC oscillator to generate backplane frequency.**
- **Backplane input/output allows simple synchronization of slave-device segment outputs to a master backplane signal.**
- **ICM7211 devices provide separate digit select inputs to accept multiplexed BCD input (Pinout and functionally compatible with Siliconix DF411).**
- **ICM7211M devices provide data and digit select code input latches controlled by chip select inputs to provide a direct high speed processor interface.**
- **ICM7211 decodes binary to hexadecimal; ICM7211A decodes binary to Code B (0-9, dash, E, H, L, P, blank)**

ICM7212 (LED) FEATURES

- **28 current-limited segment outputs provide 4-digit non-multiplexed direct LED drive at > 5mA per segment.**
- **Brightness input allows direct control of LED segment current with a single potentiometer. Can function digitally as a display enable.**
- **ICM7212M and ICM7212A devices provide same input configuration and output decoding options as the ICM7211.**

DESCRIPTION

The ICM7211 (LCD) and ICM7212 (LED) devices constitute a family of non-multiplexed four-digit seven-segment CMOS display decoder-drivers.

The ICM7211 devices are configured to drive conventional LCD displays by providing a complete RC oscillator, divider chain, backplane driver, and 28 segment outputs. These outputs provide the zero d.c. component signals necessary for long display life.

The ICM7212 devices are configured to drive common-anode LED displays, providing 28 current-controlled low leakage open-drain n-channel outputs. These devices provide a BRIGHTNESS input, which may be used at normal logic levels as a display enable, or with a potentiometer as a continuous display brightness control.

Both the LCD and LED devices are available with two input configurations. The basic devices provide four data-bit inputs and four digit select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the ICM7217, ICM7226 and ICL7103. The microprocessor interface (suffix M) devices provide data input latches and digit select code latches under control of high-speed chip select inputs. These devices simplify the task of implementing a cost-effective alphanumeric 7-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices will provide two different decoder configurations. The basic device will decode the four bit binary input into a seven-segment alphanumeric hexa-decimal output. The "A" versions will provide the same output code as the ICM7218 "Code B", i.e., 0-9, dash, E, H, L, P, blank. Either device will correctly decode true BCD to seven segment decimal outputs.

Devices in the ICM7211/7212 family are packaged in a standard 40 pin plastic dual-in-line package and all inputs are fully protected against static discharge.

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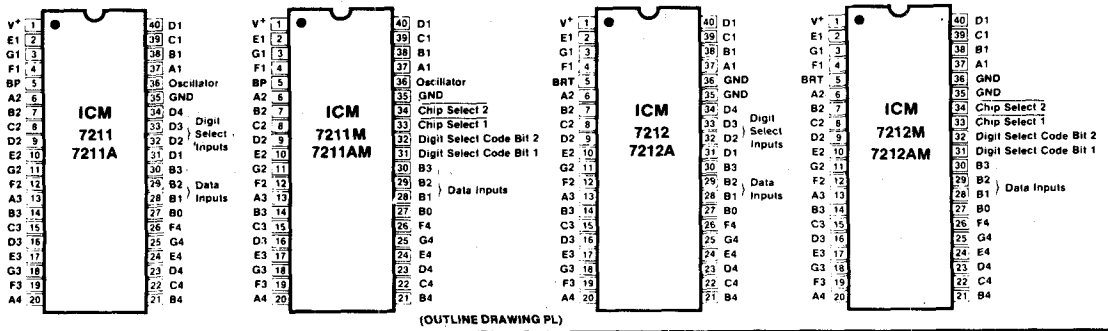
PIN CONFIGURATIONS (OUTLINE DRAWING PL)



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W @ 70°C
Supply Voltage 6.5V
Input Voltage (Any Terminal) (Note 2) ..... V^+ +0.3V, GROUND −0.3V
Operating Temperature Range ..... −20°C to +85°C
Storage Temperature Range ..... −55°C to +125°C
Lead Temperature (Soldering 10 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: This limit refers to that of the package and will not be realized during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

TABLE I: OPERATING CHARACTERISTICS

TEST CONDITIONS: All parameters measured with $V^+ = 5V$

ICM7211 CHARACTERISTICS (LCD)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	I_{op}	Test circuit, Display blank		10	50	µA
Oscillator Input Current	I_{OSCI}	Pin 36		±2	±10	
Segment Rise/Fall Time	t_{rfs}	C_L = 200pF		0.5		µs
Backplane Rise/Fall Time	t_{rfb}	C_L = 5000pF		1.5		
Oscillator Frequency	f_{osc}	Pin 36 Floating		16		kHz
Backplane Frequency	f_{bp}	Pin 36 Floating		125		Hz

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ICM7212 CHARACTERISTICS (COMMON ANODE LED)

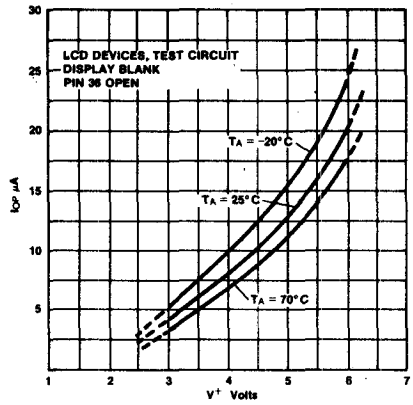
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{OP}	Pin 5 (Brightness), Pins 27-34 - GROUND		10	50	µA
Operating Current	I_{OP}	Pin 5 at V^+, Display all 8's		200		mA
Segment Leakage Current	I_{SLK}	Segment Off		±0.01	±1	µA
Segment On Current	I_{SEG}	Segment On, V_O = +3V	5	8		mA

INPUT CHARACTERISTICS

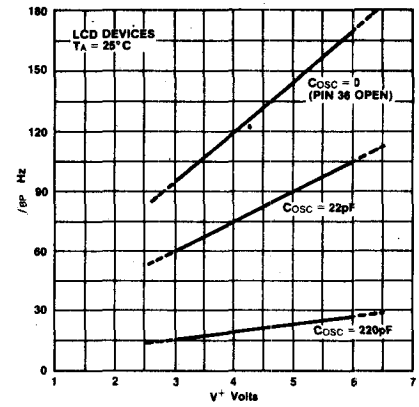
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" input voltage	V_{IH}		3			V
Logical "0" input voltage	V_{IL}				1	
Input leakage current	I_{ILK}	Pins 27-34		±.01	±1	µA
Input capacitance	C_{IN}	Pins 27-34		5		pF
BP/Brightness input leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND		±.01	±1	µA
BP/Brightness input capacitance	C_{BPI}	All Devices		200		pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{sa}	Refer to Timing Diagrams	1			µs
Data Setup Time	t_{ds}		500			ns
Data Hold Time	t_{dh}		200			
Inter-Digit Select Time	t_{ids}		2			µs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE						
Chip Select Active Pulse Width	t_{csa}	other chip select either held active, or both driven together	200			ns
Data Setup Time	t_{ds}		100			
Data Hold Time	t_{dh}		10	0		
Inter-Chip Select Time	t_{ics}		2			µs

TYPICAL CHARACTERISTICS

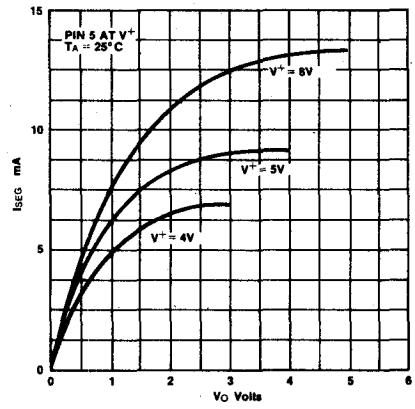
ICM7211 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



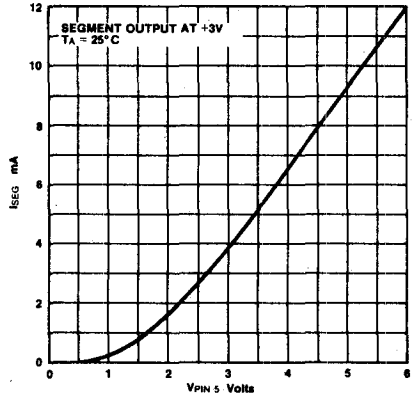
ICM7211 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



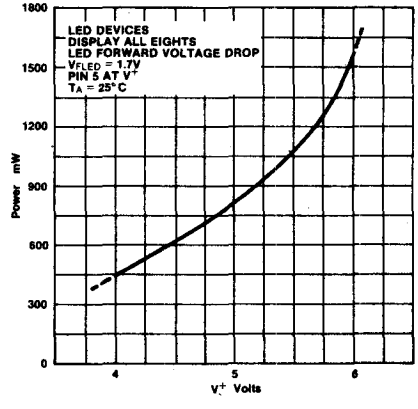
ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE



ICM7212 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



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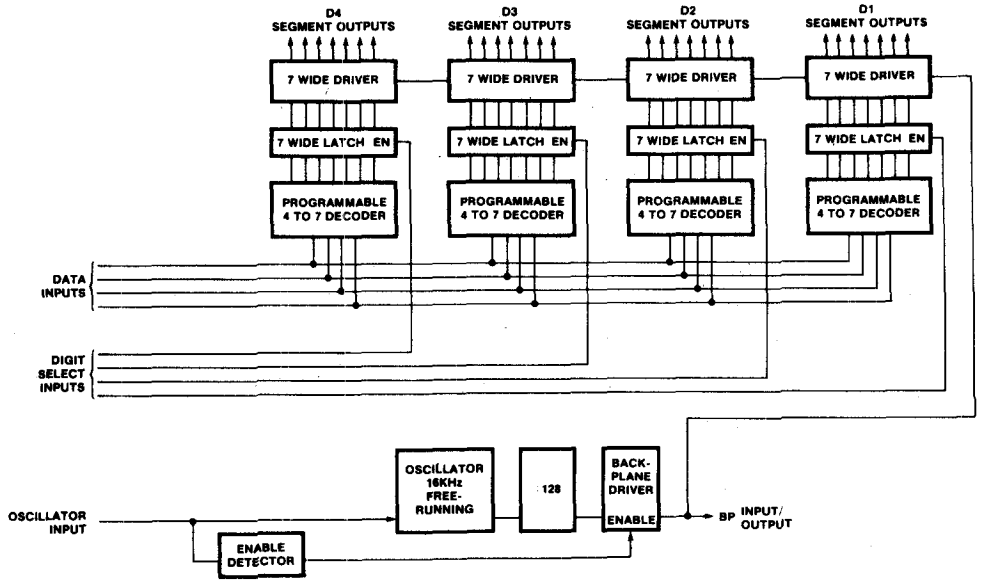
BLOCK DIAGRAMS

ICM7211 (A)



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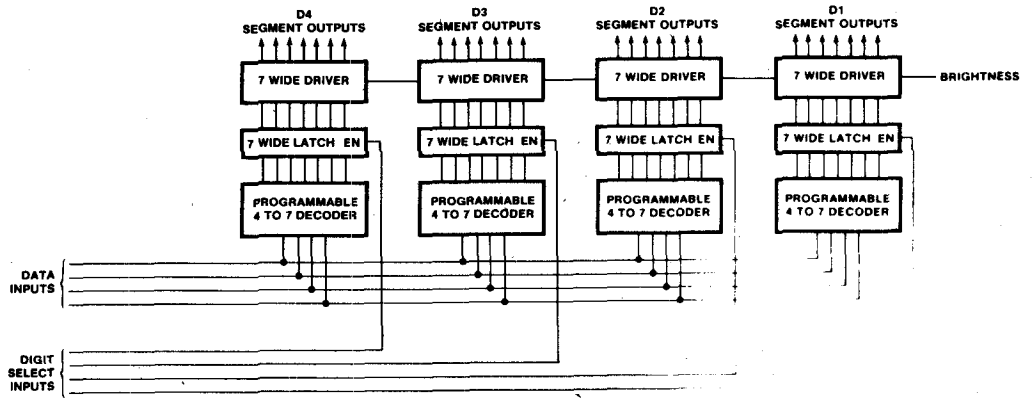
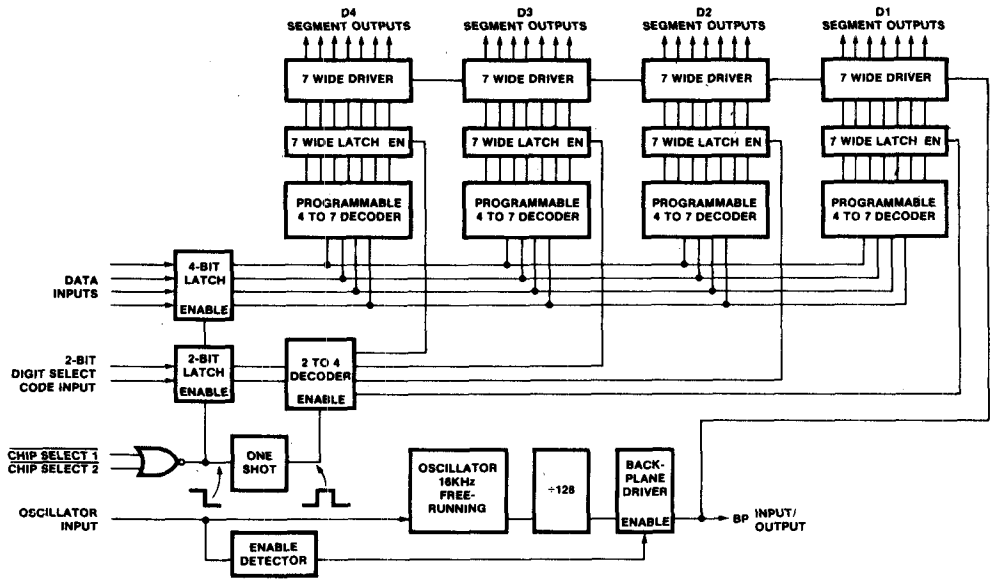
ICM7212 (A)



ICM7211(A)M



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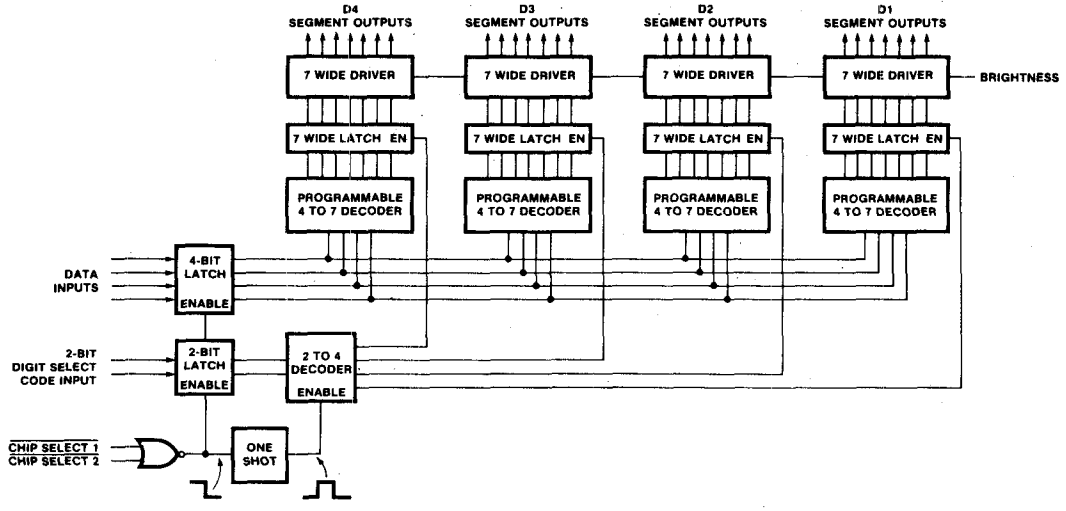
ICM7212(A)M



INPUT DEFINITIONS

In this table, V+ and GROUND are considered to be normal operating input logic levels. Actual input low and high levels are specified in Table 1. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V^+ = Logical One GND = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V^+ = Logical One GND = Logical Zero	Twos	
B2	29	V^+ = Logical One GND = Logical Zero	Fours	
B3	30	V^+ = Logical One GND = Logical Zero	Eights (Most significant)	
OSC (LCD Devices Only)	36	Floating or with external capacitor GROUND	Oscillator input Disables BP output devices, allowing segments to be synced to an external signal input at the BP terminal (Pin 5)	

ICM7211/ICM7212
MULTIPLEXED-BINARY INPUT CONFIGURATION

INPUT	TERMINAL	CONDITION	FUNCTION
D1	31	V^+ = Active GND = Inactive	D1 (Least significant) Digit Select
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 (Most significant) Digit Select

ICM7211M/ICM7212M
MICROPROCESSOR INTERFACE INPUT CONFIGURATION

INPUT	DESCRIPTION	TERMINAL	CONDITION	FUNCTION
DS1	Digit Select Code Bit 1 (LSB)	31	V^+ = Logical One GND = Logical Zero	DS1 & DS2 serve as a two bit Digit Select Code Input DS2, DS1 = 00 selects D4 DS2, DS1 = 01 selects D3 DS2, DS1 = 10 selects D2 DS2, DS1 = 11 selects D1
DS2	Digit Select Code bit 2 (MSB)	32		
$\overline{CS1}$	Chip Select 1	33	V = Inactive GND = Active	When both $\overline{CS1}$ and $\overline{CS2}$ are taken low, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of either Chip Select, the data is decoded and written into the output latches.
$\overline{CS2}$	Chip Select 2	34		

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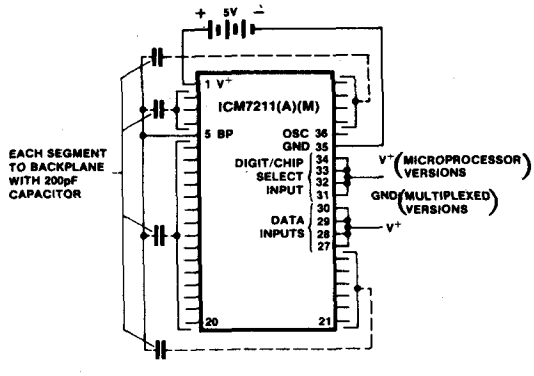
TEST CIRCUIT



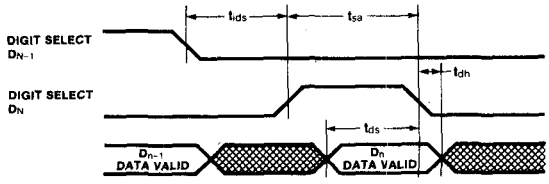


Figure 1: Multiplexed Input Timing Diagram

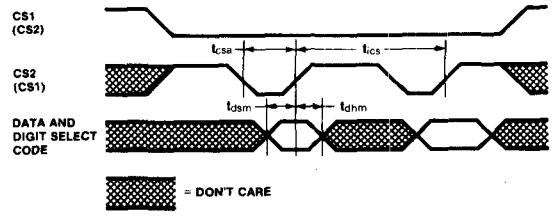


Figure 2: Microprocessor Interface Input Timing Diagram

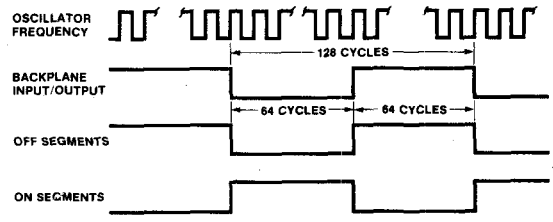
DESCRIPTION OF OPERATION

LCD DEVICES

The LCD devices in the family (ICM7211, 7211A, 7211M, 7211AM) provide outputs suitable for driving conventional four-digit by seven-segment LCD displays, including 28 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any dc component, which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCillator input (pin 36) to GROUND. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device, or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device represents a load of approximately 200pF (comparable to one additional segment), thus the limitation of the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits; and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane output driver should handle the backplane to a display of 16 one-half-inch characters (rise and fall times not exceeding 5μs. ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7211 devices be slaved to it. This external signal should be capable of driving very



Display Waveforms

large capacitive loads with short (1-2μs) rise and fall times. The maximum frequency for a backplane signal should be about 125Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 16KHz at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 125Hz with the oscillator free-running; the oscillator frequency may be reduced by connecting an external capacitor to the OSCillator terminal.

The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This can be done by driving the OSCillator input between the positive supply and a level out of the range where the backplane disable is sensed (about one fifth of the supply voltage above GROUND). Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

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LED DEVICES

The LED devices in the family (ICM7212, 7212A, 7212M, 7212AM) provide outputs suitable for directly driving four-digit by seven-segment common-anode LED displays, including 28 individual segment drivers, each consisting of a low-leakage, current-controlled, open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRIGHTNESS input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Fig (3). The potentiometer should be a high value (100KΩ to 1MΩ) to minimize I^2R power consumption, which can be significant when the display is off.

The BRIGHTNESS input may also be operated digitally as a display enable; when high, the display is fully on, and low fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two voltages at the Brightness input.

Note that the LED devices have two connections for GROUND; both of these pins should be connected. The

double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (–15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V^+ - V_{FLED})(I_{SEG})(n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the Brightness input to keep power dissipation within the limits described above.

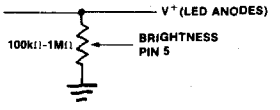


Figure 3: Brightness control

INPUT CONFIGURATIONS AND OUTPUT CODES

The standard devices in the ICM7211/12 family accept a four-bit true binary (ie, positive level = logical one) input at pins 27 thru 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7211, ICM7211M, ICM7212, and ICM7212M devices decode this binary input into a seven-segment alphanumeric hexadecimal output, while the ICM7211A, ICM7211AM, ICM7212A, and ICM7212AM decode the binary input into the same seven-segment output as in the ICM7218 "Code B", ie 0-9, dash, E, H, L, P, blank. These codes are shown explicitly in Table 2. Either decoder option will correctly decode true BCD to a seven-segment decimal output.

These devices are actually mask-programmable to provide any 16 combinations of the seven segment outputs decoded from the four input bits. For larger quantity orders, (10K pcs. minimum) custom decoder options can be arranged. Contact the factory for details.

The ICM7211, ICM7211A, ICM7212, and ICM7212A devices are designed to accept multiplexed binary or BCD input. These devices provide four separate digit lines (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30. More than one digit select may be activated simultaneously (which will write the same character into all selected digits), although the timing requirements shown in Fig (1) and Table 1 for data setup, hold, and inter-digit select times must be met to ensure correct output.

The ICM7211M, ICM7211AM, ICM7212M, and ICM7212AM devices are intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the two-bit digit select code (DS1 pin 31, DS2 pin 32) are written into input buffer latches when both chip select inputs (CS1 pin 33, CS2 pin 34) are taken low. On the rising edge of either chip select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the digit select code latches.

A select code of 00 writes into D4, SC2 = 0, SC1 = 1 writes into D3, SC2 = 1, SC1 = 0 writes into D2, and 11 writes into D1. The timing relationships for inputting data are shown in Fig (2), and the chip select pulse widths and data setup and hold times are specified in Table 1.

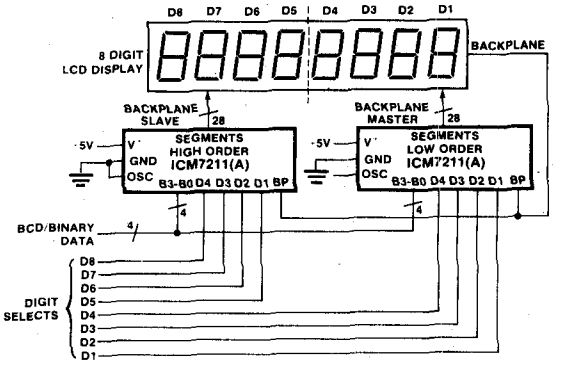
BINARY B3	B2	B1	B0	HEXADECIMAL ICM7211(M) ICM7212(M)	CODE B ICM7211A(M) ICM7212A(M)
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

Table 2: Output Codes

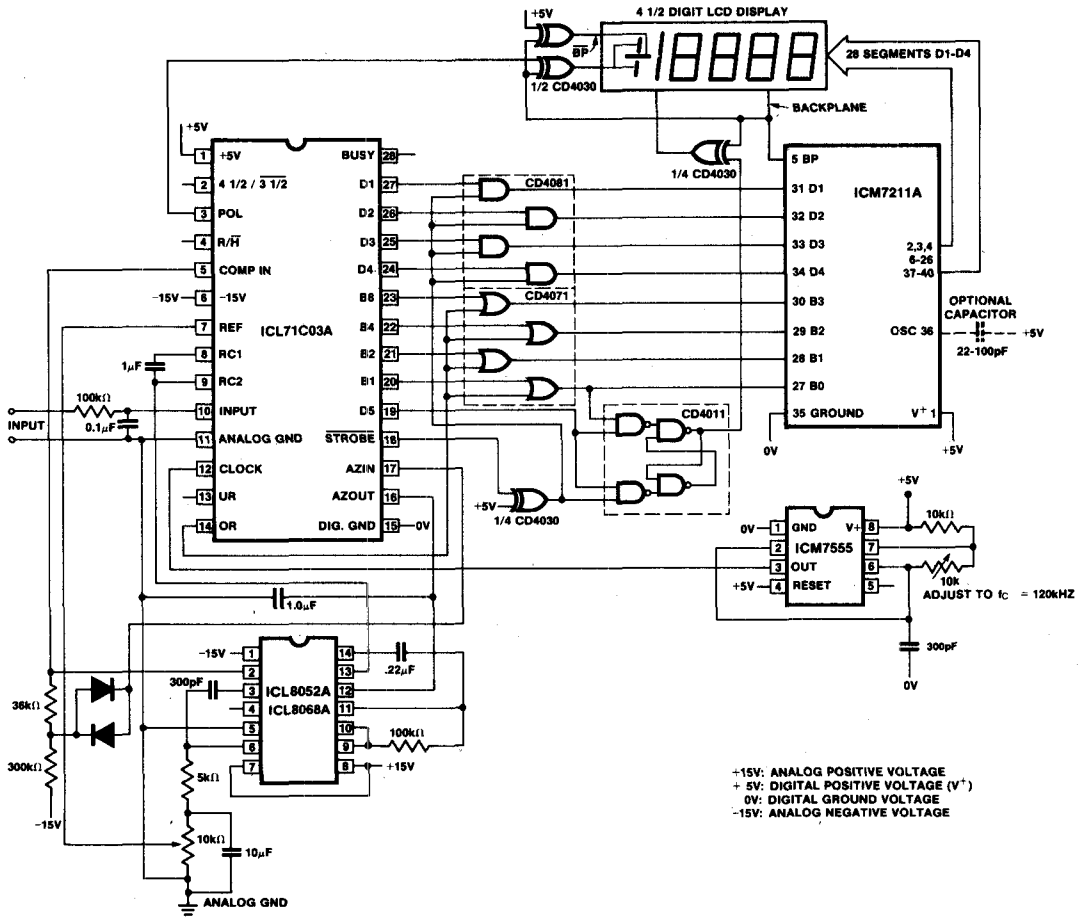
SEGMENT ASSIGNMENT

APPLICATIONS

1. Ganged ICM7211's Driving 8-Digit LCD Display.

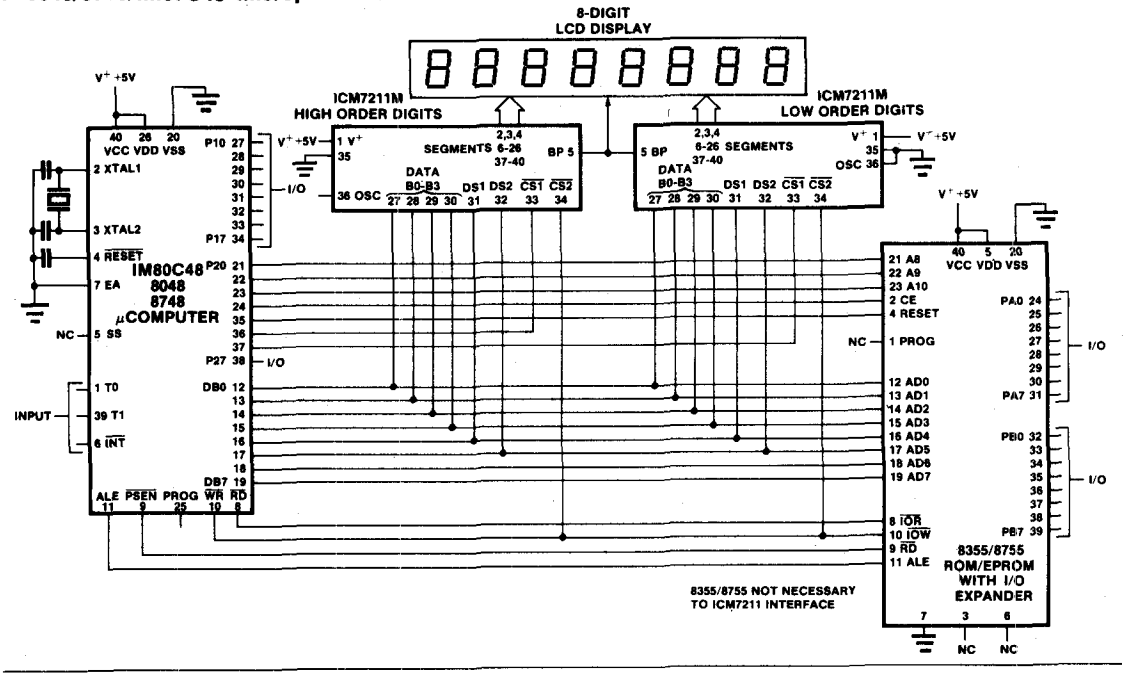


2. 4 1/2 Digit LCD DPM with Digit Blanking on Overrange.



NOTE: See also ICL8052/8068/ICL71C03 Data Sheet for a similar circuit with fewer features.

3. 8048/8748/IM87C48 Microprocessor Interface.



ORDER PART NUMBER		OUTPUT CODE	INPUT CONFIGURATIONS	DICE
LCD DISPLAY	ICM7211 IPL ICM7211A IPL	HEXADECIMAL CODE B	MULTIPLEXED 4-BIT	ICM7211/D ICM7211A/D
	ICM7211M IPL ICM7211AM IPL	HEXADECIMAL CODE B	MICROPROCESSOR INTERFACE	ICM7211M/D ICM7211AM/D
LED DISPLAY	ICM7212 IPL ICM7212A IPL	HEXADECIMAL CODE B	MULTIPLEXED 4-BIT	ICM7212/D ICM7212A/D
	ICM7212M IPL ICM7212AM IPL	HEXADECIMAL CODE B	MICROPROCESSOR INTERFACE	ICM7212M/D ICM7212AM/D

TABLE 3: Option Matrix and Ordering Information