



Complementary 20-V (D-S) MOSFET

Characteristics

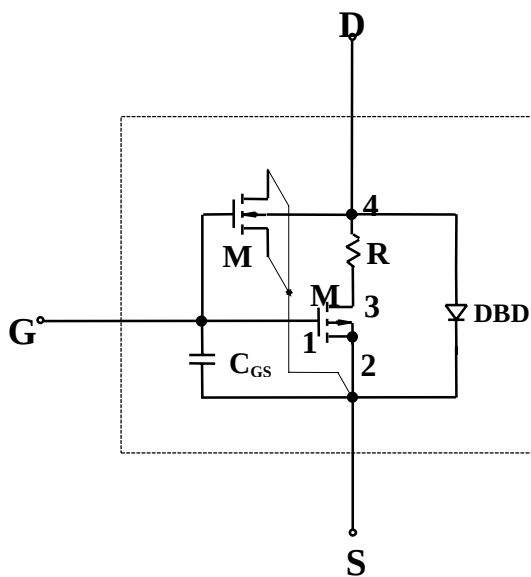
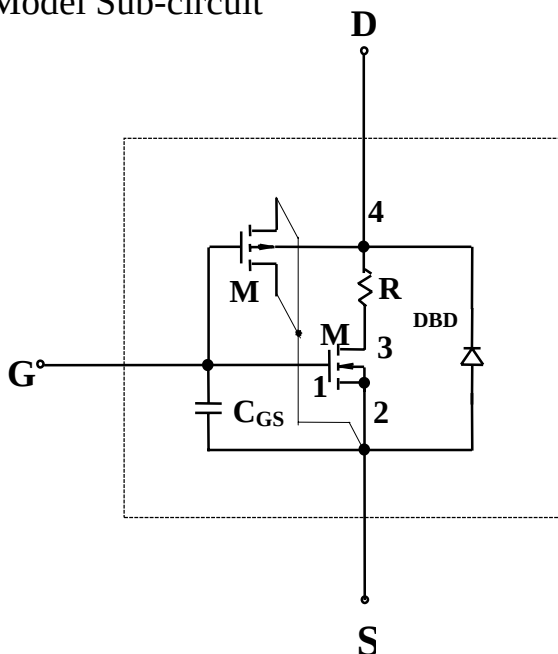
- N- and P- channel Vertical DMOS
- Macro-Model (Sub-circuit)
- Level 3 MOS
- Applicable for Both Linear and Switch Mode
- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

Description

The attached SPICE Model describes typical electrical characteristics of the n- and p- channel vertical DMOS. The sub-circuit model was extracted and optimized over a 25°C to 125°C temperature range under pulse conditions for 0 to -4.5 volts gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain

feedback capacitance network is used to model gate charge characteristics while avoiding convergence problems of switched C_{gd} model. Model parameter values are optimized to provide a best fit to measure electrical data and are not intended as an exact physical description of a device.

Model Sub-circuit



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPICE Device Model Si1551DL

Model Evaluation

N- and P- Channel Device ($T_J=25^{\circ}\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Conditions		Typical	Unit		
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA V _{DS} = V _{GS} , I _D = -250μA	N-Ch	1.1	V		
			P-Ch	1.1			
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5V, V _{GS} = 4.5V V _{DS} = -5V, V _{GS} = -4.5V	N-Ch	1.1	A		
			P-Ch	3.1			
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5V, I _D = 0.29A V _{GS} = -4.5V, I _D = - 0.41A V _{GS} = 2.7V, I _D = 0.1A V _{GS} = -2.7V, I _D = - 0.25A V _{GS} = 2.5V, I _D = 0.1A V _{GS} = -2.5V, I _D = - 0.25A	N-Ch	1.64	Ω		
			P-Ch	0.85			
			N-Ch	2.34			
			P-Ch	1.2			
			N-Ch	2.58			
			P-Ch	1.33			
Forward Transconductance ^a	g _{fs}	V _{DS} = 10V, I _D = 0.29A V _{DS} = -10V, I _D = -0.41A	N-Ch	0.33	S		
			P-Ch	0.80			
Diode Forward Voltage ^a	V _{SD}	I _S = 0.23A, V _{GS} = 0V	N-Ch	0.67	V		
		I _S = -0.23A, V _{GS} = 0V	P-Ch	-0.76			
Dynamic ^b							
Total Gate Charge	Q _g	N-Channel V _{DS} = 10V, V _{GS} = 4.5V, I _D = 0.29A P-Channel V _{DS} = -10V, V _{GS} = -4.5V, I _D = -0.41A	N-Ch	0.55	nC		
			P-Ch	0.54			
Gate-Source Charge	Q _{gs}		N-Ch	0.22			
			P-Ch	0.11			
Gate-Drain Charge	Q _{gd}		N-Ch	0.13			
			P-Ch	0.14			
Turn-On Delay Time	t _{d(on)}		N-Channel V _{DD} = 10V, R _L = 20Ω I _D ≅ 0.5A, V _{GEN} = 4.5V, R _G = 6Ω P-Channel V _{DD} = -10V, R _L = 20Ω I _D ≅ -0.5A, V _{GEN} = -4.5V, R _G = 6Ω	N-Ch		18	ns
				P-Ch		8.8	
Rise Time	t _r	N-Ch		21			
		P-Ch		11			
Turn-Off Delay Time	t _{d(off)}	N-Ch		21			
		P-Ch		11			
Fall Time	t _f	N-Ch		22			
		P-Ch		12			
Source-Drain Reverse Recovery Time	t _r	I _F = 0.23A, di/dt = 100A/μs	N-Ch	20			
		I _F = - 0.23A, di/dt =100A/μs	P-Ch	25			

Notes:

- a) Pulse test; pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- b) Guaranteed by design, not subject to production testing

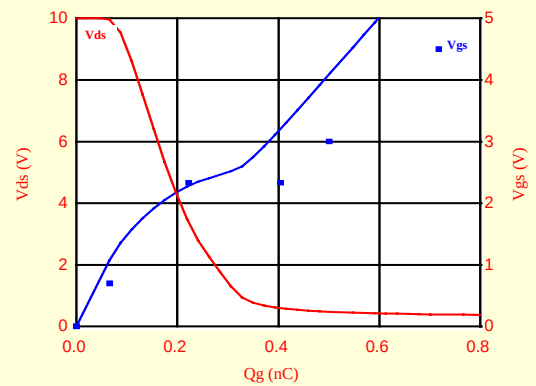
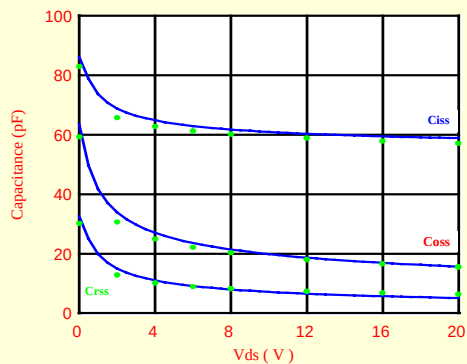
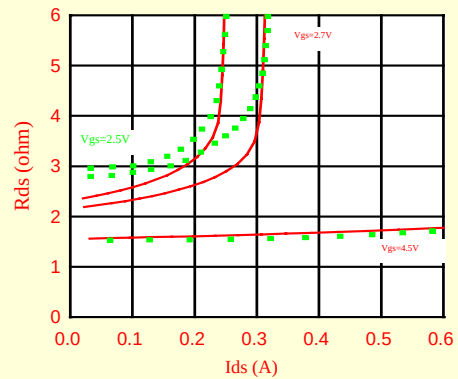
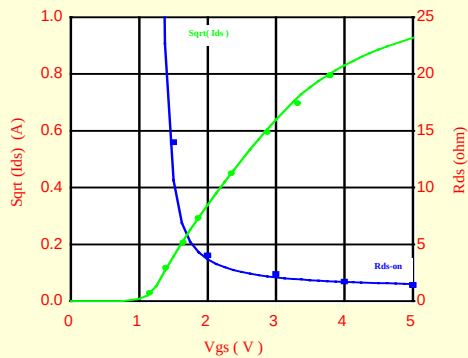
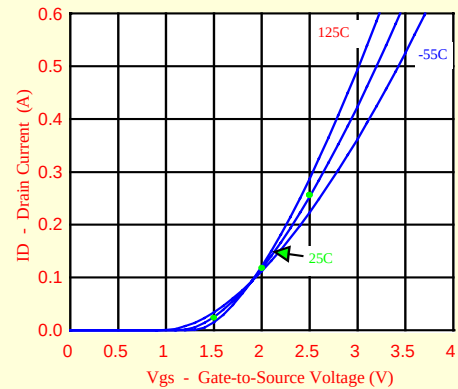
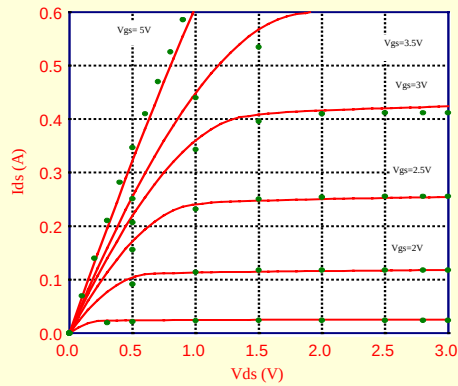


SPICE Device Model Si1551DL

Comparison of Model with Measured Data

N-Channel MOSFET

($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)





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