TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC670AP,TC74HC670AF

4 Word × 4 Bit Register File (3-state)

The TC74HC670A is a high speed 4-WORDS × 4-BITS REGISTER FILE fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The register file is organized as 4 words of 4 bits each.

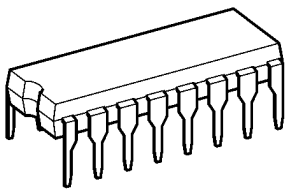
Separate read and write address inputs (RA, RB, and WA, WB) and enable inputs ($\overline{RE}$, $\overline{WE}$) are available permitting simultaneous writing into one word location and reading from another location.

Four data inputs (D0~D3) are provided to store the 4-bit words.

The write address inputs (WA, WB) determine the location of the stored word in the register. When write Enable ($\overline{WE}$) is held low, the data is entered into addressed location. When $\overline{WE}$ is held high, data and address inputs are inhibited. The data acquisition from the four registers is made possible by the read address inputs (RA, RB) when the Read Enable ($\overline{RE}$) is held low. When RE is held high the data outputs are in the high impedance state.

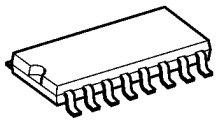
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74HC670AP



DIP16-P-300-2.54A

TC74HC670AF



SOP16-P-300-1.27A

Weight

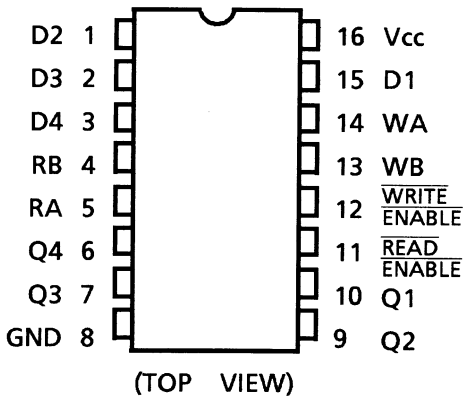
DIP16-P-300-2.54A : 1.00 g (typ.)

SOP16-P-300-1.27A : 0.18 g (typ.)

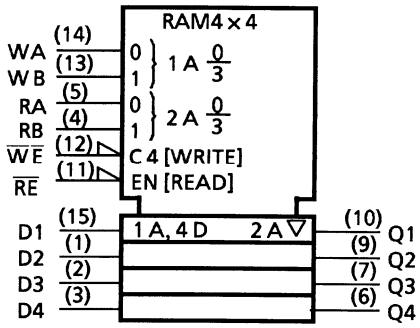
Features

- High speed: t_{pd} = 23 ns (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 4 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Pin and function compatible with 74LS670

Pin Assignment



IEC Logic Symbol



Truth Table

Write Function Table

Write Inputs			Words			
WB	WA	$\overline{WE}$	0	1	2	3
L	L	L	Q = D	Q0	Q0	Q0
L	H	L	Q0	Q = D	Q0	Q0
H	L	L	Q0	Q0	Q = D	Q0
H	H	L	Q0	Q0	Q0	Q = D
X	X	H	Q0	Q0	Q0	Q0

Read Function Table

Read Inputs			Outputs			
RB	RA	$\overline{RE}$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

X: Don't care

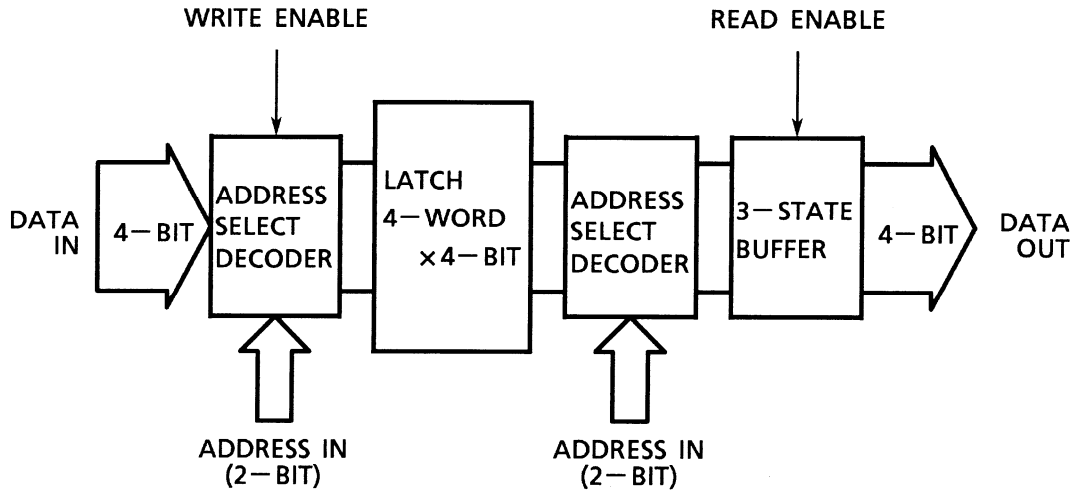
Z: High impedance

(Q = D): The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

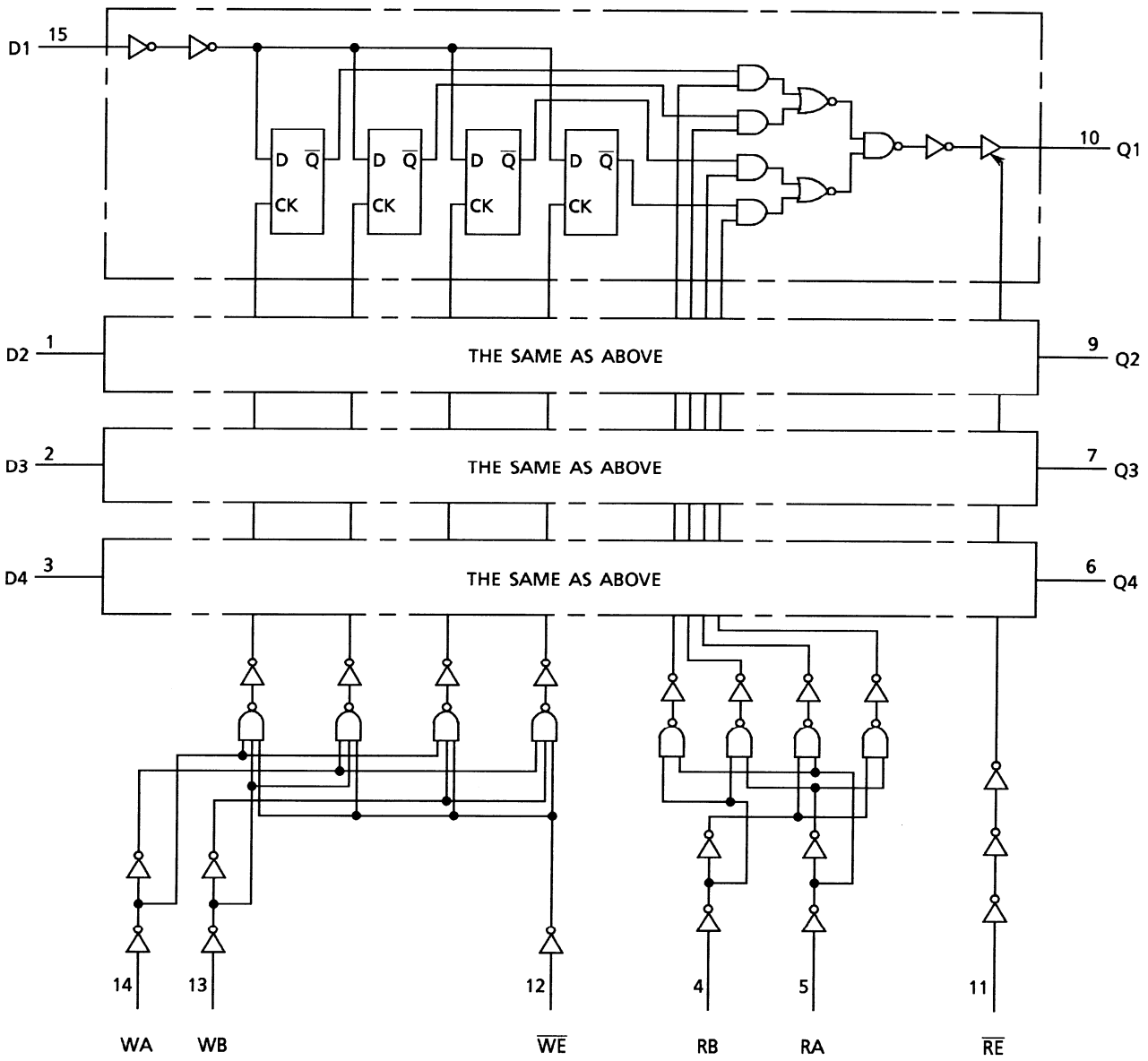
Q0: The level of Q before the indicated input conditions were established.

W0B1: The first bit of word 0, etc.

Block Diagram



System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C should be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V) 0 to 500 (V_{CC} = 4.5 V) 0 to 400 (V_{CC} = 6.0 V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I_{OH} = −4 mA	4.5	4.18	4.31	—	4.13	—	
			I_{OH} = −5.2 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
			I_{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	—	±0.5	—	±5.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 to 85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width ($\overline{WE}$)	$t_{W(L)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (Dn- $\overline{WE}$)	t_s	—	2.0	—	50	65	ns
			4.5	—	10	13	
			6.0	—	9	11	
Minimum set-up time (WA, WB- $\overline{WE}$)	t_s	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum hold time (Dn- $\overline{WE}$)	t_h	—	2.0	—	5	5	ns
			4.5	—	5	5	
			6.0	—	5	5	
Minimum hold time (WA, WB- $\overline{WE}$)	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum latch time ($\overline{WE}$ -RA, RB)	t_{latch}	(Note)	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	

Note: t_{latch} is the time allowed for the internal output of the latch to assume the state of new data.

This is important only when attempting to read from a location immediately after that location has received new data.

AC Characteristics ($C_L = 15$ pF, $V_{CC} = 5$ V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH} t_{THL}	—	—	4	8	ns
Propagation delay time (RA, AB-Qn)	t_{pLH} t_{pHL}	—	—	23	34	ns
Propagation delay time ($\overline{WE}$ -Qn)	t_{pLH} t_{pHL}	—	—	24	38	ns
Propagation delay time (Dn-Qn)	t_{pLH} t_{pHL}	—	—	22	32	ns
3-state output enable time	t_{pZL} t_{pZH}	$R_L = 1$ kΩ	—	11	18	ns
3-state output disable time	t_{pLZ} t_{pHZ}	$R_L = 1$ kΩ	—	11	15	ns

AC Characteristics (C_L = 50 pF, input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
Output transition time	t_{TLH} t_{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (RA, AB-Qn)	t_{pLH} t_{pHL}	—	2.0	—	90	195	—	245	ns
			4.5	—	27	39	—	49	
			6.0	—	22	33	—	42	
Propagation delay time ($\overline{WE}$ -Qn)	t_{pLH} t_{pHL}	—	2.0	—	95	220	—	275	ns
			4.5	—	28	44	—	55	
			6.0	—	22	37	—	47	
Propagation delay time (Dn-Qn)	t_{pLH} t_{pHL}	—	2.0	—	90	185	—	230	ns
			4.5	—	26	37	—	46	
			6.0	—	20	31	—	39	
Output enable time	t_{pZH} t_{pZL}	R_L = 1 kΩ	2.0	—	46	110	—	140	ns
			4.5	—	14	22	—	28	
			6.0	—	12	19	—	24	
Output disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	2.0	—	25	95	—	120	ns
			4.5	—	14	19	—	24	
			6.0	—	12	16	—	20	
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Output capacitance	C_{OUT}	—		—	10	—	—	—	pF
Power dissipation capacitance	C_{PD} (Note)	—		—	101	—	—	—	pF

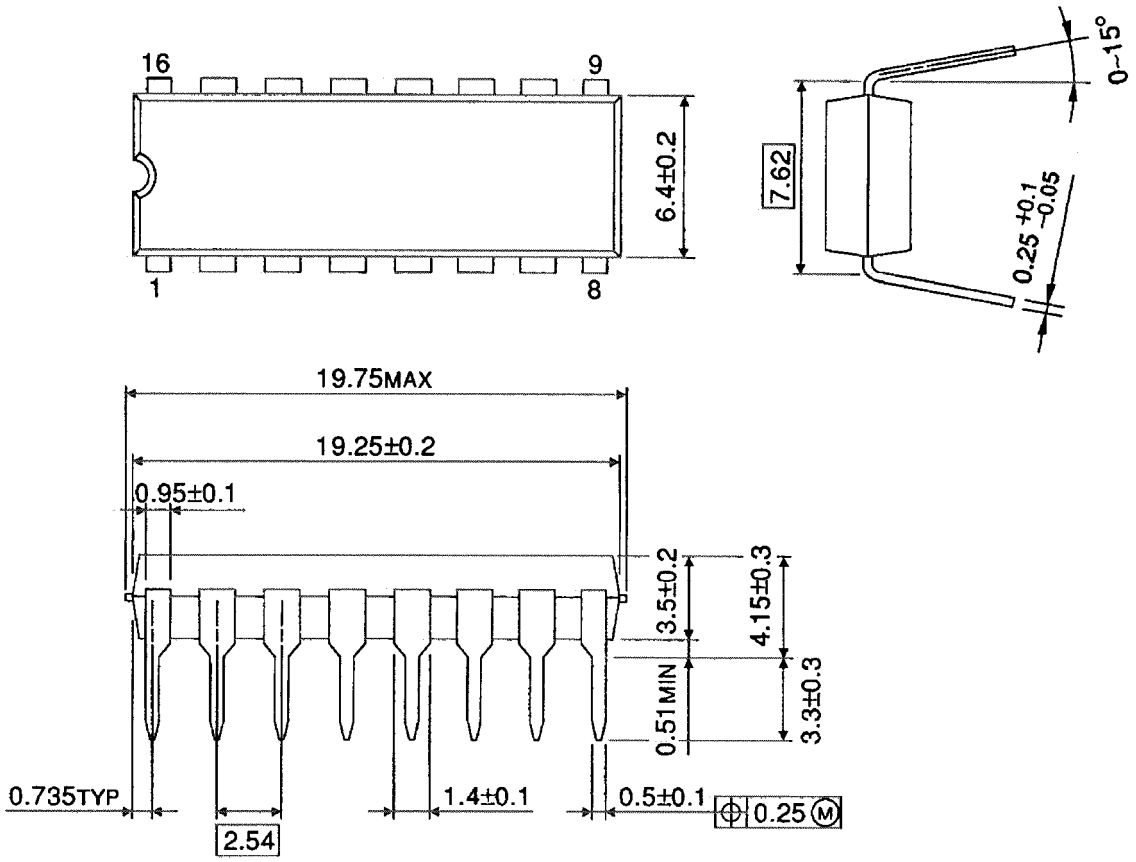
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

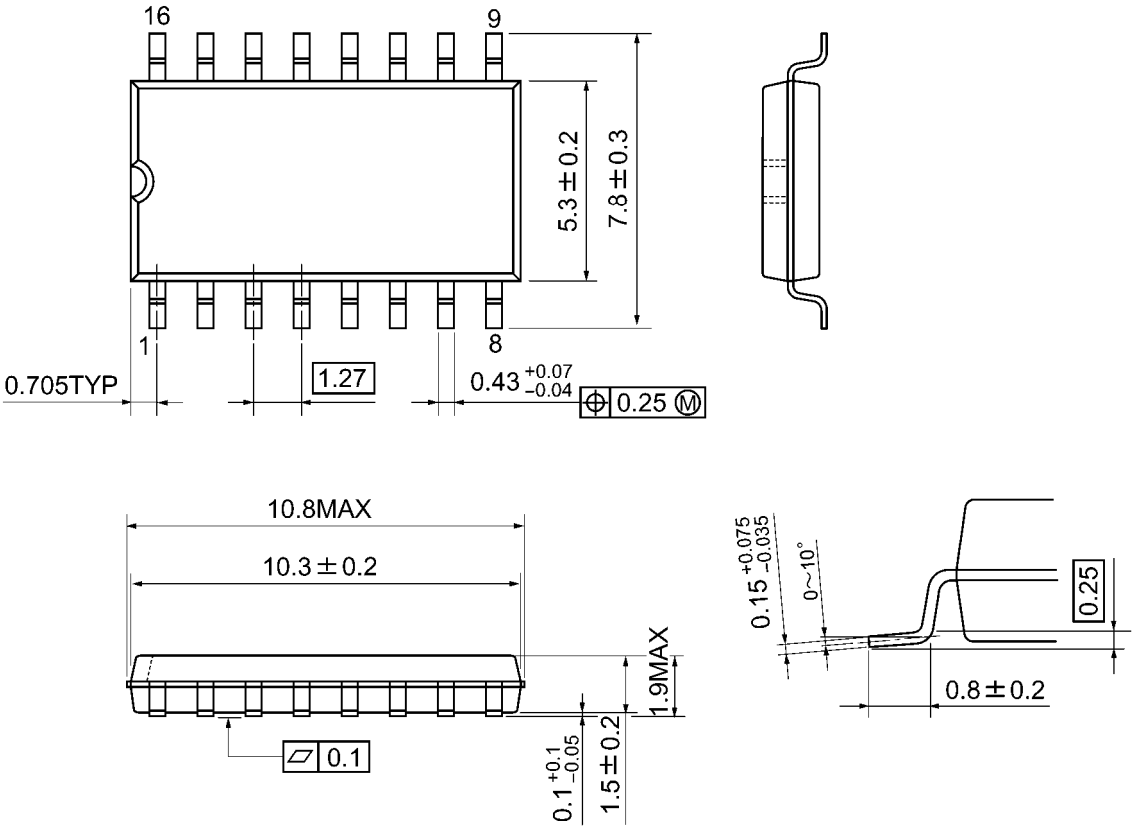
DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

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