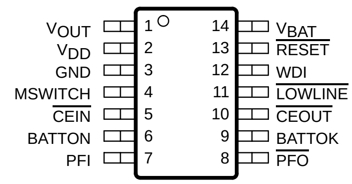
features

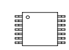
- Supply Current of 40 μA (Max)
- Battery Supply Current of 100 nA (Max)
- Precision Supply-Voltage Monitor, 1.8 V, 5 V; Other Options on Request
- Watchdog Timer With 800-ms Time-Out
- Backup-Battery Voltage Can Exceed V_{DD}
- Power-On Reset Generator With Fixed 100-ms Reset Delay Time
- Battery-OK Output
- Voltage Monitor for Power-Fail or Low-Battery Monitoring
- Manual Switchover to Battery-Backup Mode
- Chip-Enable Gating . . . 3 ns (at V_{DD} = 5 V) Max Propagation Delay
- Battery-Freshness Seal
- 14-pin TSSOP Package
- Temperature Range . . . –40°C to 85°C

typical applications

- Fax Machines
- Set-Top Boxes
- Advanced Voice Mail Systems
- Portable Battery-Powered Equipment
- Computer Equipment
- Advanced Modems
- Automotive Systems
- Portable Long-Time Monitoring Equipment
- Point of Sale Equipment

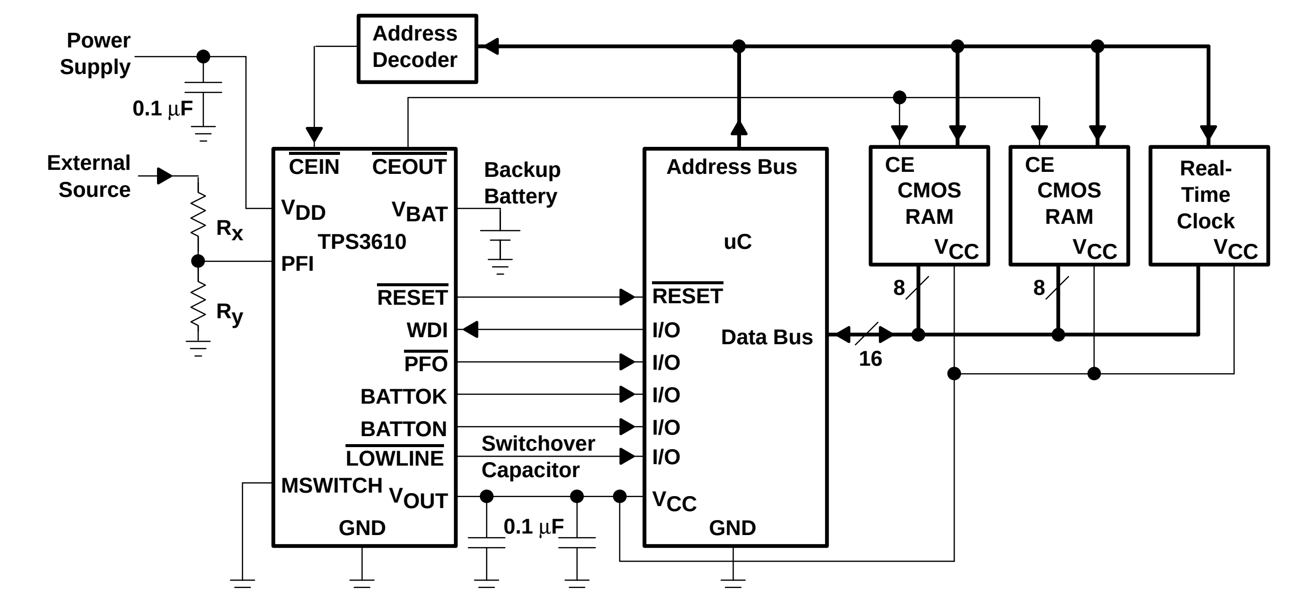
TPS3610
TSSOP (PW) Package
(TOP VIEW)





ACTUAL SIZE
(5,10mm x 6,60mm)

typical operating circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description

The TPS3610 family of supervisory circuits monitors and controls processor activity by providing backup-battery switchover for data retention of CMOS RAM. Other features include an additional power-fail comparator, low-line indication, watchdog function, battery-status indicator, manual switchover, and write protection for CMOS RAM.

The TPS3610 family allow usage of 3-V or 3.6-V lithium batteries as the backup supply in systems with, e.g., V_{DD} = 1.8 V. During power-on, $\overline{RESET}$ is asserted when the supply voltage (V_{DD} or V_{BAT}) becomes higher than 1.1 V. Thereafter, the supply-voltage supervisor monitors V_{DD} and keeps $\overline{RESET}$ output active as long as V_{DD} remains below the threshold voltage V_{IT}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V_{DD} has risen above the threshold voltage V_{IT}. When the supply voltage drops below the threshold voltage V_{IT}, the output becomes active (low) again.

The product spectrum is designed for supply voltages of 1.8 V and 5 V. The circuits are available in a 14-pin TSSOP package. TPS3610 devices are characterized for operation over a temperature range of –40°C to 85°C.

standard and application-specific versions (see Note 1)

TPS3610U 18 PW R

- **R** — **Tape and Reel**
- **PW** — **TI Package Designator**
- **18** — **Nominal Supply Voltage**
- **U** — **Nominal Battok Threshold Voltage**

APPLICATION-SPECIFIC VERSIONS, NOMINAL SUPPLY AND BATTOK VOLTAGE			
T_A	NOMINAL SUPPLY VOLTAGE, $V_{DD(NOM)}$ (V)	NOMINAL BATTOK THRESHOLD VOLTAGE, $V_{IT(BOK)}$ (V)	PACKAGED DEVICES TSSOP (PW)†
–40°C to 85°C	1.8	1.6	TPS3610U18PWR
	5	2.4	TPS3610T50PWR

† The PW package is only available taped and reeled (indicated by the R suffix on the device type).

NOTE 1: For other NOMINAL and BATTOK voltage versions, contact your local TI sales office for availability and order lead time.

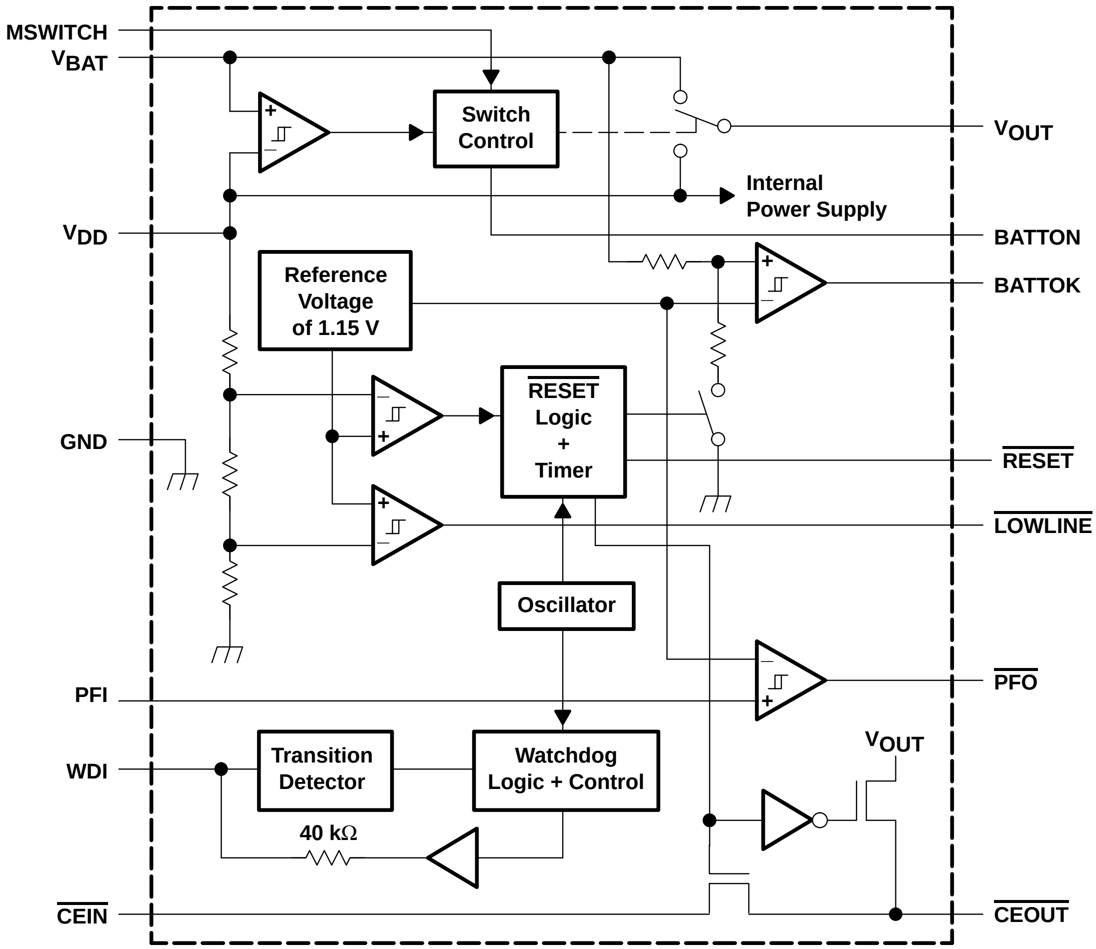
TRUTH TABLES

INPUTS				OUTPUTS				
$V_{DD} > V_{LL}$	$V_{DD} > V_{IT}$	$V_{DD} > V_{BAT}$	MSWITCH	V_{OUT}	BATTON	$\overline{\text{LOWLINE}}$	$\overline{\text{RESET}}$	$\overline{\text{CEOUT}}$
0	0	0	0	V_{BAT}	1	0	0	DIS
0	0	0	0	V_{BAT}	1	0	0	DIS
0	0	0	1	V_{BAT}	1	0	0	DIS
0	0	0	1	V_{BAT}	1	0	0	DIS
0	0	1	0	V_{DD}	0	0	0	DIS
0	0	1	0	V_{DD}	0	0	0	DIS
0	0	1	1	V_{BAT}	1	0	0	DIS
0	0	1	1	V_{BAT}	1	0	0	DIS
0	1	0	0	V_{DD}	0	0	1	DIS
0	1	0	0	V_{DD}	0	0	1	EN
0	1	0	1	V_{BAT}	1	0	1	DIS
0	1	0	1	V_{BAT}	1	0	1	EN
0	1	1	0	V_{DD}	0	0	1	DIS
0	1	1	0	V_{DD}	0	0	1	EN
0	1	1	1	V_{BAT}	1	0	1	DIS
0	1	1	1	V_{BAT}	1	0	1	EN
1	1	0	0	V_{DD}	0	1	1	DIS
1	1	0	0	V_{DD}	0	1	1	EN
1	1	0	1	V_{BAT}	1	1	1	DIS
1	1	0	1	V_{BAT}	1	1	1	EN
1	1	1	0	V_{DD}	0	1	1	DIS
1	1	1	0	V_{DD}	0	1	1	EN
1	1	1	1	V_{BAT}	1	1	1	DIS
1	1	1	1	V_{BAT}	1	1	1	EN

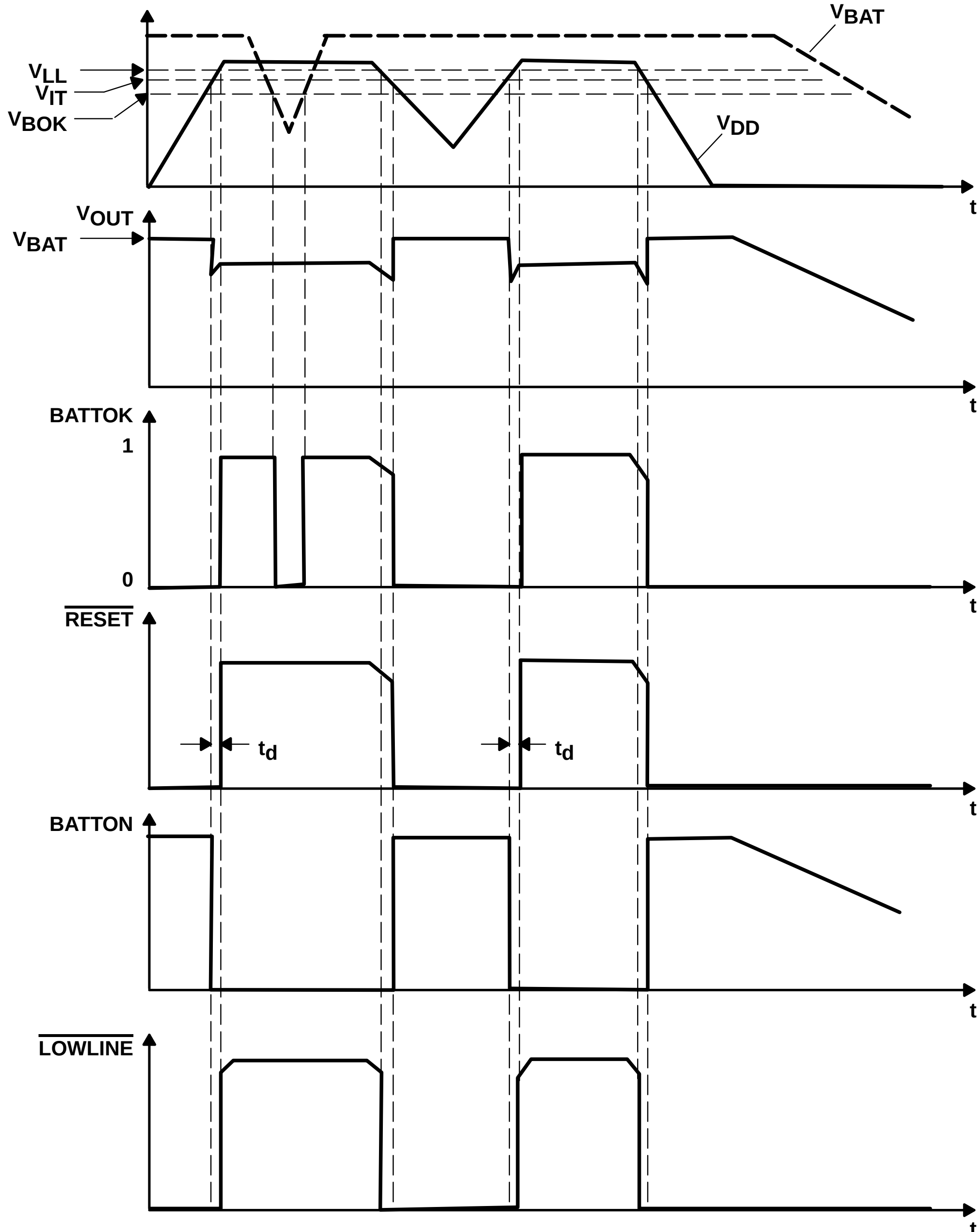
BATTOK		POWER-FAIL		CHIP-ENABLE	
$V_{BAT} > V_{BOK}$	BATTOK	$PFI > V_{(PFI)}$	$\overline{\text{PFO}}$	$\overline{\text{CEIN}}$	$\overline{\text{CEOUT}}$
0	0	0	0	0	0
1	1	1	1	1	1

Condition: $V_{DD} > V_{IT}$ Condition: $V_{DD} > V_{DD}min$ Condition: Enabled

functional block diagram



timing diagram



† MSWITCH = 0
Timing diagram shown under operation, not in freshness seal mode.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BATTOK	9	O	Battery status output
BATTON	6	O	Logic output/external bypass switch driver output
$\overline{\text{CEIN}}$	5	I	Chip-enable input
$\overline{\text{CEOUT}}$	10	O	Chip-enable output
GND	3	I	Ground
$\overline{\text{LOWLINE}}$	11	O	Early power-fail warning output
MSWITCH	4	I	Manual switch to force device into battery-backup mode
V_{OUT}	1	O	Supply output
PFI	7	I	Power-fail comparator input
$\overline{\text{PFO}}$	8	O	Power-fail comparator output
$\overline{\text{RESET}}$	13	O	Active-low reset output
V_{BAT}	14	I	Backup-battery input
V_{DD}	2	I	Input supply voltage
WDI	12	I	Watchdog timer input

detailed description

battery freshness seal

The battery freshness seal of the TPS3610 family disconnects the backup battery from internal circuitry until it is needed. This function ensures that the backup battery connected to V_{BAT} is fresh when the final product is put to use. The following steps explain how to enable the freshness seal mode:

1. Connect V_{BAT} ($V_{BAT} > V_{BAT}$min)
2. Ground $\overline{\text{PFO}}$
3. Connect PFI to V_{DD} (PFI = V_{DD})
4. Connect V_{DD} to power supply ($V_{DD} > V_{IT}$) and keep connected for 5 ms < t < 35 ms

The battery freshness seal mode is disabled by the positive-going edge of $\overline{\text{RESET}}$ when V_{DD} is applied.

BATTOK output

BATTOK is a logic feedback of the device to indicate the status of the backup battery. The supervisor checks the battery voltage every 200 ms with a voltage divider load of approximately 100 kΩ and a measurement cycle on-time of 25 µs. The measurement cycle starts after the reset is released. If the battery voltage V_{BAT} is below the negative-going threshold voltage $V_{IT(BOK)}$, the indicator BATTOK does a high-to-low transition. Otherwise it retains its status to V_{DD} level.

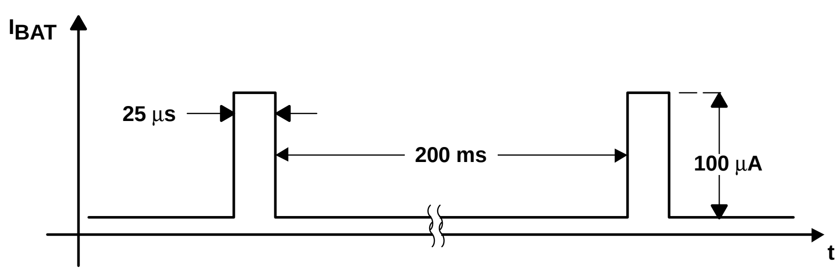


Figure 1. BATTOK Timing

detailed description (continued)

chip-enable signal gating

The internal gating of chip-enable signals, CE, prevents erroneous data from corrupting CMOS RAM during an undervoltage condition. The TPS3610 use a series transmission gate from $\overline{\text{CEIN}}$ to $\overline{\text{CEOUT}}$. During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from $\overline{\text{CEIN}}$ to $\overline{\text{CEOUT}}$ enables TPS3610 devices to be used with most processors.

The CE transmission gate is disabled and $\overline{\text{CEIN}}$ is high-impedance (disable mode) while reset is asserted. During a power-down sequence, when V_{DD} crosses the reset threshold, the CE transmission gate is disabled and $\overline{\text{CEIN}}$ immediately becomes high impedance if the voltage at $\overline{\text{CEIN}}$ is high. If $\overline{\text{CEIN}}$ is low while reset is asserted, the CE transmission gate is disabled at the same time $\overline{\text{CEIN}}$ goes high, or 15 µs after $\overline{\text{RESET}}$ asserts, whichever occurs first. This allows the current write cycle to complete during power-down. When the CE transmission gate is enabled, the impedance of $\overline{\text{CEIN}}$ appears as a resistor in series with the load at $\overline{\text{CEOUT}}$. The overall device propagation delay through the CE transmission gate depends on V_{OUT}, the source impedance of the device connected to $\overline{\text{CEIN}}$ and the load at $\overline{\text{CEOUT}}$. To achieve minimum propagation delay, the capacitive load at $\overline{\text{CEOUT}}$ should be minimized, and a low-output-impedance driver should be used.

During disable mode, the transmission gate is off and an active pullup connects $\overline{\text{CEOUT}}$ to V_{OUT}. The pullup turns off when the transmission gate is enabled.

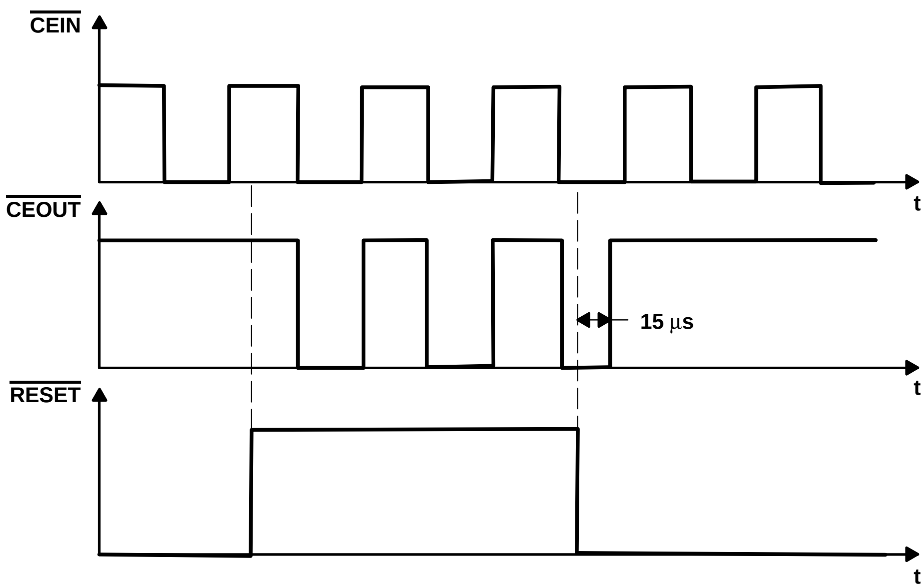


Figure 2. Chip-Enable Timing

detailed description (continued)

power-fail comparator (PFI and $\overline{\text{PFO}}$)

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail-input (PFI) is compared with an internal voltage reference of 1.15 V. If the input voltage falls below the power-fail threshold $V_{IT(PFI)}$ of typical 1.15 V, the power-fail output ($\overline{\text{PFO}}$) goes low. If $V_{IT(PFI)}$ goes above $V_{(PFI)}$, plus about 12-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above $V_{(PFI)}$. The sum of both resistors should be about 1 MΩ, to minimize power consumption and also to assure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, PFI should be connected to ground and $\overline{\text{PFO}}$ left unconnected.

$\overline{\text{LOWLINE}}$

The lowline comparator monitors V_{DD} with a threshold voltage typically 2% above the reset threshold (V_{IT}). For normal operation (V_{DD} above the reset threshold), $\overline{\text{LOWLINE}}$ is pulled to V_{DD}. $\overline{\text{LOWLINE}}$ can be used to provide a nonmaskable interrupt (NMI) to the processor when power begins to fall. In most battery-operated portable systems, reserve energy in the battery provides enough time to complete the shutdown routine once the low-line warning is encountered and before reset asserts. If the system must also contend with a more rapid V_{DD} fall time, such as when the main battery is disconnected or a high-side switch is opened during normal operation, a capacitor can be used on the V_{DD} line to provide enough time for executing the shutdown routine. First, the worst-case settling time (t_{sd}) required for the system to perform its shutdown routine needs to be defined. Then, using the worst-case load current (I_L) that can be drained from the capacitor, and the minimum reset threshold voltage (V_{IT}min), the capacitor value (C_H) can be calculated as follows:

$$C_H = \frac{I_L \times t_{sd}}{V_{IT}\text{min} \times 0.012}$$

BATTON

Most often BATTON is used as a gate drive for an external pass transistor for high-current applications. In addition, it can be used as a logic output to indicate the battery switchover status. BATTON is high when V_{OUT} is connected to V_{BAT}.

BATTON can be connected directly to the gate of a PMOS transistor (see Figure 3). No current-limiting resistor is required. If a PMOS transistor is used, it must be connected in the reverse of the traditional method (see Figure 3), which orients the body diode from V_{DD} to V_{OUT} and prevents the backup battery from discharging through the FET when its gate is high.

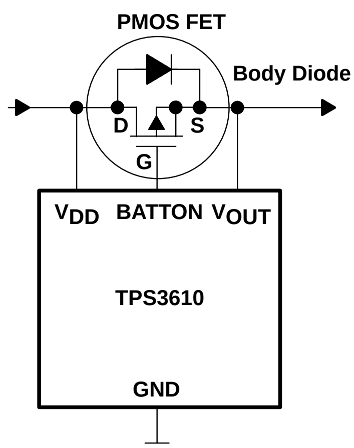


Figure 3. Driving an External MOSFET Transistor With BATTON

detailed description (continued)

backup-battery switchover

In case of a brownout or power failure, it may be necessary to preserve the contents of RAM. If a backup-battery is installed at V_{BAT}, the device automatically switches the connected RAM to backup power when V_{DD} fails. In order to allow the backup-battery (e.g., a 3.6-V lithium cell) to have a higher voltage than V_{DD}, these supervisors do not connect V_{BAT} to V_{OUT} when V_{BAT} is greater than V_{DD}. V_{BAT} only connects to V_{OUT} (through a 15-Ω switch) when V_{DD} falls below V_{IT} *and* V_{BAT} is greater than V_{DD}. When V_{DD} recovers, switchover is deferred either until V_{DD} crosses V_{BAT}, or until V_{DD} rises above the reset threshold V_{IT}. V_{OUT} connects to V_{DD} through a 1-Ω (max) PMOS switch when V_{DD} crosses the reset threshold.

FUNCTION TABLE

$V_{DD} > V_{BAT}$	$V_{DD} > V_{IT}$	V_{OUT}
1	1	V_{DD}
1	0	V_{DD}
0	1	V_{DD}
0	0	V_{BAT}

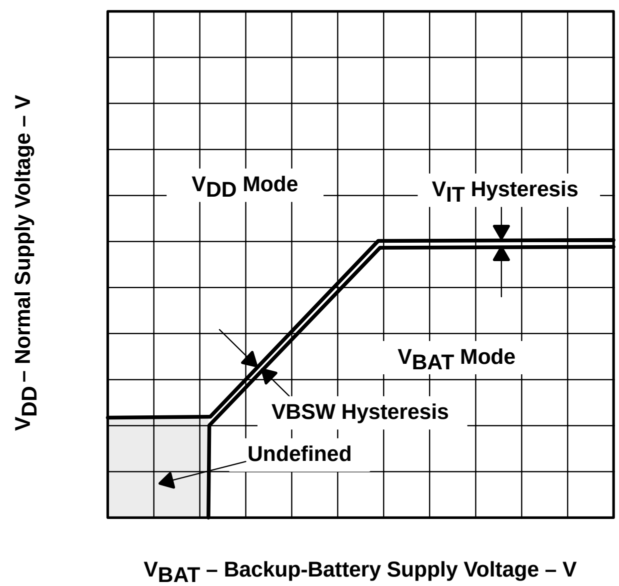


Figure 4. Normal Supply Voltage vs Backup-Battery Supply Voltage

detailed description (continued)

manual switchover (MSWITCH)

While operating in the normal mode from V_{DD}, the device can be forced manually to operate in battery-backup mode by connecting MSWITCH to V_{DD}. Refer to Table 1 for different switchover modes.

Table 1. Switchover Modes

	MSWITCH	STATUS
V_{DD} mode	GND	V_{DD} mode
	V_{DD}	Switch to battery-backup mode
Battery-backup mode	GND	Battery-backup mode
	V_{DD}	Battery-backup mode

If the manual switchover feature is not used, MSWITCH *must* be connected to ground.

watchdog

In a microprocessor- or DSP-based system, it is important not only to supervise the supply voltage, but also to ensure correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller or DSP has to toggle the watchdog input within typically 0.8 s to avoid the occurence of a time-out. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected, the watchdog is disabled and is retriggered internally.

saving current while using the watchdog

The watchdog input is internally driven low during the first 7/8 of the watchdog time-out period, then the input momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), WDI should be left low for the majority of the watchdog time-out period, and pulsed low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If instead WDI is externally driven high for the majority of the timeout period, a current of, e.g., 5 V/40 kΩ ≈ 125 µA, can flow into WDI.

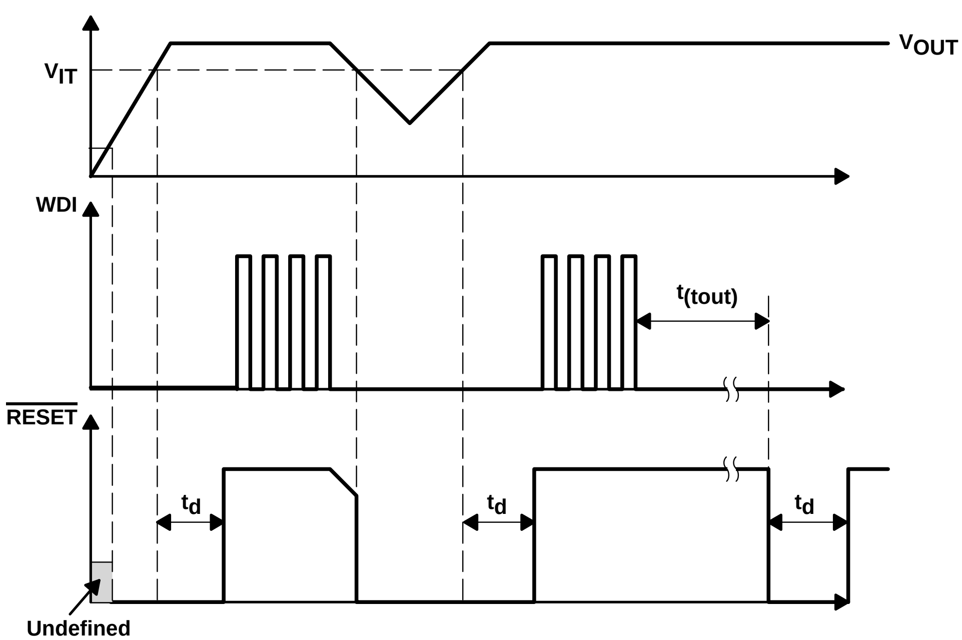


Figure 5. Watchdog Timing

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 2) . . . . 7 V
All other pins (see Note 2) . . . . –0.3 V to 7 V
Continuous output current at V_{OUT}, $I_{O(VOUT)}$ . . . . 400 mA
Continuous output current (all other pins) I_O . . . . ±10 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t=1000h continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PW	700 mW	5.6 mW/°C	448 mW	364 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.65	5.5	V
Battery supply voltage, V_{BAT}	1.5	5.5	V
Input voltage, V_I	0	V_{DD}+0.3	V
High-level input voltage, V_{IH}	0.7xV_{DD}		V
Low-level input voltage, V_{IL}		0.3×V_{DD}	V
Continuous output current at V_{OUT}, I_O		300	mA
Input transition rise and fall rate at WDI, MSWITCH, Δt/ΔV		100	ns/V
Slew rate at V_{DD} or V_{BAT}		1	V/µs
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{RESET}$, BATTOK	V_{DD} = 1.8 V,	I_{OH} = –400 µA	V_{DD}–0.2 V			V
			V_{DD} = 3.3 V,	I_{OH} = –2 mA	V_{DD}–0.4 V			
			V_{DD} = 5 V,	I_{OH} = –3 mA				
		BATTON	V_{OUT} = 1.8 V,	I_{OH} = –400 µA	V_{OUT}–0.2 V			
			V_{OUT} = 3.3 V,	I_{OH} = –2 mA	V_{OUT}–0.4 V			
			V_{OUT} = 5 V,	I_{OH} = –3 mA				
		$\overline{LOWLINE}$, $\overline{PFO}$	V_{DD} = 1.8 V,	I_{OH} = –20 µA	V_{DD}–0.3 V			
			V_{DD} = 3.3 V,	I_{OH} = –80 µA,	V_{DD}–0.4 V			
			V_{DD} = 5 V,	I_{OH} = –120 µA				
		$\overline{CEOUT}$, Enable mode, $\overline{CEIN}$ = V_{OUT}	V_{OUT} = 1.8 V,	I_{OH} = –1 mA	V_{OUT}–0.2 V			
			V_{OUT} = 3.3 V,	I_{OH} = –2 mA	V_{OUT}–0.3 V			
			V_{OUT} = 5 V,	I_{OH} = –5 mA				
		$\overline{CEOUT}$, Disable mode	V_{OUT} = 3.3 V,	I_{OH} = –0.5 mA	V_{OUT}–0.4 V			
V_{OL}	Low-level output voltage	$\overline{RESET}$, $\overline{PFO}$, BATTOK, $\overline{LOWLINE}$	V_{DD} = 1.8 V,	I_{OL} = 400 µA			0.2	V
			V_{DD} = 3.3 V,	I_{OL} = 2 mA			0.4	
			V_{DD} = 5 V,	I_{OL} = 3 mA				
		BATTON	V_{OUT} = 1.8 V,	I_{OL} = 500 µA			0.2	
			V_{OUT} = 3.3 V,	I_{OL} = 3 mA			0.4	
			V_{OUT} = 5 V,	I_{OL} = 5 mA				
		$\overline{CEOUT}$, Enable mode, $\overline{CEIN}$ = 0 V	V_{OUT} = 1.8 V,	I_{OL} = 1 mA			0.2	
			V_{OUT} = 3.3 V,	I_{OL} = 2 mA			0.3	
			V_{OUT} = 5 V,	I_{OL} = 5 mA				
	Power-up reset voltage (see Note 3)		I_{OL} = 20 µA,	V_{BAT} > 1.1 V, OR V_{DD} > 1.1 V,			0.4	V
V_{OUT}	Normal mode		I_O = 8.5 mA, V_{BAT} = 0 V	V_{DD} = 1.8 V,	V_{DD}–50 mV			V
			I_O = 125 mA, V_{BAT} = 0 V	V_{DD} = 3.3 V,	V_{DD}–150 mV			
			I_O = 200 mA, V_{BAT} = 0 V	V_{DD} = 5 V,	V_{DD}–200 mV			
	Battery-backup mode		I_O = 0.5 mA, V_{BAT} = 1.5 V	V_{DD} = 0 V,	V_{BAT}–20 mV			
			I_O = 7.5 mA, V_{BAT} = 3.3 V	V_{DD} = 0 V,	V_{BAT}–113 mV			

NOTE 3: The lowest supply voltage at which $\overline{RESET}$ becomes active. $t_{r,}$ V_{DD} ≥ 15 µs/V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT}	Negative-going input threshold voltage (see Note 4)	TPS3610U18	T_A = –40°C to 85°C		1.68	1.71	1.74	V
		TPS3610T50			4.46	4.55	4.64	
$V_{(PFI)}$		PFI			1.13	1.15	1.17	
$V_{(BOK)}$		TPS3610T50			2.33	2.4	2.47	
		TPS3610U18			1.55	1.6	1.65	
$V_{(LL)}$		$\overline{\text{LOWLINE}}$			V_{IT}+1.2%	V_{IT}+2%	V_{IT}+2.8%	V
V_{hys}	Hysteresis	V_{IT}	1.65 V < V_{IT} < 2.5 V			20		mV
			2.5 V < V_{IT} < 3.5 V			40		
			3.5 V < V_{IT} < 5.5 V			60		
		$\overline{\text{LOWLINE}}$	1.65 V < $V_{(LL)}$ < 2.5 V			20		
			2.5 V < $V_{(LL)}$ < 3.5 V			40		
			3.5 V < $V_{(LL)}$ < 5.5 V			60		
		BATTOK	1.65 V < $V_{(BOK)}$ < 2.5 V			20		
			2.5 V < $V_{(BOK)}$ < 3.5 V			40		
			3.5 V < $V_{(BOK)}$< 5.5 V			60		
		PFI				12		
		V_{BSW} (see Note 5)	V_{DD} = 1.8 V			55		
I_{IH}	High-level input current	WDI (see Note 6)	WDI = V_{DD} = 5 V				150	µA
I_{IL}	Low-level input current		WDI = 0 V,	V_{DD} = 5 V			–150	
I_I	Input current	PFI, MSWITCH			–25		25	nA
I_{OS}	Short-circuit output current	$\overline{\text{PFO}}$	$\overline{\text{PFO}}$ = 0 V	V_{DD} = 1.8 V			–0.3	mA
				V_{DD} = 3.3 V			–1.1	
				V_{DD} = 5 V			–2.4	
I_{DD}	Supply current at V_{DD}		V_{OUT} = V_{DD}				40	µA
			V_{OUT} = V_{BAT}				40	
I_{BAT}	Supply current at V_{BAT}		V_{OUT} = V_{DD}		–0.1		0.1	µA
			V_{OUT} = V_{BAT}				0.5	
I_{lkg}	Leakage current at $\overline{\text{CEIN}}$		Disable mode,	V_I < V_{DD}			±1	µA
$r_{DS(on)}$	V_{DD} to V_{OUT} on-resistance		V_{DD} = 5 V			0.6	1	Ω
	V_{BAT} to V_{OUT} on-resistance		V_{BAT} = 3.3 V			8	15	
C_i	Input capacitance		V_I = 0 V to 5 V			5		pF

NOTES: 4. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near to the supply terminals.
5. For V_{DD} < 1.6 V, V_{OUT} switches to V_{BAT} regardless of V_{BAT}
6. For details on how to optimize current consumption when using WDI. Refer to detailed description section, *watchdog*.

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	At V_{DD}	$V_{IH} = V_{IT}$ + 0.2 V, $V_{IL} = V_{IT}$ –0.2 V	6			µs
		At WDI	$V_{DD} = V_{IT}$ + 0.2 V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	100			ns

switching characteristics at R_L = 1 MΩ, C_L = 50 pF, T_A =–40°C to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{DD} > V_{IT}$ +0.2 V (see timing diagram	60	100	140	ms
$t_{(tout)}$	Watchdog timeout			0.48	0.8	1.12	s
t_{PLH}	Propagation (delay) time, low-to-high-level output	50% $\overline{RESET}$ to 50% $\overline{CEOUT}$			15		µs
t_{PHL}	Propagation (delay) time, high-to-low-level output	50% $\overline{CEIN}$ to 50% $\overline{CEOUT}$, C_L = 50 pF only (see Note 7)	V_{DD} = 1.8 V		5	15	ns
			V_{DD} = 3.3 V		1.6	5	
			V_{DD} = 5 V		1	3	
		V_{DD} to $\overline{RESET}$	$V_{IL} = V_{IT}$–0.2 V, $V_{IH} = V_{IT}$+0.2 V		2	5	µs
		PFI to $\overline{PFO}$	$V_{IL} = V_{(PFI)}$–0.2 V, $V_{IH} = V_{(PFI)}$+0.2 V		3	5	
t_t	Transition time	V_{DD} to BATTON	$V_{IH} = V_{BAT}$ + 200 mV, $V_{IL} = V_{BAT}$ – 200 mV, $V_{BAT} < V_{IT}$			3	µs

NOTE 7: Specified by design

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$r_{DS(on)}$	Static drain-source on-state resistance (V_{DD} to V_{OUT})	vs Output current	6
	Static drain-source on-state resistance (V_{BAT} to V_{OUT})		7
	Static drain-source on-state resistance	vs Input voltage at $\overline{CEIN}$	8
I_{DD}	Supply current	vs Supply voltage	9
V_{IT}	Normalized threshold at $\overline{RESET}$	vs Free-air temperature	10
V_{OH}	High-level output voltage at $\overline{RESET}$	vs High-level output current	11, 12
	High-level output voltage at $\overline{PFO}$		13, 14
	High-level output voltage at $\overline{CEOUT}$		15, 16, 17, 18
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	Low-level output voltage at BATTON		23, 24
$t_{p(min)}$	Minimum Pulse Duration at V_{DD}	vs Threshold overdrive at V_{DD}	25
$t_{p(min)}$	Minimum Pulse Duration at PFI	vs Threshold overdrive at PFI	26

TYPICAL CHARACTERISTICS

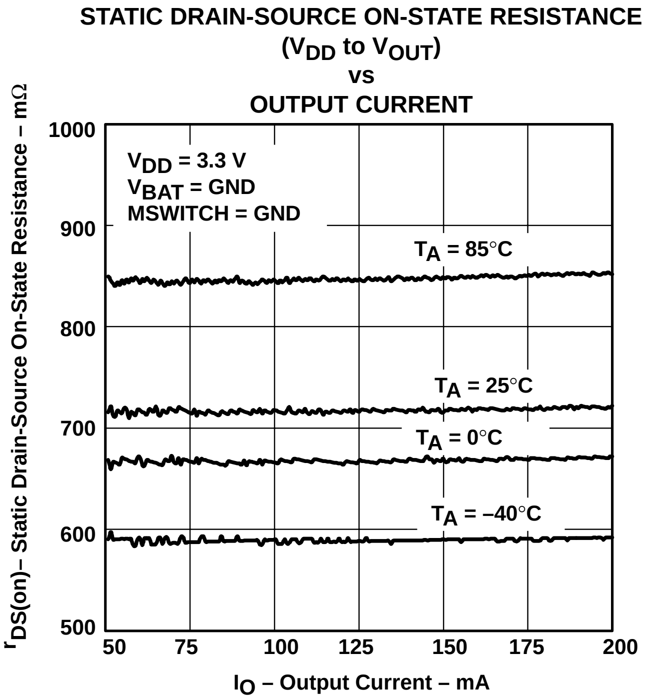


Figure 6

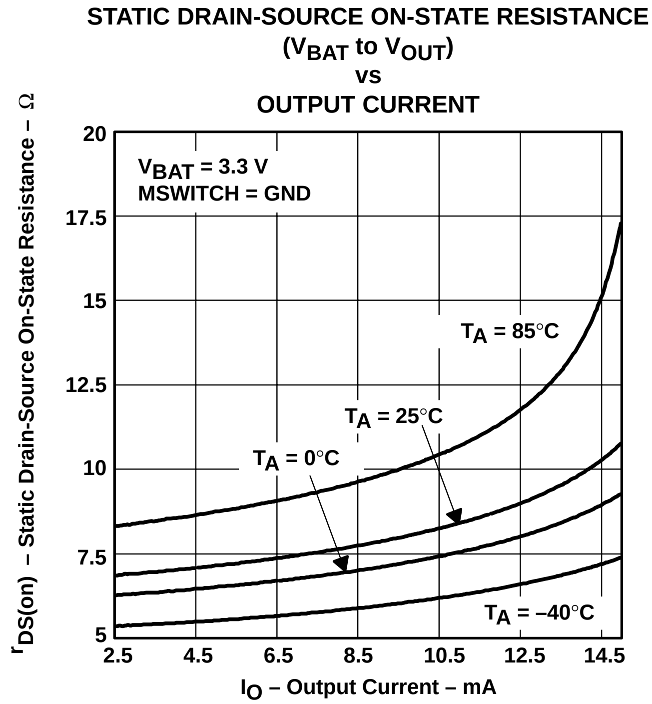


Figure 7

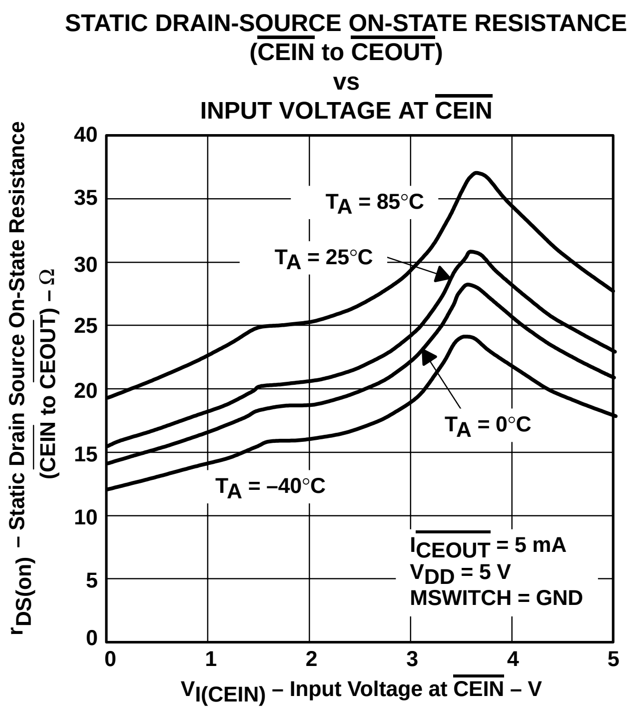


Figure 8

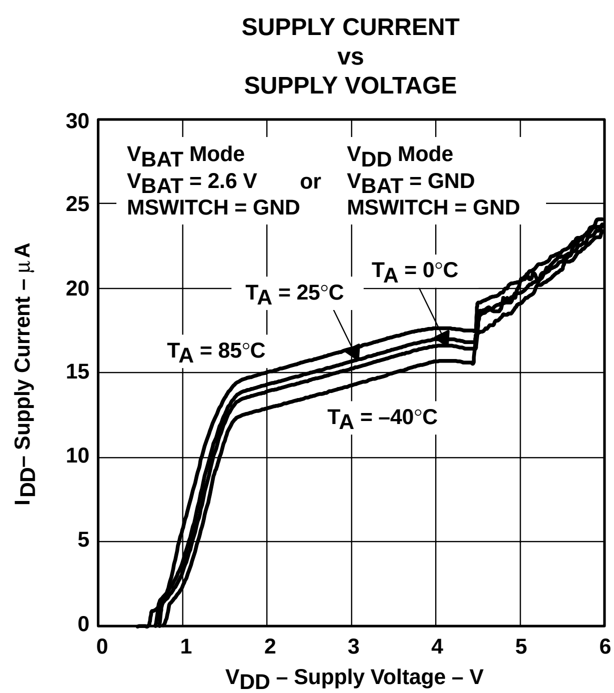


Figure 9

TYPICAL CHARACTERISTICS

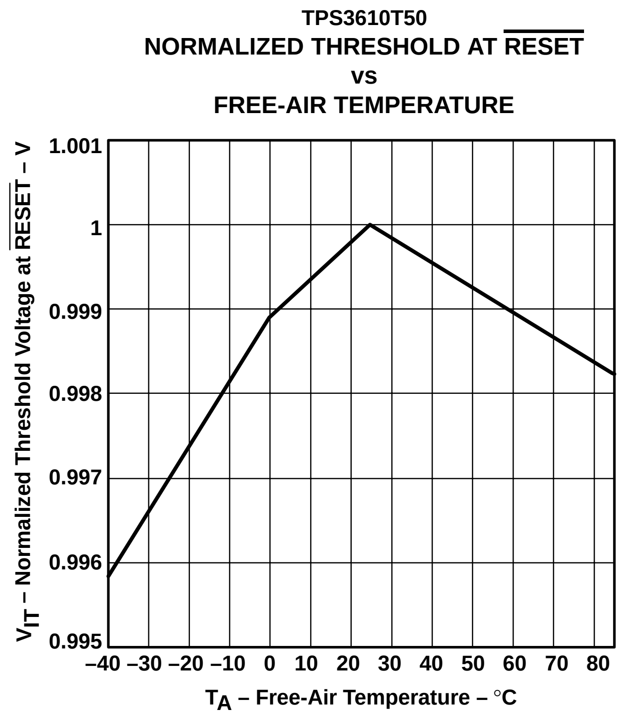


Figure 10

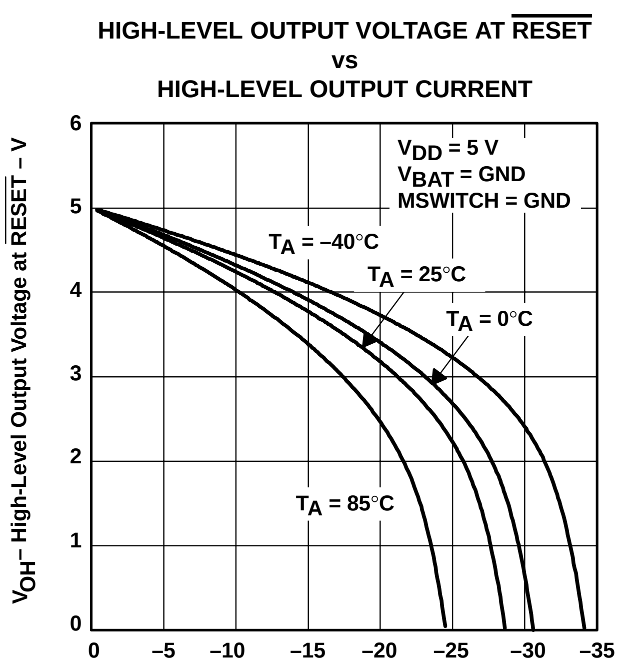


Figure 11

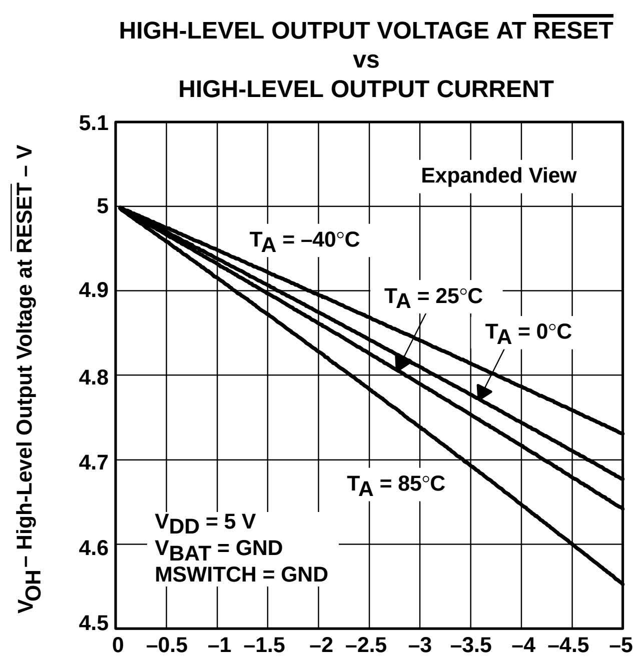


Figure 12

TYPICAL CHARACTERISTICS

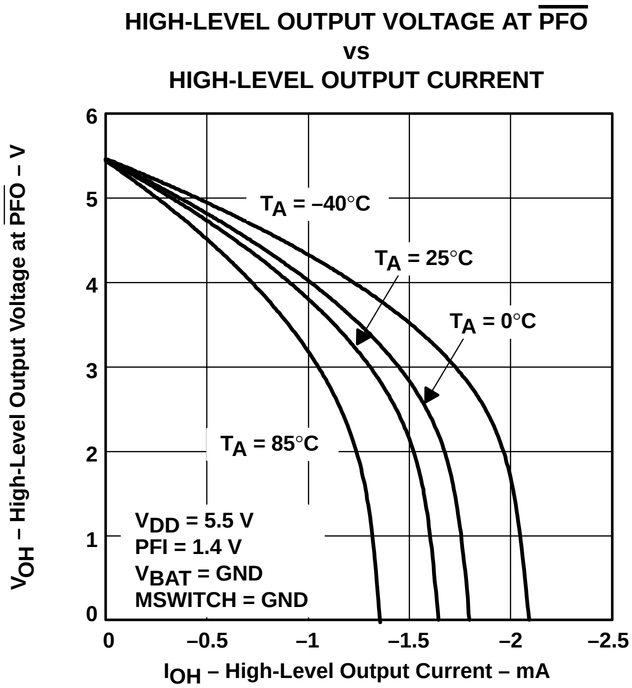


Figure 13

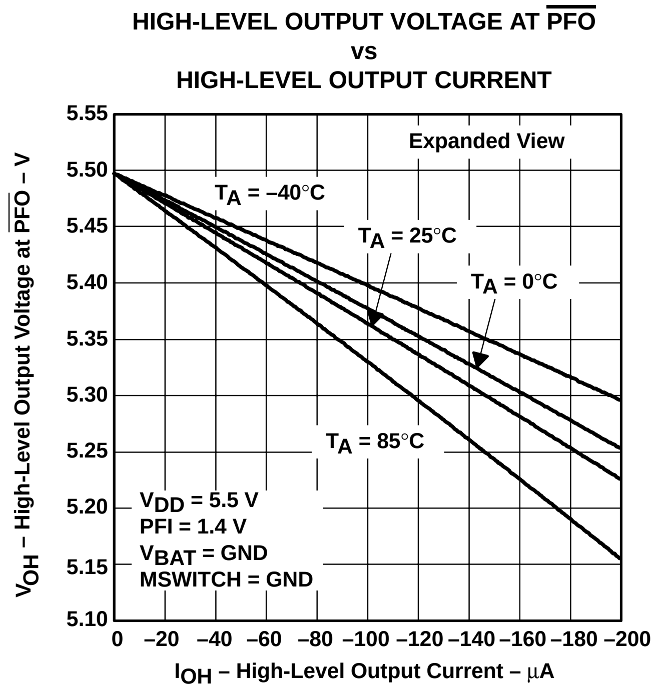


Figure 14

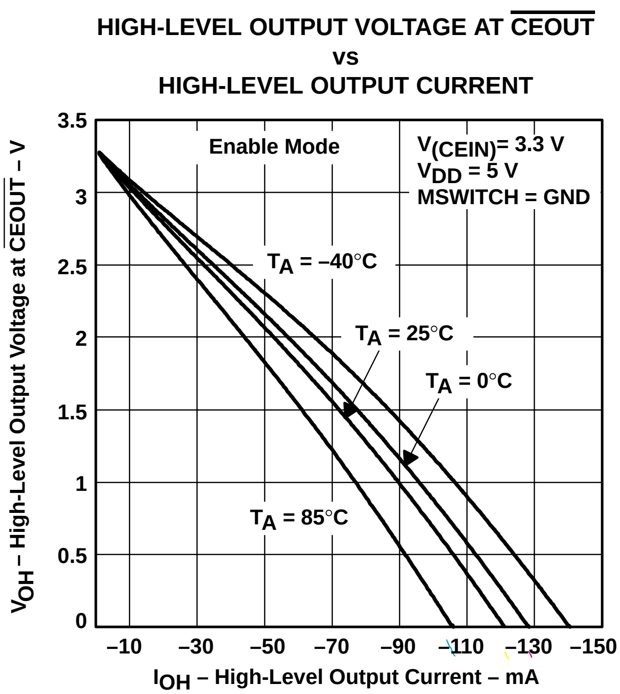


Figure 15

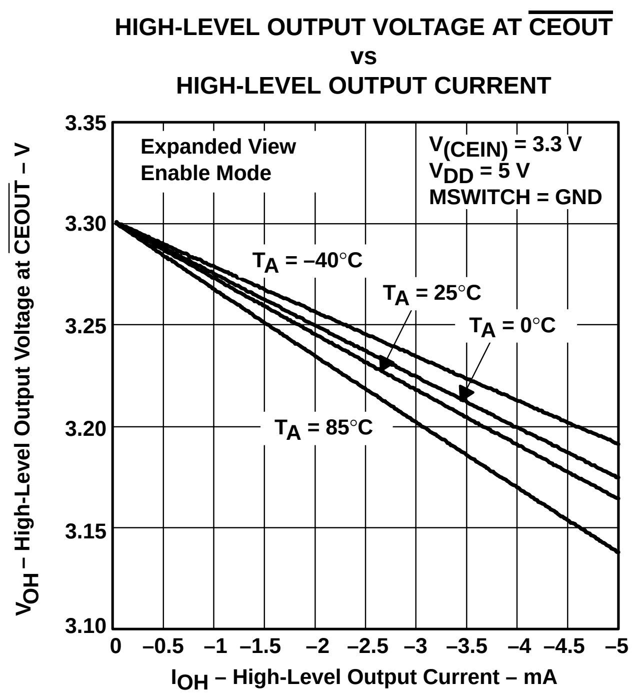


Figure 16

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{CEOUT}}$
vs
HIGH-LEVEL OUTPUT CURRENT

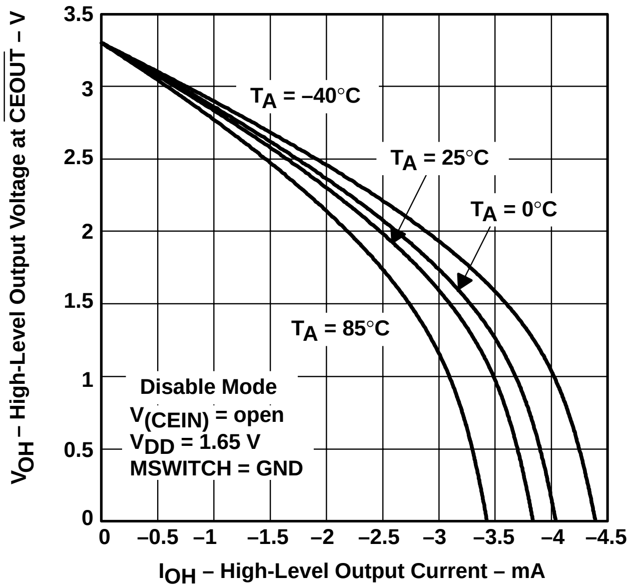


Figure 17

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{CEOUT}}$
vs
HIGH-LEVEL OUTPUT CURRENT

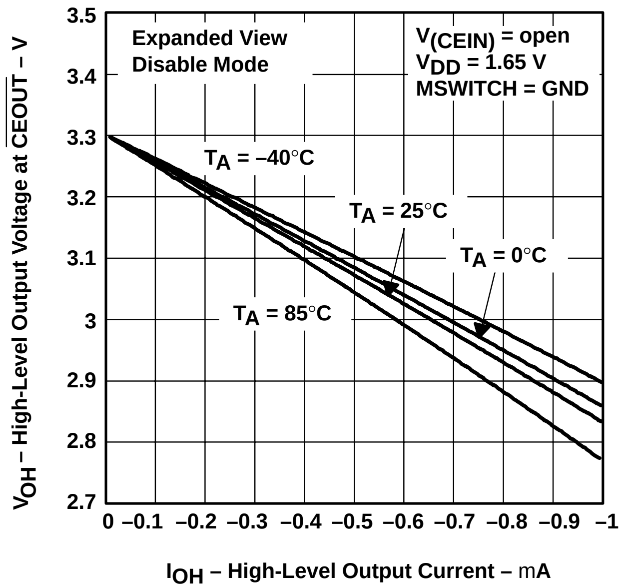


Figure 18

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$
vs
LOW-LEVEL OUTPUT CURRENT

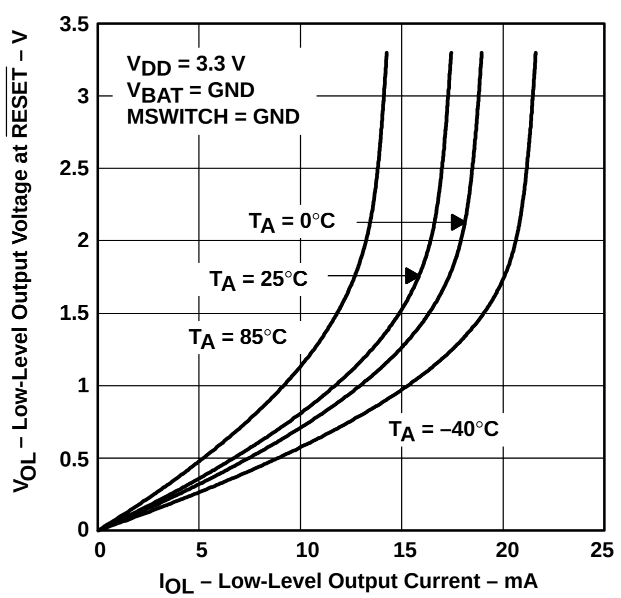


Figure 19

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$
vs
LOW-LEVEL OUTPUT CURRENT

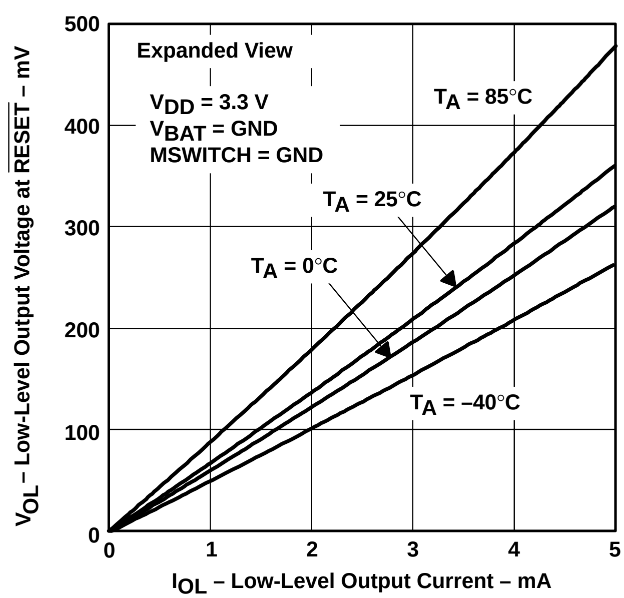


Figure 20

TYPICAL CHARACTERISTICS

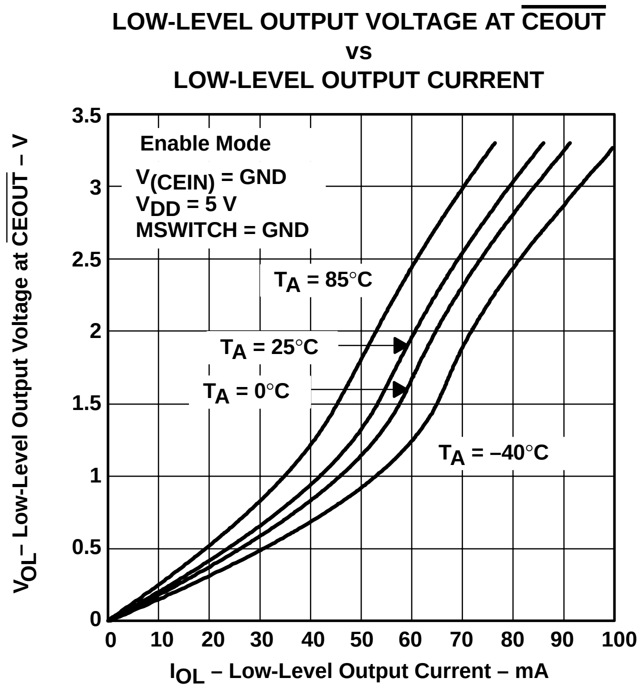


Figure 21

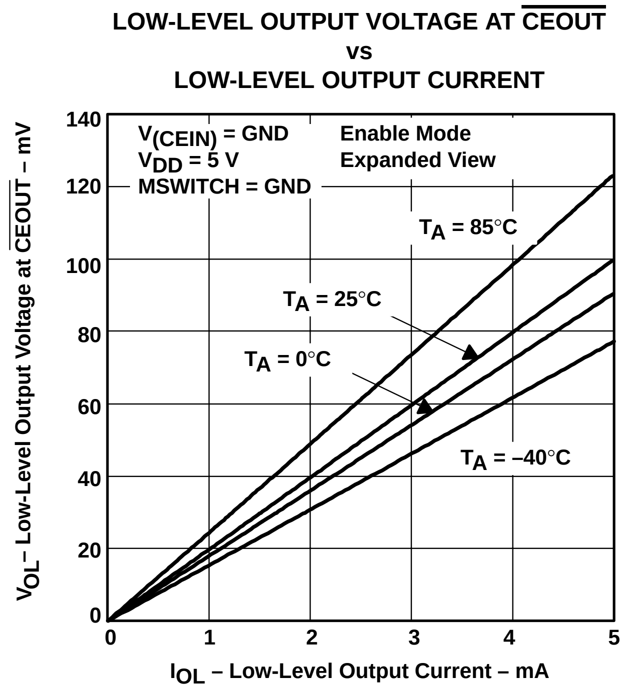


Figure 22

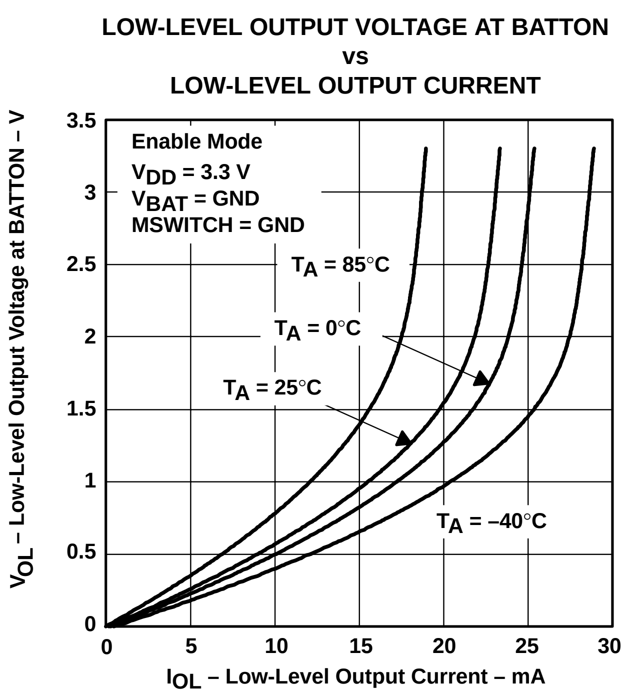


Figure 23

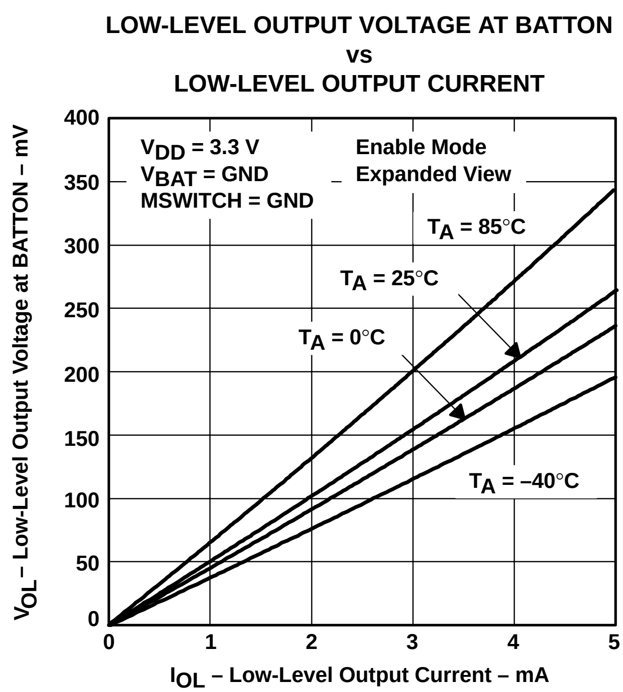


Figure 24

TYPICAL CHARACTERISTICS

TPS3610T50
MINIMUM PULSE DURATION AT V_{DD}
vs
THRESHOLD OVERDRIVE AT V_{DD}

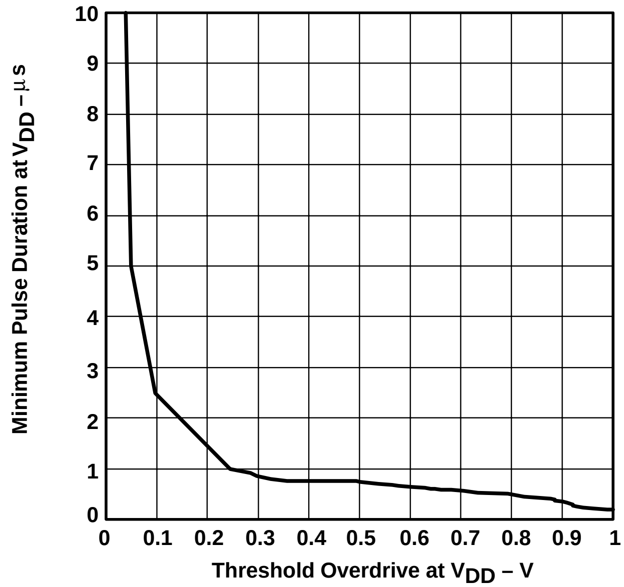


Figure 25

TPS3610T50
MINIMUM PULSE DURATION AT PFI
vs
THRESHOLD OVERDRIVE AT PFI

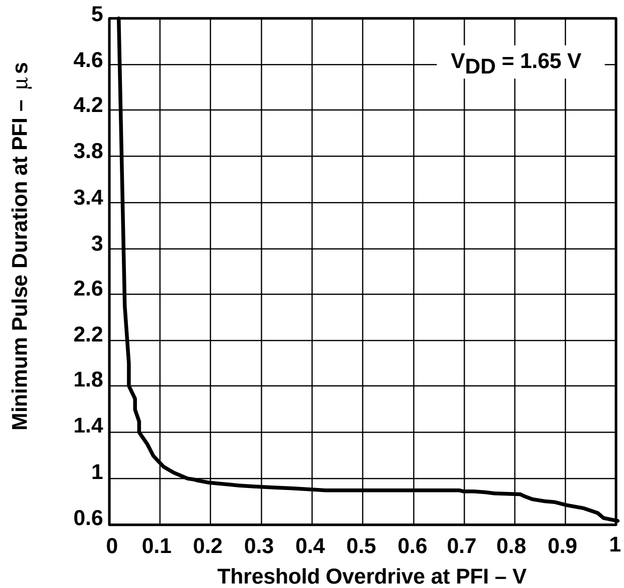
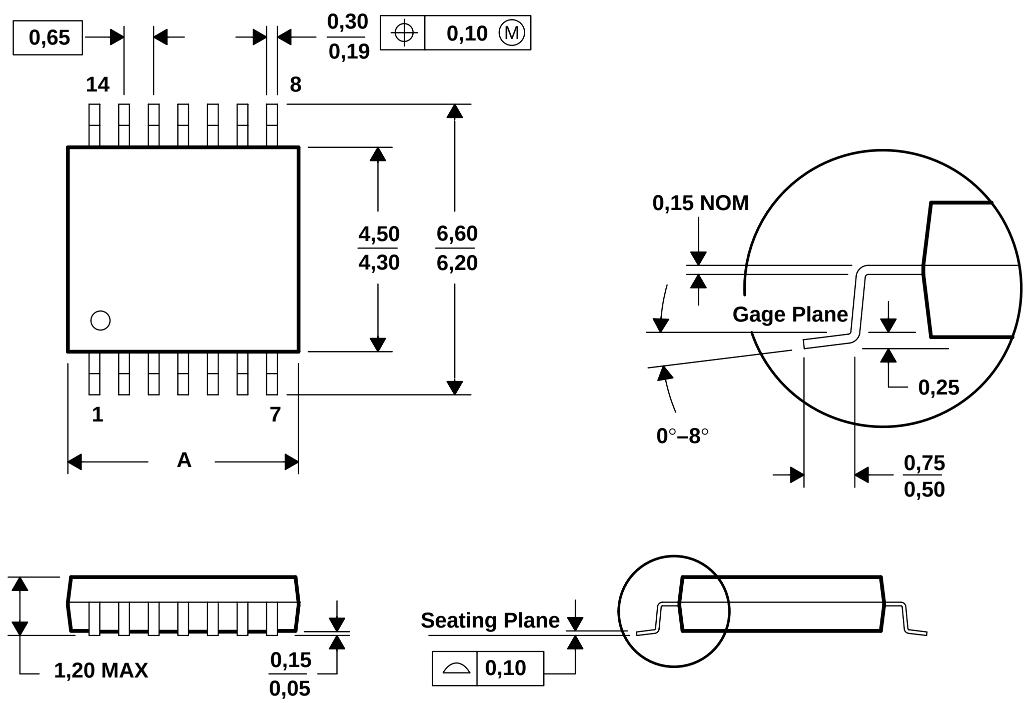


Figure 26

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

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