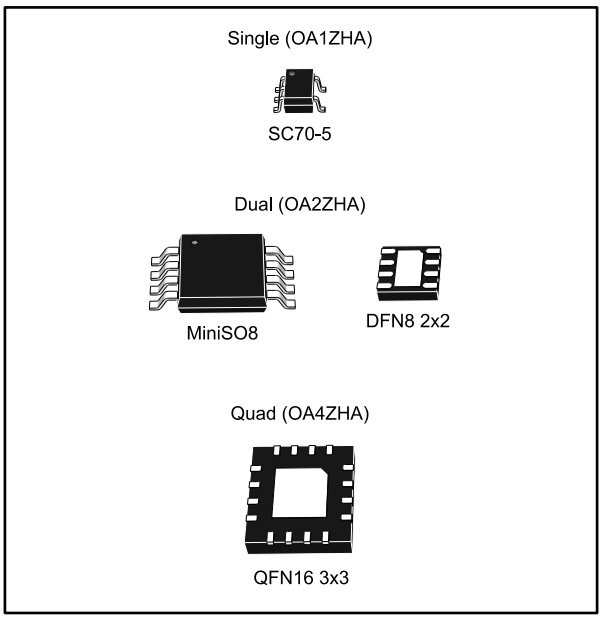
OA1ZHA, OA2ZHA, OA4ZHA

High precision 5 µV zero drift, low-power op amps

Datasheet - production data



Features

- Very high accuracy and stability: offset voltage 5 µV max at 25 °C, 8 µV over full temperature range (-40 °C to 125 °C)
- Rail-to-rail input and output
- Low supply voltage: 1.8 - 5.5 V
- Low power consumption: 40 µA max. at 5 V
- Gain bandwidth product: 400 kHz
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 to 125 °C
- Micro-packages: SC70-5, DFN8 2x2, and QFN16 3x3

Benefits

- High precision operational amplifiers (op amps) with no need for calibration
- Accuracy virtually unaffected by temperature change

Applications

- Wearable
- Fitness and healthcare
- Medical instrumentation

Description

The OA1ZHA, OA2ZHA, OA4ZHA series of low-power, high-precision op amps offers very low input offset voltages with virtually zero drift.

OA1ZHA, OA2ZHA, OA4ZHA are respectively the single, dual and quad op amp versions, with pinout compatible with industry standards.

The OA1ZHA, OA2ZHA, OA4ZHA series offers rail-to-rail input and output, excellent speed/power consumption ratio, and 400 kHz gain bandwidth product, while consuming less than 40 µA at 5 V. All devices also feature an ultra-low input bias current.

The OA1ZHA, OA2ZHA, OA4ZHA family is the ideal choice for wearable, fitness and healthcare applications.

This is information on a product in full production.

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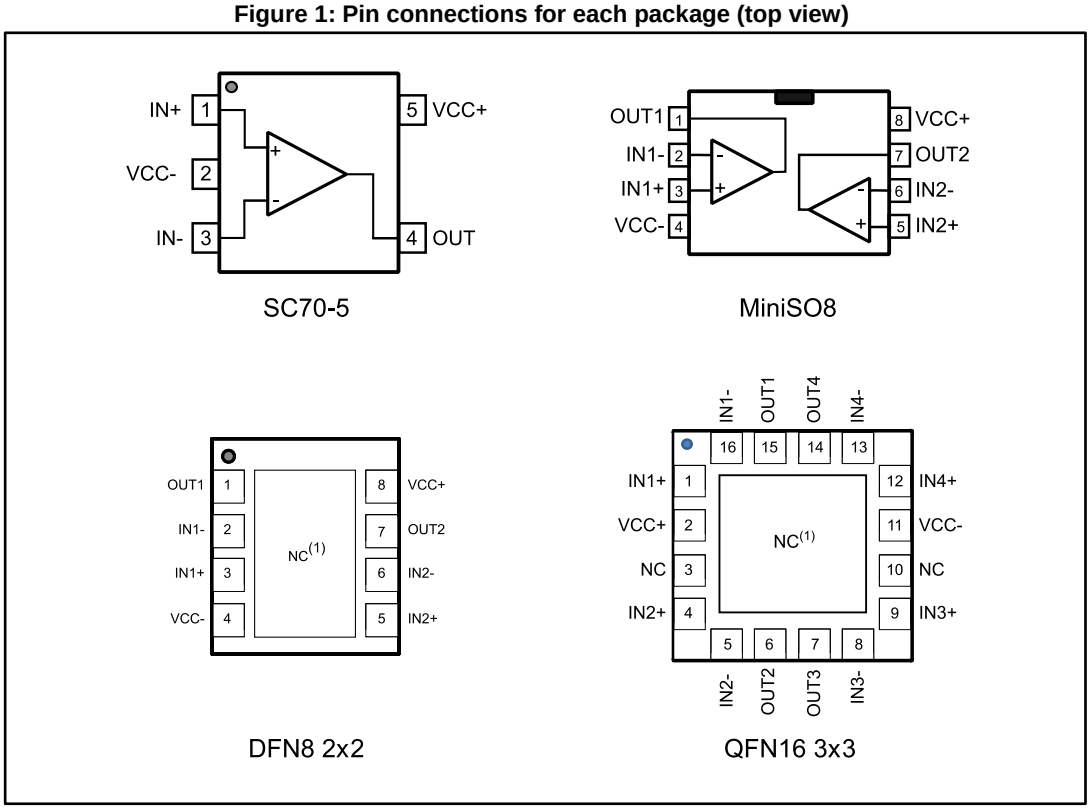
1 Package pin connections

Figure 1: Pin connections for each package (top view)



1. The exposed pads of the DFN8 2x2 and the QFN16 3x3 can be connected to VCC- or left floating.

2 Absolute maximum ratings and operating conditions

Table 1: Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		6	V
V_{id}	Differential input voltage (2)		$\pm V_{CC}$	
V_{in}	Input voltage (3)		(V_{CC-}) - 0.2 to (V_{CC+}) + 0.2	
I_{in}	Input current (4)		10	mA
T_{stg}	Storage temperature		-65 to 150	°C
T_j	Maximum junction temperature		150	
R_{thja}	Thermal resistance junction-to-ambient (5)(6)	SC70-5	205	°C/W
		MiniSO8	190	
		DFN8 2x2	57	
		QFN16 3x3	39	
ESD	HBM: human body model (7)	OA1ZHA only	4	kV
	MM: machine model (8)		300	V
	CDM: charged device model		1.5	kV
		QFN16 3x3	TBD	
	Latch-up immunity		200	mA

Notes:

(1)All voltage values, except differential voltage, are with respect to network ground terminal.

(2)The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.

(3)V_{CC} - V_{in} must not exceed 6 V, V_{in} must not exceed 6 V.

(4)Input current must be limited by a resistor in series with the inputs.

(5)R_{th} are typical values.

(6)Short-circuits can cause excessive heating and destructive dissipation.

(7)Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.

(8)Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.8 to 5.5	V
V_{icm}	Common mode input voltage range	(V_{CC-}) - 0.1 to (V_{CC+}) + 0.1	
T_{oper}	Operating free air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 3: Electrical characteristics at VCC+ = 1.8 V with VCC- = 0 V, Vicm = VCC/2, T = 25 ° C, and RL = 10 kΩ connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		1	5	µV
		-40 °C < T < 125 °C			8	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)	-40 °C < T < 125 °C		10	30	nV/°C
I_{ib}	Input bias current ($V_{out} = V_{CC}/2$)	T = 25 °C		50	200 (2)	pA
		-40 °C < T < 125 °C			300 (2)	
I_{io}	Input offset current ($V_{out} = V_{CC}/2$)	T = 25 °C		100	400 (2)	
		-40 °C < T < 125 °C			600 (2)	
CMR	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{ic} = 0 V to V_{CC}, $V_{out} = V_{CC}/2$, R_L > 1 MΩ	T = 25 °C	110	122		dB
		-40 °C < T < 125 °C	110			
A_{vd}	Large signal voltage gain, V_{out} = 0.5 V to (V_{CC} - 0.5 V)	T = 25 °C	118	135		
		-40 °C < T < 125 °C	110			
V_{OH}	High-level output voltage	T = 25 °C			30	mV
		-40 °C < T < 125 °C			70	
V_{OL}	Low-level output voltage	T = 25 °C			30	
		-40 °C < T < 125 °C			70	
I_{out}	I_{sink} ($V_{out} = V_{CC}$)	T = 25 °C	7	8		mA
		-40 °C < T < 125 °C	6			
	I_{source} (V_{out} = 0 V)	T = 25 °C	5	7		
		-40 °C < T < 125 °C	4			
I_{CC}	Supply current (per amplifier), $V_{out} = V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C		28	40	µA
		-40 °C < T < 125 °C			40	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		400		kHz
F_u	Unity gain frequency			300		
ϕm	Phase margin			55		Degrees
G_m	Gain margin			17		dB
SR	Slew rate (3)			0.17		V/µs
t_s	Setting time	To 0.1 %, V_{in} = 1 Vp-p, R_L = 10 kΩ, C_L = 100 pF		50		µs
e_n	Equivalent input noise voltage	f = 1 kHz		60		nV/√Hz
		f = 10 kHz		60		
C_s	Channel separation	f = 100 Hz		120		dB
t_{init}	Initialization time	T = 25 °C		50		µs
		-40 °C < T < 125 °C		100		

Notes:

(1)See *Section 5.5: "Input offset voltage drift over temperature"*. Input offset measurements are performed on x100 gain configuration. The amplifiers and the gain setting resistors are at the same temperature.

(2)Guaranteed by design

(3)Slew rate value is calculated as the average between positive and negative slew rates.

Table 4: Electrical characteristics at VCC+ = 3.3 V with VCC- = 0 V, Vicm = VCC/2, T = 25 ° C, and RL = 10 kΩ connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		1	5	µV
		-40 °C < T < 125 °C			8	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)	-40 °C < T < 125 °C		10	30	nV/°C
I_{ib}	Input bias current (V_{out} = V_{CC}/2)	T = 25 °C		60	200 (2)	pA
		-40 °C < T < 125 °C			300 (2)	
I_{io}	Input offset current (V_{out} = V_{CC}/2)	T = 25 °C		120	400 (2)	
		-40 °C < T < 125 °C			600 (2)	
CMR	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{ic} = 0 V to V_{CC}, V_{out} = V_{CC}/2, R_L > 1 MΩ	T = 25 °C	115	128		dB
		-40 °C < T < 125 °C	115			
A_{vd}	Large signal voltage gain, V_{out} = 0.5 V to (V_{CC} - 0.5 V)	T = 25 °C	118	135		
		-40 °C < T < 125 °C	110			
V_{OH}	High-level output voltage	T = 25 °C			30	mV
		-40 °C < T < 125 °C			70	
V_{OL}	Low-level output voltage	T = 25 °C			30	
		-40 °C < T < 125 °C			70	
I_{out}	I_{sink} (V_{out} = V_{CC})	T = 25 °C	15	18		mA
		-40 °C < T < 125 °C	12			
	I_{source} (V_{out} = 0 V)	T = 25 °C	14	16		
		-40 °C < T < 125 °C	10			
I_{CC}	Supply current (per amplifier), V_{out} = V_{CC}/2, R_L > 1 MΩ)	T = 25 °C		29	40	µA
		-40 °C < T < 125 °C			40	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		400		kHz
F_u	Unity gain frequency			300		
ϕm	Phase margin			56		Degrees
G_m	Gain margin			19		dB
SR	Slew rate (3)			0.19		V/µs
t_s	Setting time	To 0.1 %, V_{in} = 1 Vp-p, R_L = 10 kΩ, C_L = 100 pF		50		µs
e_n	Equivalent input noise voltage	f = 1 kHz		40		nV/√Hz
		f = 10 kHz		40		
C_s	Channel separation	f = 100 Hz		120		dB
t_{init}	Initialization time	T = 25 °C		50		µs
		-40 °C < T < 125 °C		100		

Notes:

(1)See *Section 5.5: "Input offset voltage drift over temperature"*. Input offset measurements are performed on x100 gain configuration. The amplifiers and the gain setting resistors are at the same temperature.

(2)Guaranteed by design

(3)Slew rate value is calculated as the average between positive and negative slew rates.

Table 5: Electrical characteristics at VCC+ = 5 V with VCC- = 0 V, Vicm = VCC/2, T = 25 ° C, and RL = 10 kΩ connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		1	5	µV
		-40 °C < T < 125 °C			8	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)	-40 °C < T < 125 °C		10	30	nV/°C
I_{ib}	Input bias current ($V_{out} = V_{CC}/2$)	T = 25 °C		70	200 (2)	pA
		-40 °C < T < 125 °C			300 (2)	
I_{io}	Input offset current ($V_{out} = V_{CC}/2$)	T = 25 °C		140	400 (2)	
		-40 °C < T < 125 °C			600 (2)	
CMR	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{ic} = 0 V to V_{CC}, $V_{out} = V_{CC}/2$, R_L > 1 MΩ	T = 25 °C	115	136		dB
		-40 °C < T < 125 °C	115			
SVR	Supply voltage rejection ratio, 20 log ($\Delta V_{CC}/\Delta V_{io}$), V_{CC} = 1.8 V to 5.5 V, $V_{out} = V_{CC}/2$, R_L > 1 MΩ	T = 25 °C	120	140		
		-40 °C < T < 125 °C	120			
A_{vd}	Large signal voltage gain, V_{out} = 0.5 V to (V_{CC} - 0.5 V)	T = 25 °C	120	135		
		-40 °C < T < 125 °C	110			
EMIRR (3)	EMI rejection rate = -20 log ($V_{RFpeak}/\Delta V_{io}$)	V_{RF} = 100 mV_p, f = 400 MHz		84		
		V_{RF} = 100 mV_p, f = 900 MHz		87		
		V_{RF} = 100 mV_p, f = 1800 MHz		90		
		V_{RF} = 100 mV_p, f = 2400 MHz		91		
V_{OH}	High-level output voltage	T = 25 °C			30	mV
		-40 °C < T < 125 °C			70	
V_{OL}	Low-level output voltage	T = 25 °C			30	
		-40 °C < T < 125 °C			70	
I_{out}	I_{sink} ($V_{out} = V_{CC}$)	T = 25 °C	15	18		mA
		-40 °C < T < 125 °C	14			
	I_{source} (V_{out} = 0 V)	T = 25 °C	14	17		
		-40 °C < T < 125 °C	12			
I_{CC}	Supply current (per amplifier), $V_{out} = V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C		31	40	µA
		-40 °C < T < 125 °C			40	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		400		kHz
F_u	Unity gain frequency			300		
ϕm	Phase margin			53		Degrees
G_m	Gain margin			19		dB
SR	Slew rate (4)			0.19		V/µs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_s	Setting time	To 0.1 %, V_{in} = 100 mVp-p, R_L = 10 kΩ, C_L = 100 pF		10		µs
e_n	Equivalent input noise voltage	f = 1 kHz		37		nV/√Hz
		f = 10 kHz		37		
C_s	Channel separation	f = 100 Hz		120		dB
t_{init}	Initialization time	T = 25 °C		50		µs
		-40 °C < T < 125 °C		100		

Notes:

(1)See *Section 5.5: "Input offset voltage drift over temperature"*. Input offset measurements are performed on x100 gain configuration. The amplifiers and the gain setting resistors are at the same temperature.

(2)Guaranteed by design

(3)Tested on SC70-5 package

(4)Slew rate value is calculated as the average between positive and negative slew rates.

4 Electrical characteristic curves

Figure 2: Supply current vs. supply voltage

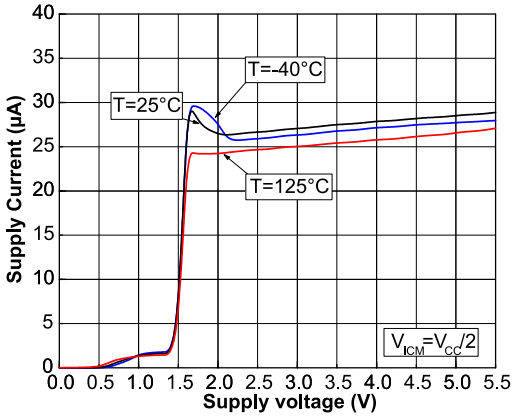


Figure 3: Input offset voltage distribution at VCC = 5 V

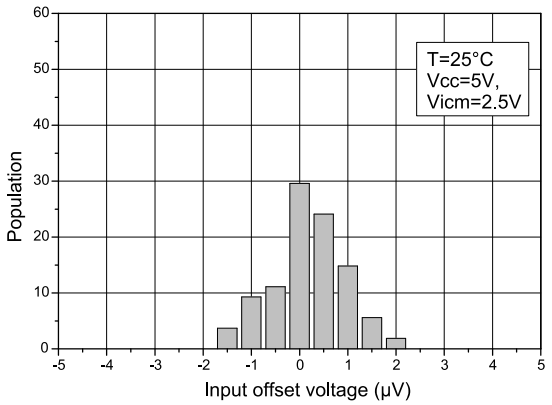


Figure 4: Input offset voltage distribution at VCC = 3.3 V

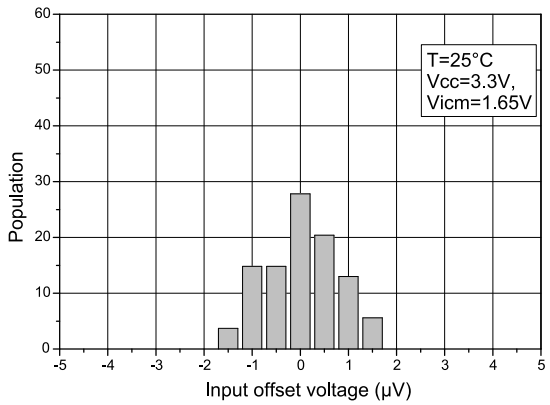


Figure 5: Input offset voltage distribution at VCC = 1.8 V

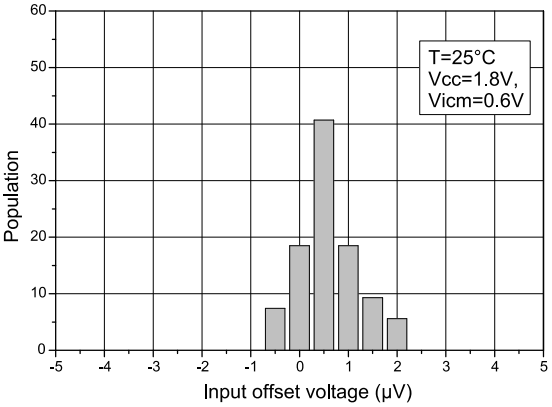


Figure 6: Vio temperature co-efficient distribution (-40 °C to 25 °C)

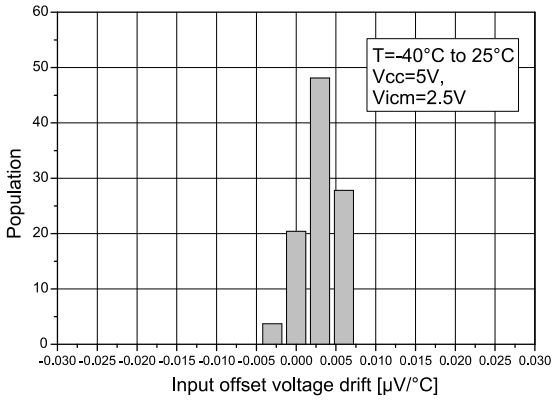


Figure 7: Vio temperature co-efficient distribution (25 °C to 125 °C)

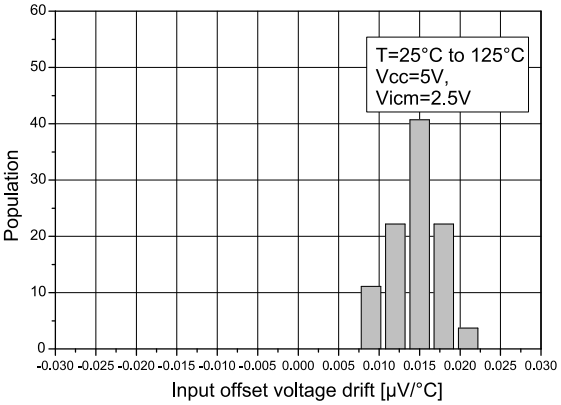


Figure 8: Input offset voltage vs. supply voltage

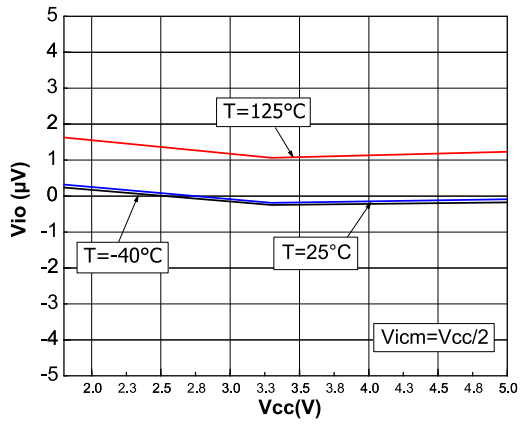


Figure 9: Input offset voltage vs. input common-mode at VCC = 1.8 V

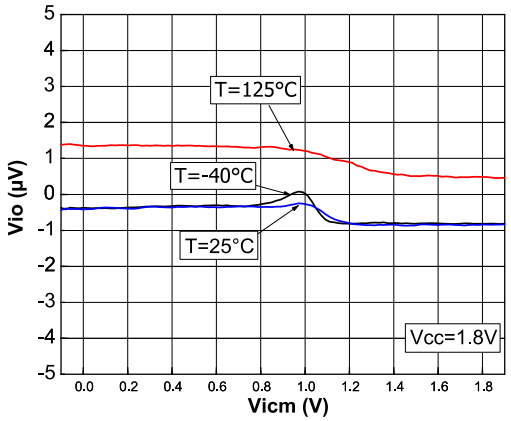


Figure 10: Input offset voltage vs. input common-mode at VCC = 2.7 V

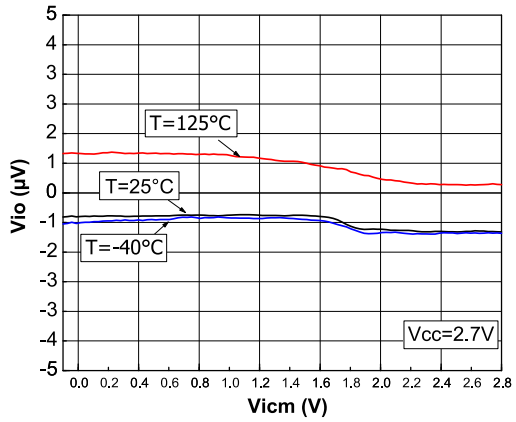


Figure 11: Input offset voltage vs. input common-mode at VCC = 5.5 V

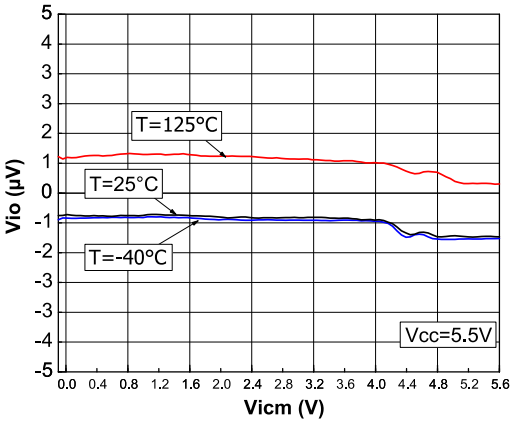


Figure 12: Input offset voltage vs. temperature

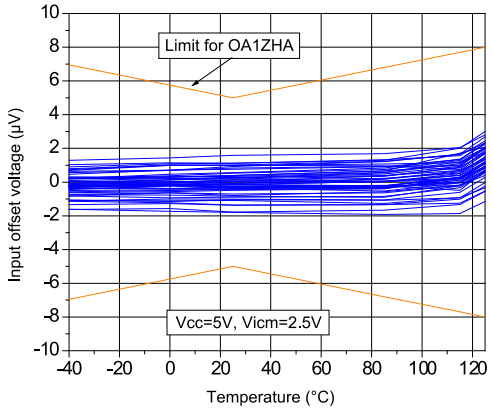


Figure 13: VOH vs. supply voltage

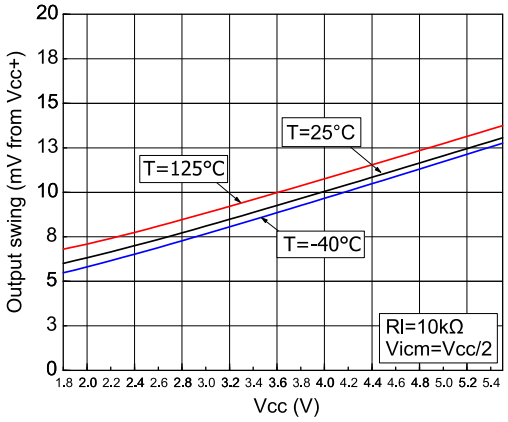


Figure 14: VOL vs. supply voltage

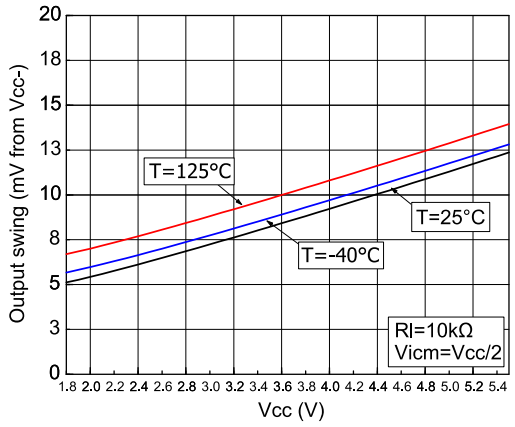


Figure 15: Output current vs. output voltage at VCC = 1.8 V

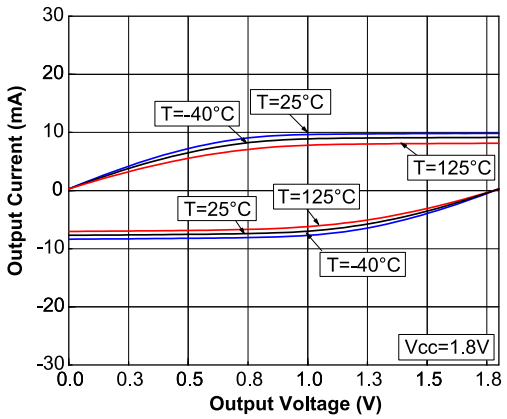


Figure 16: Output current vs. output voltage at VCC = 5.5 V

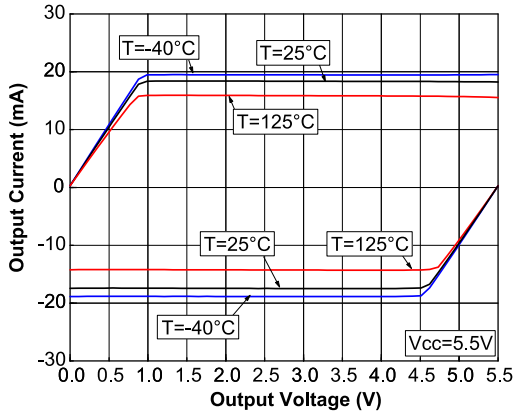


Figure 17: Input bias current vs. common mode at VCC = 5 V

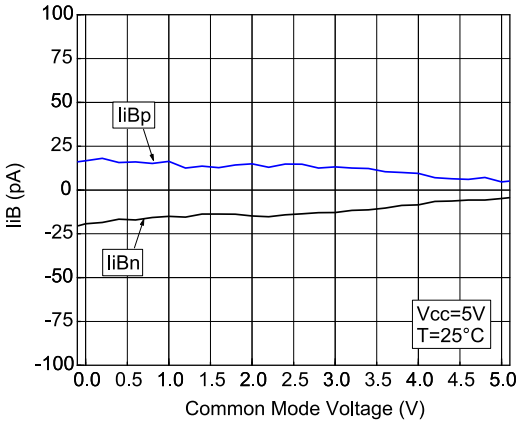


Figure 18: Input bias current vs. common-mode at VCC = 1.8 V

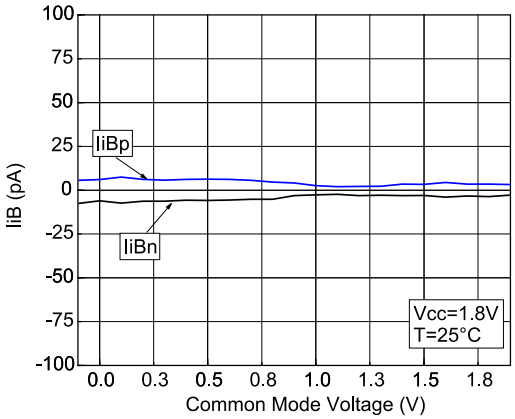


Figure 19: Input bias current vs. temperature at VCC = 5 V

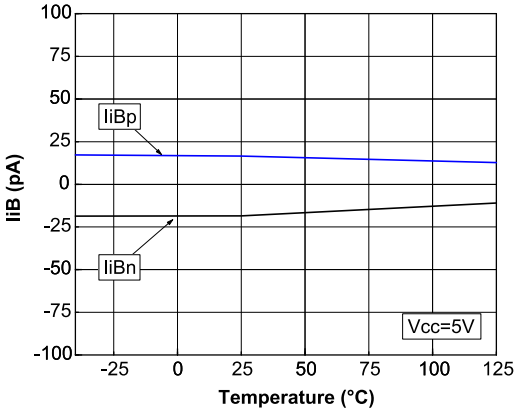


Figure 20: Bode diagram at VCC = 1.8 V

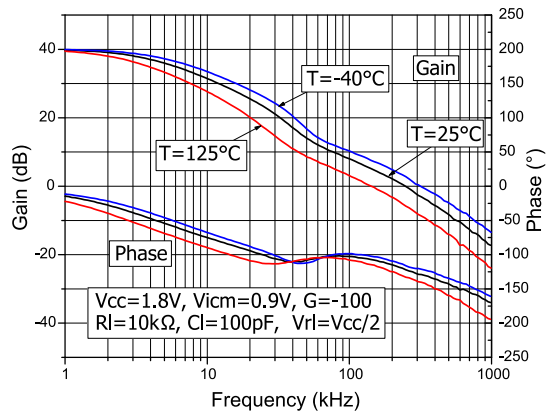


Figure 21: Bode diagram at VCC = 2.7 V

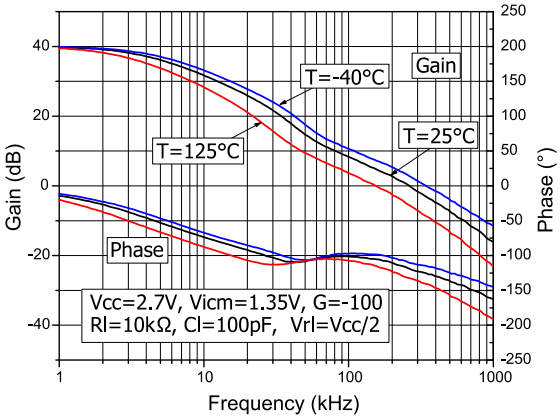


Figure 22: Bode diagram at VCC = 5.5 V

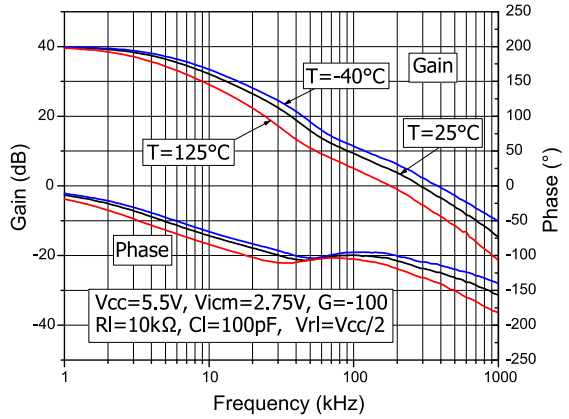


Figure 23: Open loop gain vs. frequency

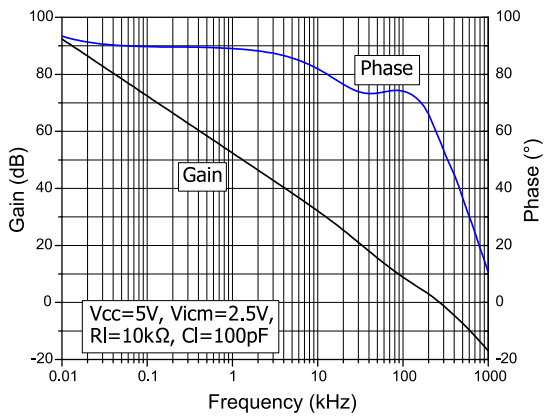


Figure 24: Positive slew rate vs. supply voltage

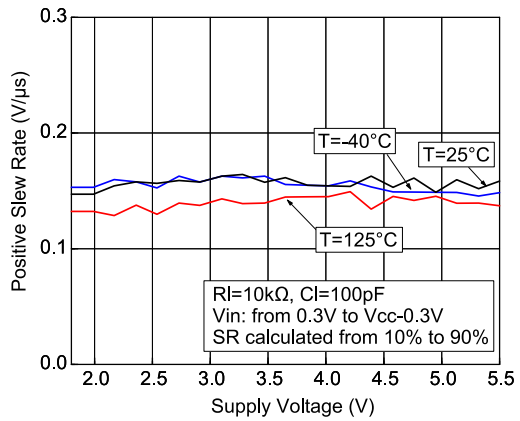


Figure 25: Negative slew rate vs. supply voltage

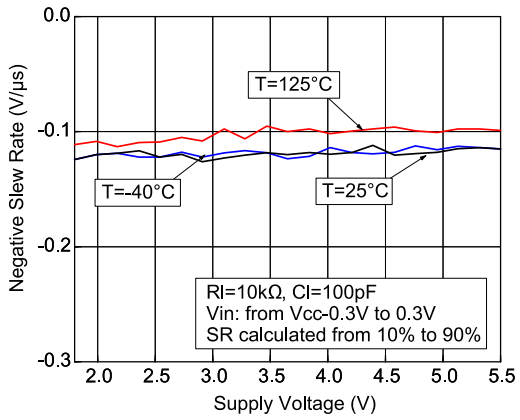


Figure 26: 0.1 Hz to 10 Hz noise

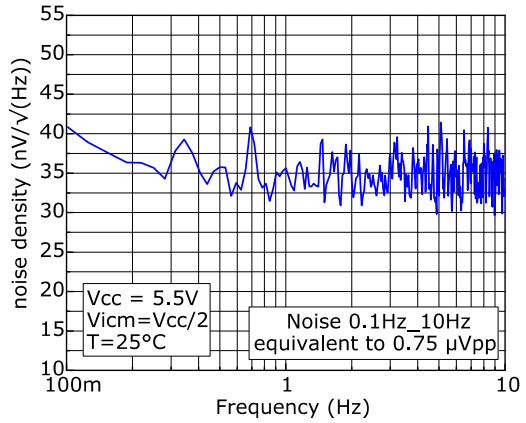


Figure 27: Noise vs. frequency

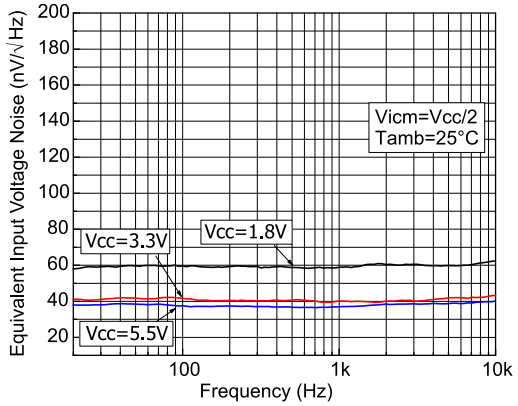


Figure 28: Noise vs. frequency and temperature

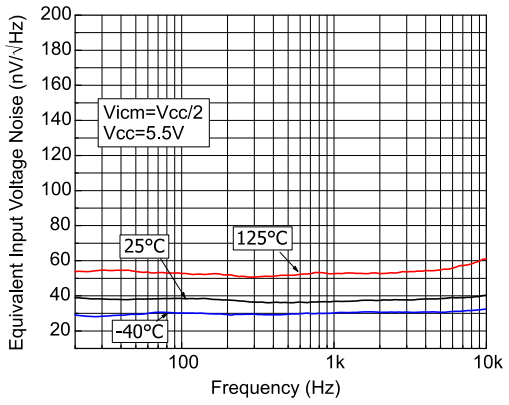


Figure 29: Output overshoot vs. load capacitance

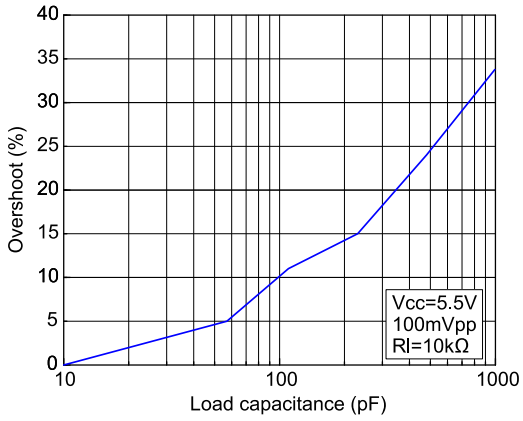


Figure 30: Small signal

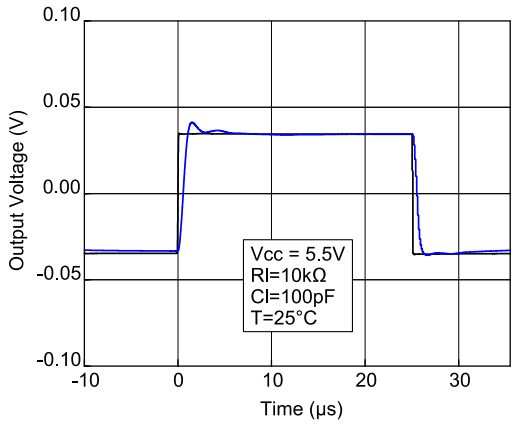


Figure 31: Large signal

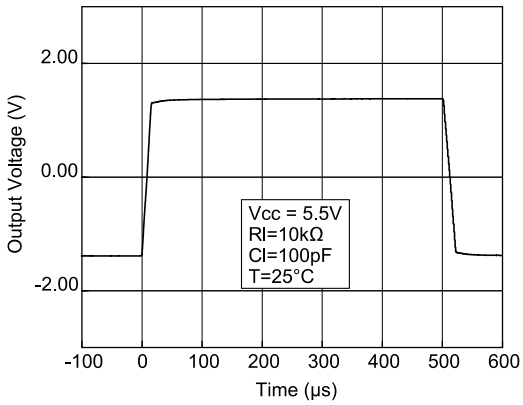


Figure 32: Positive overvoltage recovery at VCC = 1.8 V

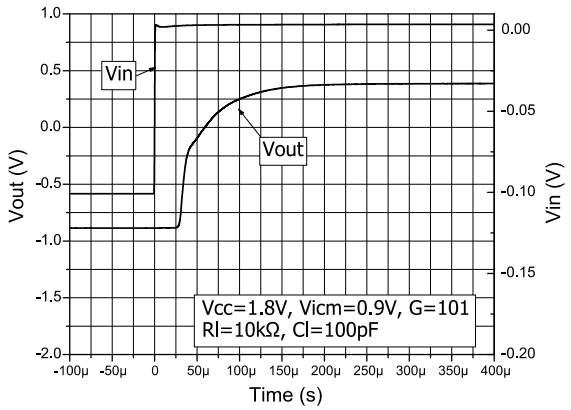


Figure 33: Positive overvoltage recovery at VCC = 5 V

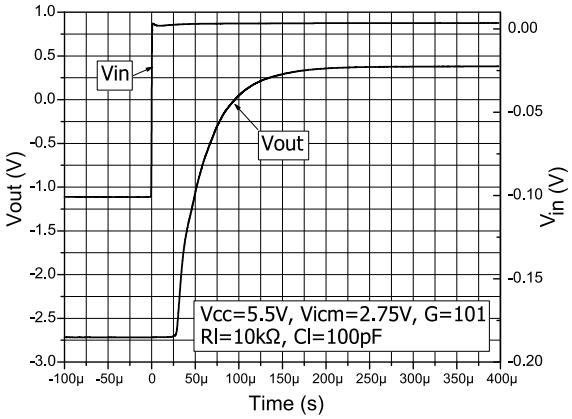


Figure 34: Negative overvoltage recovery at VCC = 1.8 V

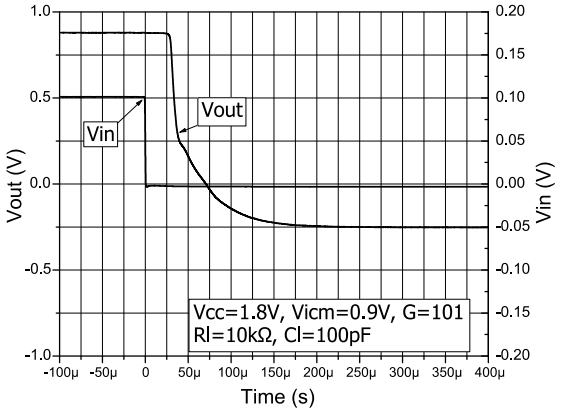


Figure 35: Negative overvoltage recovery at VCC = 5 V

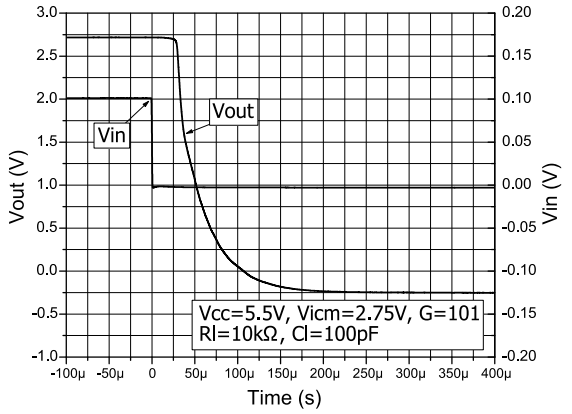


Figure 36: PSRR vs. frequency

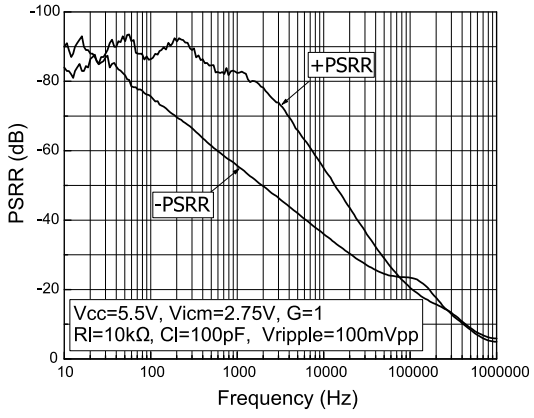
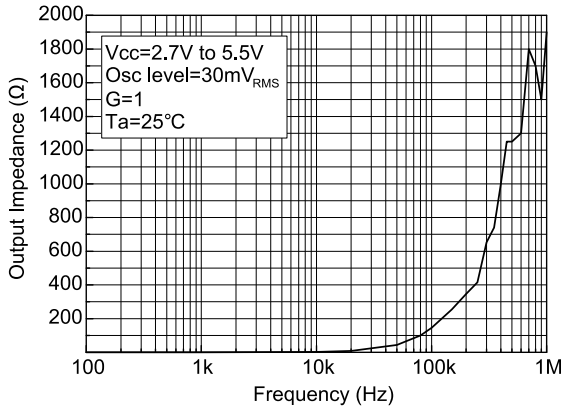


Figure 37: Output impedance vs. frequency



5 Application information

5.1 Operation theory

The OA1ZHA, OA2ZHA and OA4ZHA are high precision CMOS op amp. They achieve a low offset drift and no 1/f noise thanks to their chopper architecture. Chopper-stabilized amps constantly correct low-frequency errors across the inputs of the amplifier.

Chopper-stabilized amplifiers can be explained with respect to:

- Time domain
- Frequency domain

5.1.1 Time domain

The basis of the chopper amplifier is realized in two steps. These steps are synchronized thanks to a clock running at 400 kHz.

Figure 38: Block diagram in the time domain (step 1)

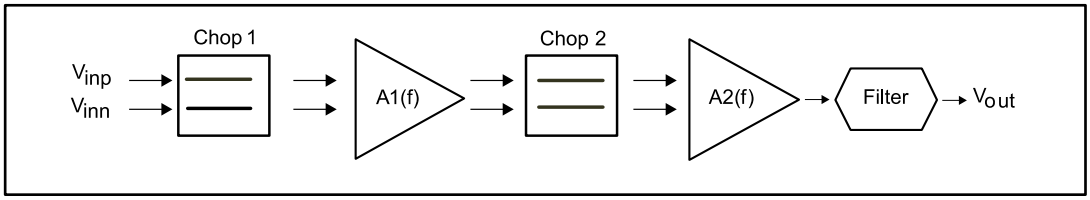


Figure 39: Block diagram in the time domain (step 2)

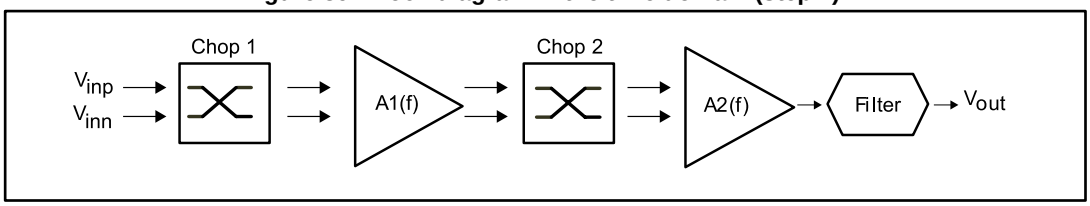


Figure 38: "Block diagram in the time domain (step 1)" shows step 1, the first clock cycle, where V_{io} is amplified in the normal way.

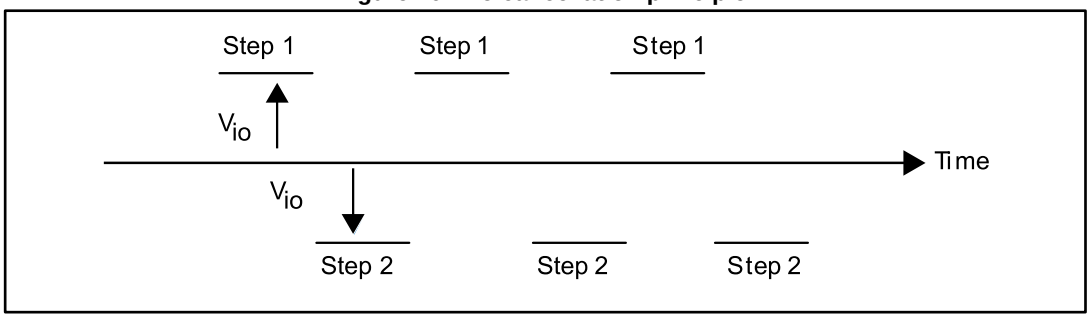
Figure 39: "Block diagram in the time domain (step 2)" shows step 2, the second clock cycle, where Chop1 and Chop2 swap paths. At this time, the V_{io} is amplified in a reverse way as compared to step 1.

At the end of these two steps, the average V_{io} is close to zero.

The A2(f) amplifier has a small impact on the V_{io} because the V_{io} is expressed as the input offset and is consequently divided by A1(f).

In the time domain, the offset part of the output signal before filtering is shown in *Figure 40: "Vio cancellation principle"*.

Figure 40: Vio cancellation principle



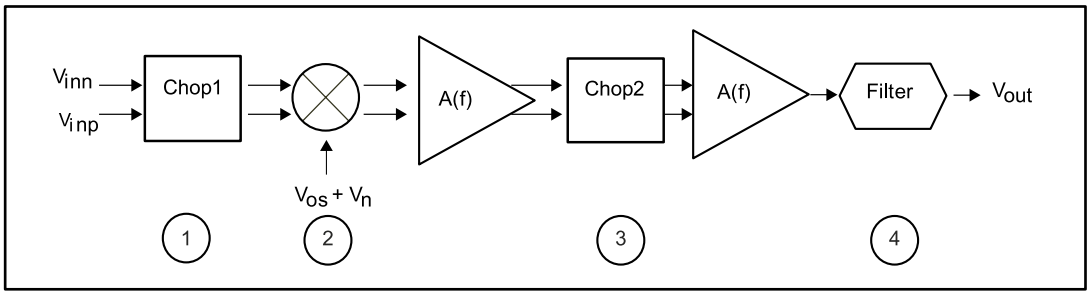
The low pass filter averages the output value resulting in the cancellation of the V_{io} offset.

The 1/f noise can be considered as an offset in low frequency and it is canceled like the V_{io}, thanks to the chopper technique.

5.1.2 Frequency domain

The frequency domain gives a more accurate vision of chopper-stabilized amplifier architecture.

Figure 41: Block diagram in the frequency domain



The modulation technique transposes the signal to a higher frequency where there is no 1/f noise, and demodulate it back after amplification.

1. According to *Figure 41: "Block diagram in the frequency domain"*, the input signal V_{in} is modulated once (Chop1) so all the input signal is transposed to the high frequency domain.
2. The amplifier adds its own error (V_{io} (output offset voltage) + the noise V_n (1/f noise)) to this modulated signal.
3. This signal is then demodulated (Chop2), but since the noise and the offset are modulated only once, they are transposed to the high frequency, leaving the output signal of the amplifier without any offset and low frequency noise. Consequently, the input signal is amplified with a very low offset and 1/f noise.
4. To get rid of the high frequency part of the output signal (which is useless) a low pass filter is implemented.

To further suppress the remaining ripple down to a desired level, another low pass filter may be added externally on the output of the OA1ZHA, OA2ZHA and OA4ZHA device.

5.2 Operating voltages

OA1ZHA, OA2ZHA and OA4ZHA CMOS op amp can operate from 1.8 to 5.5 V. The parameters are fully specified for 1.8 V, 3.3 V, and 5 V power supplies. However, the parameters are very stable in the full ςXX range and several characterization curves show the OA1ZHA, OA2ZHA and OA4ZHA op amp characteristics at 1.8 V and 5.5 V. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 to 125 ° C.

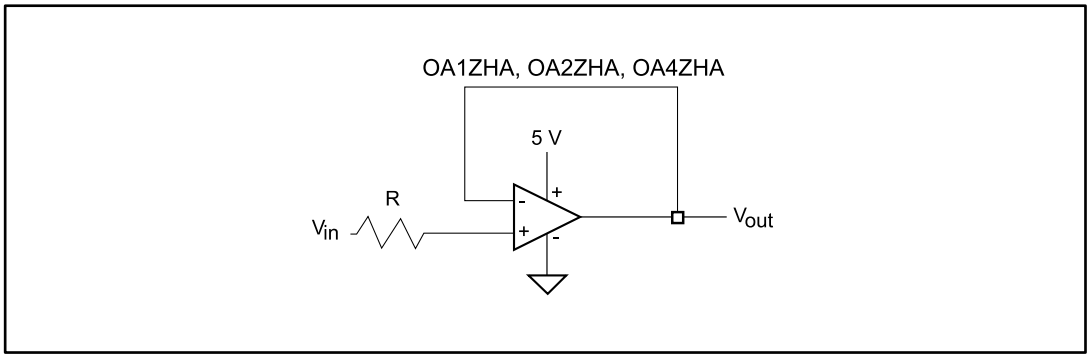
5.3 Input pin voltage ranges

OA1ZHA, OA2ZHA and OA4ZHA CMOS op amp can operate from 1.8 to 5.5 V. The parameters are fully specified for 1.8 V, 3.3 V, and have internal ESD diode protection on the inputs. These diodes are connected between the input and each supply rail to protect the input MOSFETs from electrical discharge.

If the input pin voltage exceeds the power supply by 0.5 V, the ESD diodes become conductive and excessive current can flow through them. Without limitation this over current can damage the device.

In this case, it is important to limit the current to 10 mA, by adding resistance on the input pin, as described in *Figure 42: "Input current limitation"*.

Figure 42: Input current limitation



5.4 Rail-to-rail input

OA1ZHA, OA2ZHA and OA4ZHA CMOS op amp have a rail-to-rail input, and the input common mode range is extended from (V_{CC-}) - 0.1 V to (V_{CC+}) + 0.1 V.

5.5 Input offset voltage drift over temperature

The maximum input voltage drift variation over temperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using *Equation 1*.

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25\,°C)}{T - 25\,°C}\right|$$

where T = -40 °C and 125 °C.

The OA1ZHA, OA2ZHA and OA4ZHA CMOS datasheet maximum value is guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.6 Rail-to-rail output

The operational amplifier output levels can go close to the rails: to a maximum of 30 mV above and below the rail when connected to a 10 kΩ resistive load to $V_{CC}/2$.

5.7 Capacitive load

Driving large capacitive loads can cause stability problems. Increasing the load capacitance produces gain peaking in the frequency response, with overshoot and ringing in the step response. It is usually considered that with a gain peaking higher than 2.3 dB an op amp might become unstable.

Generally, the unity gain configuration is the worst case for stability and the ability to drive large capacitive loads.

Figure 43: "Stability criteria with a serial resistor at VDD = 5 V" and *Figure 44: "Stability criteria with a serial resistor at VDD = 1.8 V"* show the serial resistor that must be added to the output, to make a system stable. *Figure 45: "Test configuration for Riso"* shows the test configuration using an isolation resistor, R_{iso}.

Figure 43: Stability criteria with a serial resistor at VDD = 5 V

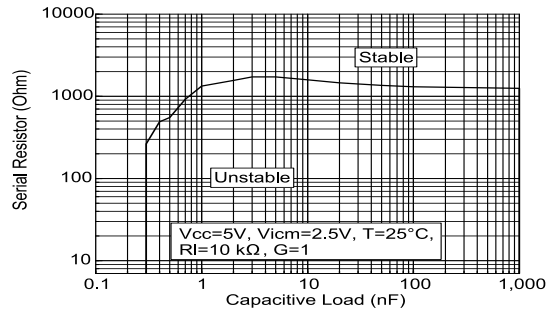


Figure 44: Stability criteria with a serial resistor at VDD = 1.8 V

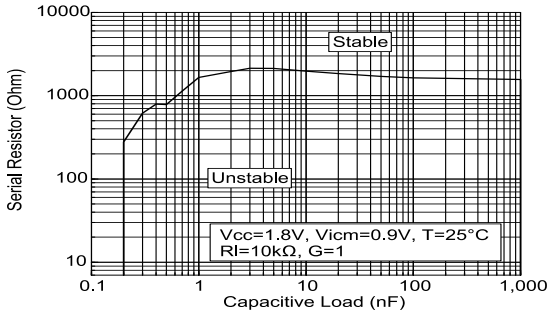
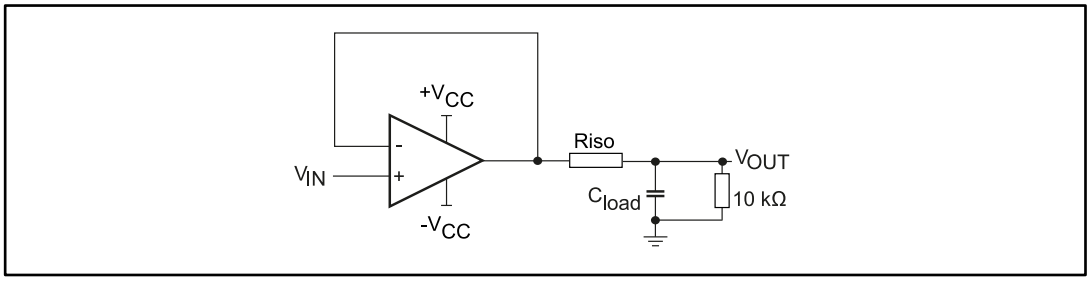


Figure 45: Test configuration for Riso



5.8 PCB layout recommendations

Particular attention must be paid to the layout of the PCB, tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. Good practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used.

The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

5.9 Optimized application recommendation

OA1ZHA, OA2ZHA and OA4ZHA CMOS op amp are based on chopper architecture. As they are switched devices, it is strongly recommended to place a 0.1 µF capacitor as close as possible to the supply pins.

A good decoupling has several advantages for an application. First, it helps to reduce electromagnetic interference. Due to the modulation of the chopper, the decoupling capacitance also helps to reject the small ripple that may appear on the output.

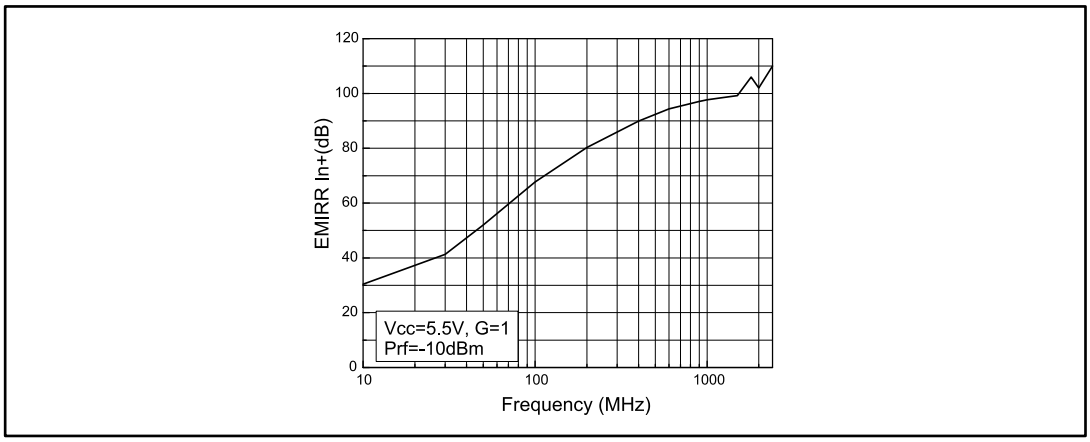
OA1ZHA, OA2ZHA and OA4ZHA CMOS op amp have been optimized for use with 10 kΩ in the feedback loop. With this, or a higher value of resistance, these devices offer the best performance.

5.10 EMI rejection ration (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amp is a change in the offset voltage as a result of RF signal rectification.

OA1ZHA, OA2ZHA and OA4ZHA CMOS op amp have been specially designed to minimize susceptibility to EMIRR and show an extremely good sensitivity. *Figure 46: "EMIRR on IN+ pin"* shows the EMIRR IN+ of the OA1ZHA, OA2ZHA and OA4ZHA measured from 10 MHz up to 2.4 GHz.

Figure 46: EMIRR on IN+ pin

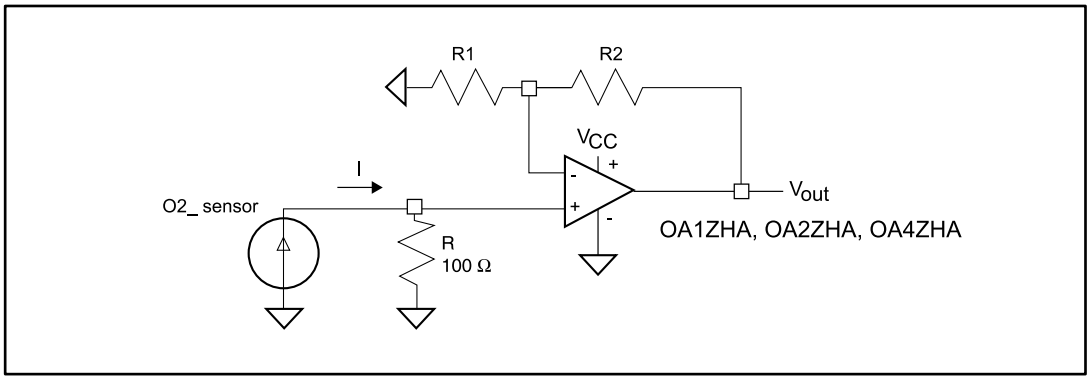


5.11 Application examples

5.11.1 Oxygen sensor

The electrochemical sensor creates a current proportional to the concentration of the gas being measured. This current is converted into voltage thanks to R resistance. This voltage is then amplified by OA1ZHA, OA2ZHA and OA4ZHA CMOS op amp (see *Figure 47: "Oxygen sensor principle schematic"*).

Figure 47: Oxygen sensor principle schematic



The output voltage is calculated using *Equation 2*:

Equation 2

$$V_{out} = (I \times R - V_{io}) \times \left(\frac{R_2}{R_1} + 1\right)$$

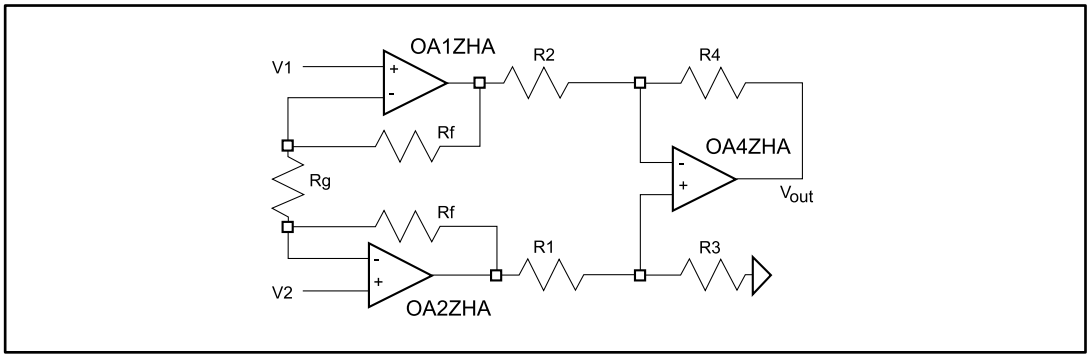
As the current delivered by the O2 sensor is extremely low, the impact of the V_{io} can become significant with a traditional operational amplifier. The use of the chopper amplifier of the OA1ZHA, OA2ZHA and OA4ZHA is perfect for this application.

In addition, using OA1ZHA, OA2ZHA and OA4ZHA op amp for the O2 sensor application ensures that the measurement of O2 concentration is stable even at different temperature thanks to a very good $\Delta V_{io}/\Delta T$.

5.11.2 Precision instrumentation amplifier

The instrumentation amplifier uses three op amp. The circuit, shown in *Figure 48: "Precision instrumentation amplifier schematic"*, exhibits high input impedance, so that the source impedance of the connected sensor has no impact on the amplification.

Figure 48: Precision instrumentation amplifier schematic



The gain is set by tuning the R_g resistor. With R1 = R2 and R3 = R4, the output is given by *Equation 3*.

Equation 3

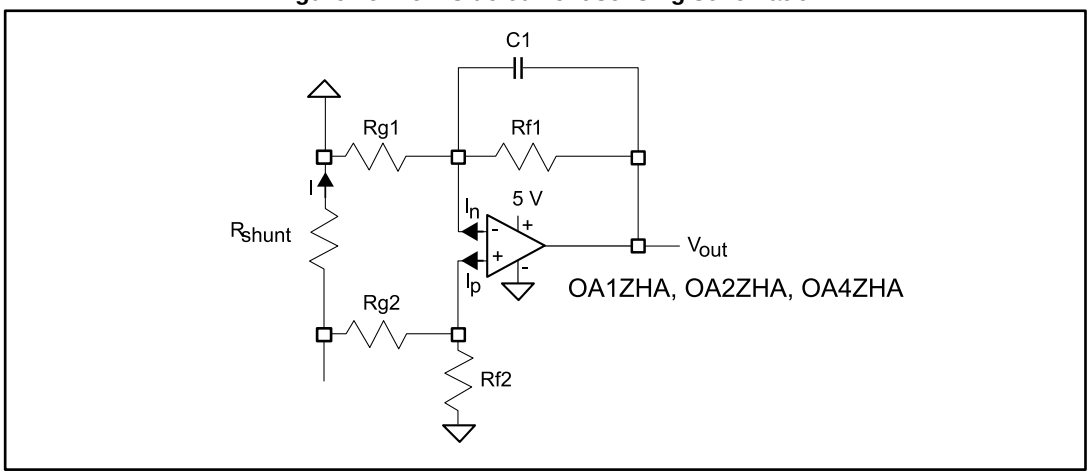
$$V_{out} = (V_2 - V_1)\left[\frac{R_4}{R_2} \cdot \frac{2R_f}{R_g} + 1\right]$$

The matching of R1, R2 and R3, R4 is important to ensure a good common mode rejection ratio (CMR).

5.11.3 Low-side current sensing

Power management mechanisms are found in most electronic systems. Current sensing is useful for protecting applications. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The resulting voltage drop is amplified using OA1ZHA, OA2ZHA and OA4ZHA CMOS op amp (see *Figure 49: "Low-side current sensing schematic"*).

Figure 49: Low-side current sensing schematic



V_{out} can be expressed as follows:

Equation 4

$$V_{out} = R_{shunt} \times I\left(1 - \frac{R_{g2}}{R_{g2} + R_{f2}}\right)\left(1 + \frac{R_{f1}}{R_{g1}}\right) + I_p\left(\frac{R_{g2} \times R_{f2}}{R_{g2} + R_{f2}}\right) \times \left(1 + \frac{R_{f1}}{R_{g1}}\right) - I_n \times R_{f1} - V_{io}\left(1 + \frac{R_{f1}}{R_{g1}}\right)$$

Assuming that $R_{f2} = R_{f1} = R_f$ and $R_{g2} = R_{g1} = R_g$, *Equation 4* can be simplified as follows:

Equation 5

$$V_{out} = R_{shunt} \times I\left(\frac{R_f}{R_g}\right) - V_{io}\left(1 + \frac{R_f}{R_g}\right) + R_f \times I_{io}$$

The main advantage of using the chopper of the OA1ZHA, OA2ZHA and OA4ZHA, for a low-side current sensing, is that the errors due to V_{io} and I_{io} are extremely low and may be neglected.

Therefore, for the same accuracy, the shunt resistor can be chosen with a lower value, resulting in lower power dissipation, lower drop in the ground path, and lower cost.

Particular attention must be paid on the matching and precision of R_{g1}, R_{g2}, R_{f1}, and R_{f2}, to maximize the accuracy of the measurement.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

6.1 SC70-5 (or SOT323-5) package information

Figure 50: SC70-5 (or SOT323-5) package outline

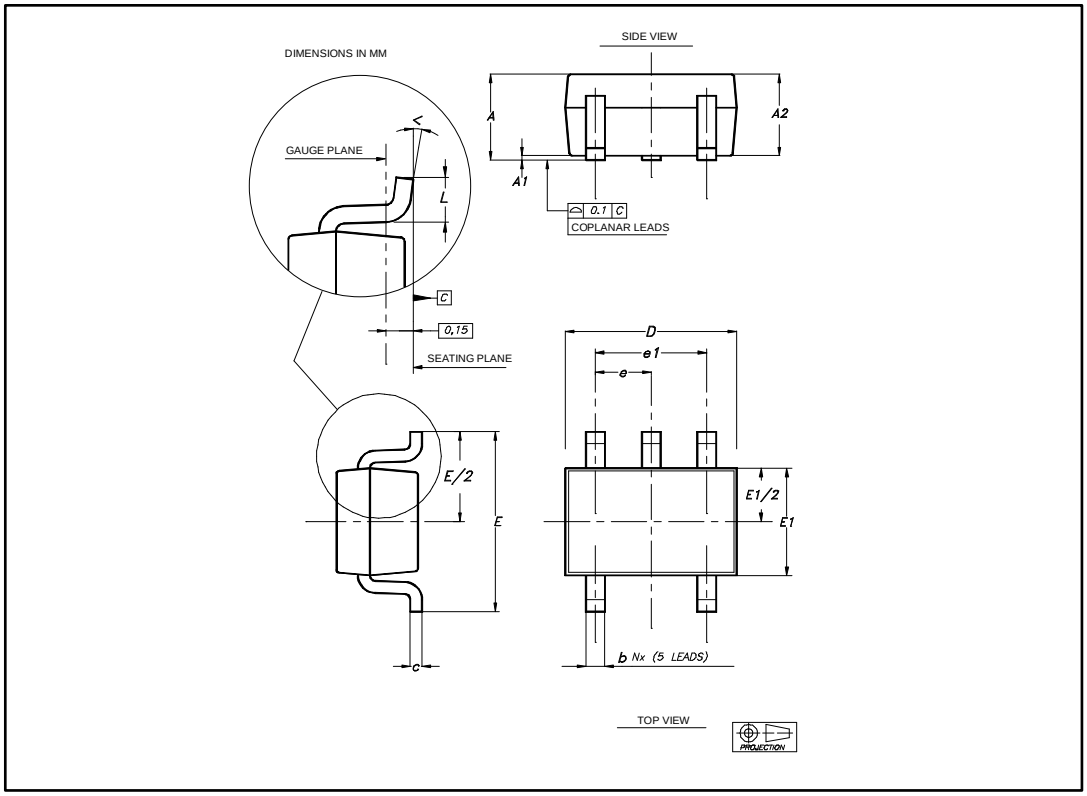


Table 6: SC70-5 (or SOT323-5) mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.032		0.043
A1			0.10			0.004
A2	0.80	0.90	1.00	0.032	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°	0°		8°

6.2 MiniSO8 package information

Figure 51: MiniSO8 package outline

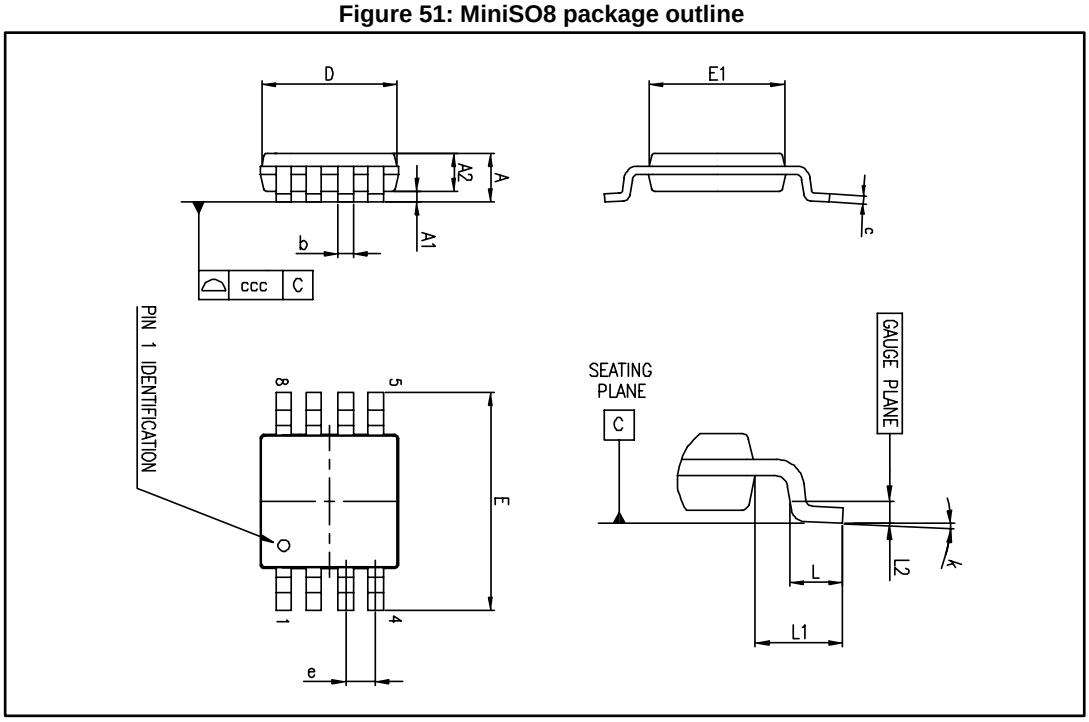


Table 7: MiniSO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

6.3 DFN8 2x2 package information

Figure 52: DFN8 2x2 package outline

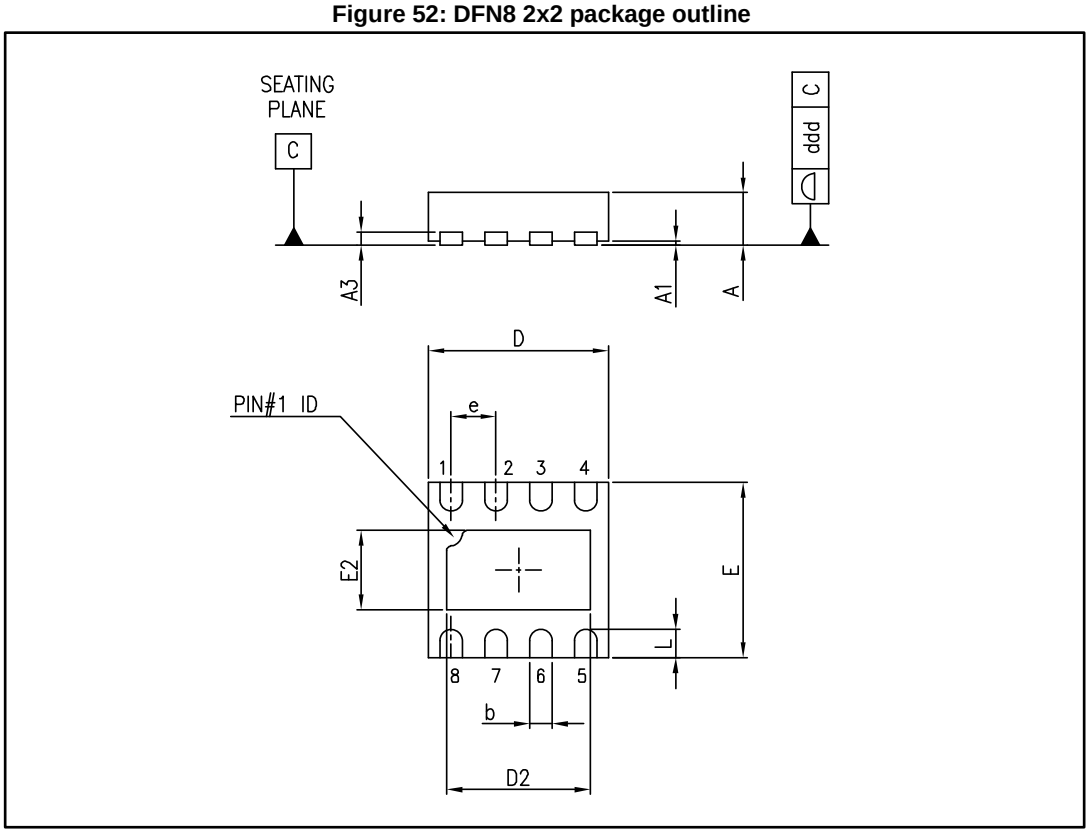
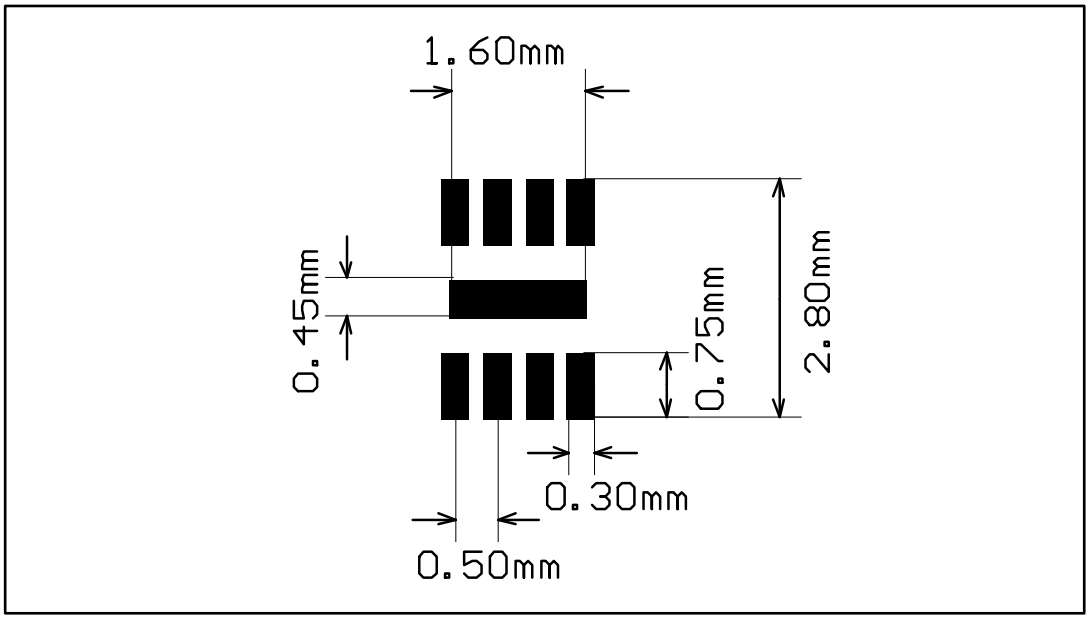


Table 8: DFN8 2x2 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L	0.225	0.325	0.425	0.009	0.013	0.017
ddd			0.08			0.003

Figure 53: DFN8 2x2 recommended footprint



6.4 QFN16 3x3 package information

Figure 54: QFN16 3x3 package outline

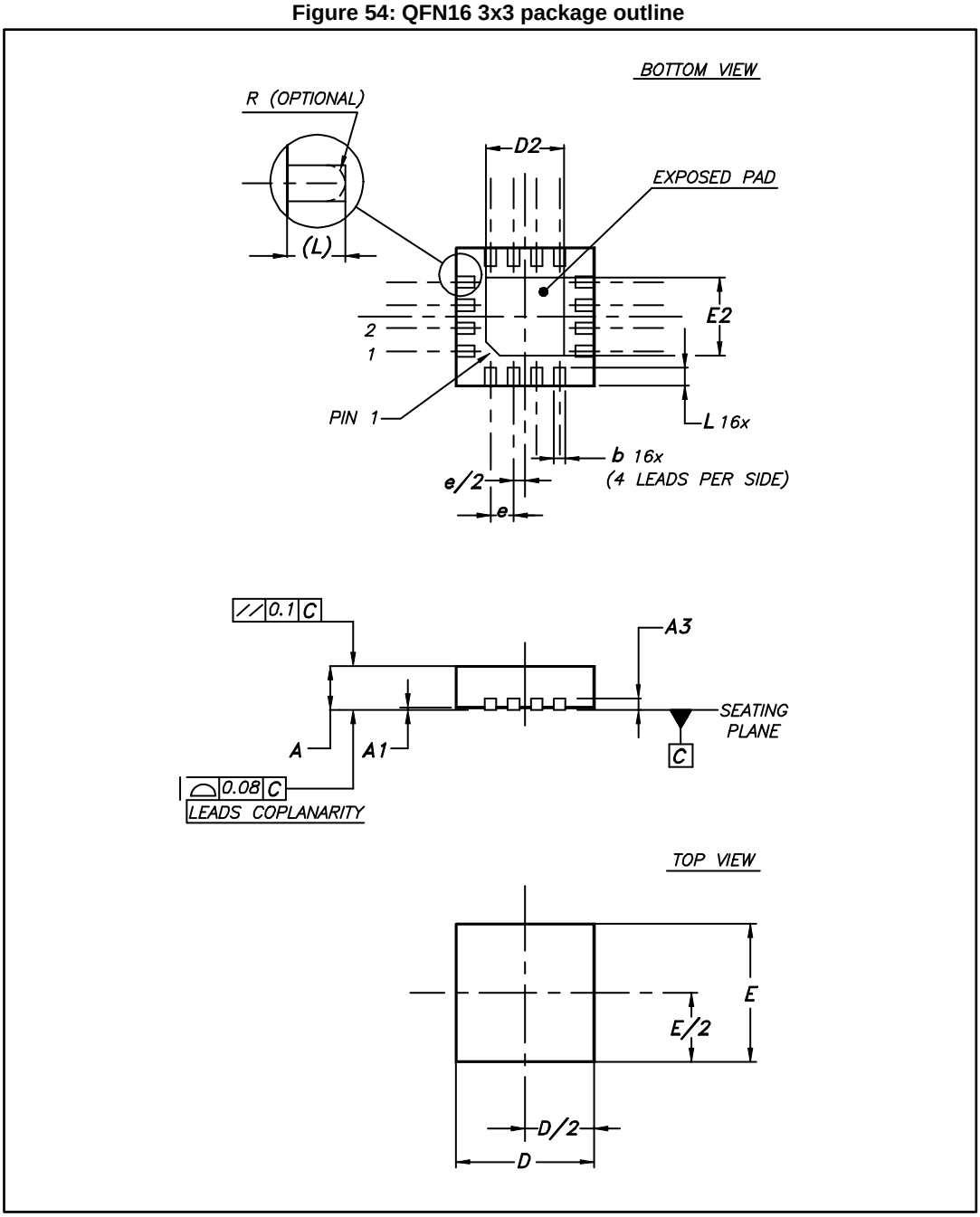
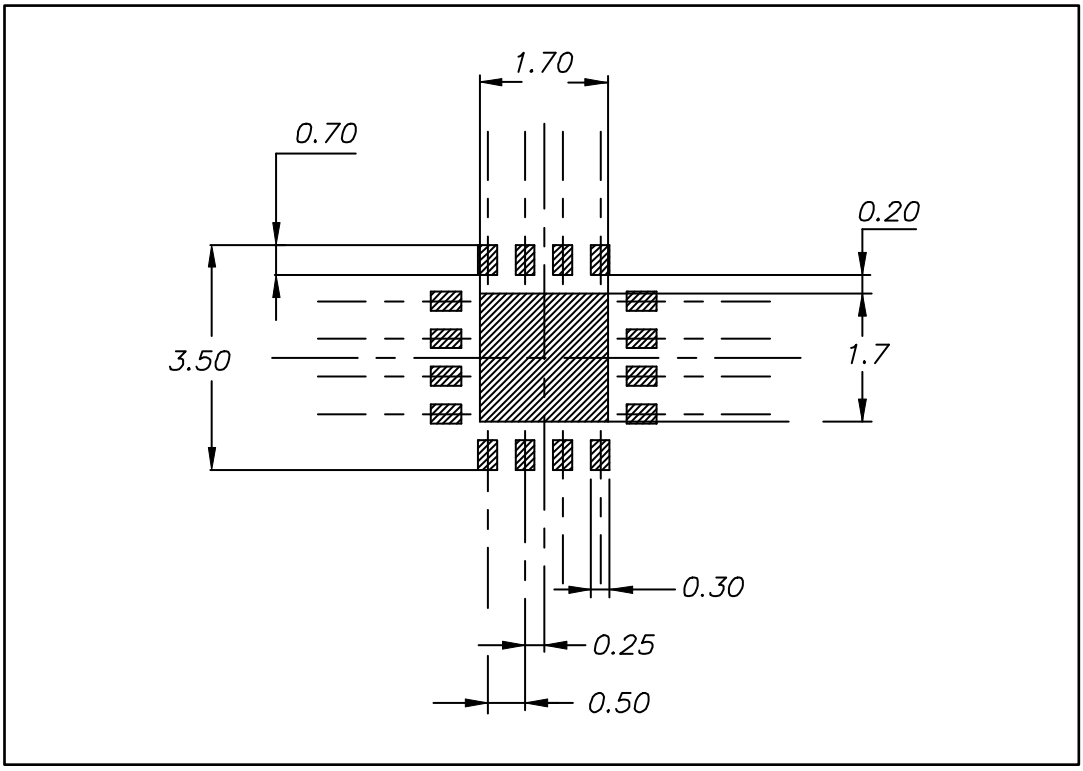


Table 9: QFN16 3x3 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0		0.05	0		0.002
A3		0.20			0.008	
b	0.18		0.30	0.007		0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	1.50		1.80	0.059		0.071
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50		1.80	0.059		0.071
e		0.50			0.020	
L	0.30		0.50	0.012		0.020

Figure 55: QFN16 3x3 recommended footprint



7 Ordering information

Table 10: Order codes

Order code	Temperature range	Package	Packaging	Marking
OA1ZHA22C	-40 to 125 °C	SC70-5	Tape and reel	K44
OA2ZHA34S		MiniSO8		K208
OA2ZHA22Q		DFN8 2x2		K33
OA4ZHA33Q		QFN16 3x3		K193

8 Revision history

Table 11: Document revision history

Date	Revision	Changes
04-Mar-2014	1	Initial release.
30-Jun-2016	2	Updated document layout Removed “Device summary” table from cover page and added information to *Table 10: "Order codes"*. *Section 6.4: "QFN16 3x3 package information"*: added recommended footprint. Added *Section 7: "Ordering information"* *Table 10: "Order codes"*: updated marking of MiniSO8 package.
03-Aug-2017	3	Added minimum and typical dimension values for row L in *Table 8: "DFN8 2x2 mechanical data"*.

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