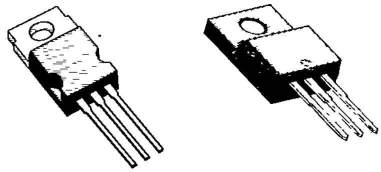
SGS-THOMSON
MICROELECTRONICS

S G S-THOMSON

IRF 840/FI-841/FI
IRF 842/FI-843/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF840	500 V	0.85 Ω	8 A
IRF840FI	500 V	0.85 Ω	4.5 A
IRF841	450 V	0.85 Ω	8 A
IRF841FI	450 V	0.85 Ω	4.5 A
IRF842	500 V	1.1 Ω	7 A
IRF842FI	500 V	1.1 Ω	4 A
IRF843	450 V	1.1 Ω	7 A
IRF843FI	450 V	1.1 Ω	4 A



TO-220 ISOWATT220

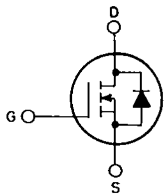
- HIGH VOLTAGE - 450 V FOR OFF LINE SMPS
- ULTRA FAST SWITCHING - FOR OPERATION AT > 100KHz
- EASY DRIVE - FOR REDUCED COST AND SIZE
- COST EFFECTIVE PLASTIC PACKAGE

INDUSTRIAL APPLICATIONS:

- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	TO-220 / ISOWATT220	IRF 840 / 840FI	841 / 841FI	842 / 842FI	843 / 843FI	
V_{DS} *	Drain-source voltage ($V_{GS}=0$)	500	450	500	450	V
V_{DGR} *	Drain-gate voltage ($R_{GS}=20$ KΩ)	500	450	500	450	V
V_{GS}	Gate-source voltage	±20				V
I_{DM} (•)	Drain current (pulsed)	32	32	28	28	A
I_{DLM}	Drain inductive current, clamped (L= 100 μH)	32	32	28	28	A
		840	**841**	**842**	**843**	
I_D	Drain current (cont.) at T_c= 25°C	8	8	7	7	A
I_D	Drain current (cont.) at T_c= 100°C	5.1	5.1	4.4	4.4	A
		840FI	**841FI**	**842FI**	**843FI**	
I_D■	Drain current (cont.) at T_c= 25°C	4.5	4.5	4	4	A
I_D■	Drain current (cont.) at T_c= 100°C	2.8	2.8	2.5	2.5	A
		TO-220		**ISOWATT220**		
P_{tot}■	Total dissipation at T_c <25°C	125		40		W
■	Derating factor	1		0.32		W/°C
T_{stg}	Storage temperature	−55 to 150				°C
T_j	Max. operating junction temperature	150				°C

* T_j = 25°C to 125°C
(•) Repetitive Rating: Pulse width limited by max junction temperature.
■ See note on ISOWATT220 on this datasheet.

June 1988

THERMAL DATA▪

			TO-220	ISOWATT220	
$R_{thj-case}$	Thermal resistance junction-case	max	1	3.12	°C/W
R_{thc-s}	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25°C$ unless otherwise specified)

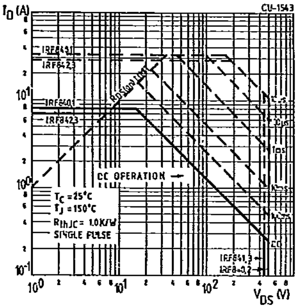
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\,DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu A$ $V_{GS} = 0$ for **IRF840/842/840FI/842FI** for **IRF841/843/841FI/843FI**	 500 450			 V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 $T_c = 125°C$			250 1000	µA µA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20$ V			±500	nA
ON **						
$V_{GS\,(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu A$	2		4	V
$I_{D(on)}$	On-state drain current	$V_{DS} > I_{D\,(on)} \times R_{DS(on)\,max}$ $V_{GS} = 10$ V for **IRF840/841/840FI/841FI** for **IRF842/843/842FI/843FI**	 8 7			 A A
$R_{DS\,(on)}$	Static drain-source on resistance	$V_{GS} = 10$ V $I_D = 4.4$ A for **IRF840/841/840FI/841FI** for **IRF842/843/842FI/843FI**			 0.85 1.1	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	$V_{DS} > I_{D\,(on)} \times R_{DS\,(on)\,max}$ $I_D = 4.4$ A	4.9			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25$ V $f = 1$ MHz $V_{GS} = 0$			1600 350 150	pF pF pF
SWITCHING						
$t_{d\,(on)}$ t_r $t_{d\,(off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	$V_{DD} = 200$ V $I_D = 4.0$ A $R_i = 4.7\ \Omega$ (see test circuit)			35 15 90 30	ns ns ns ns
Q_g	Total Gate Charge	$V_{GS} = 10$ V $I_D = 8$ A V_{DS} = Max Rating × 0.8 (see test circuit)			63	nC

ELECTRICAL CHARACTERISTICS (Continued)

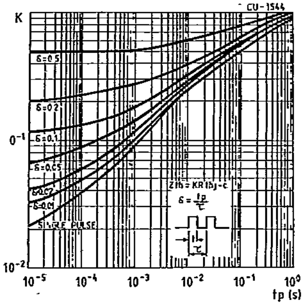
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)					8 32	A A
V_{SD}**	Forward on voltage	I_{SD} = 8 A	V_{GS} = 0			2	V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovered charge	T_j = 150°C I_{SD} = 8.0 A	 di/dt = 100 A/µs		1100 6.4		ns µC

** Pulsed: Pulse duration ⩽ 300 µs, duty cycle ⩽ 1.5%
(•) Repetive Rating: Pulse width limited by max junction temperature
▪ See note on ISOWATT220 in this datasheet

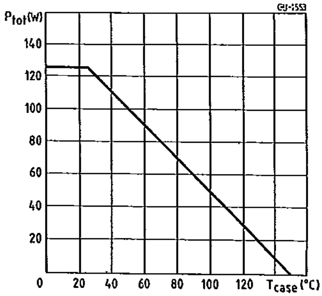
Safe operating areas (standard package)



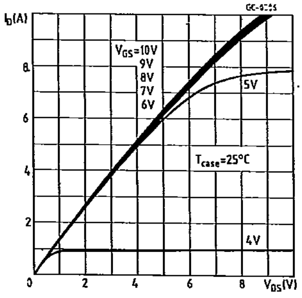
Thermal impedance (standard package)



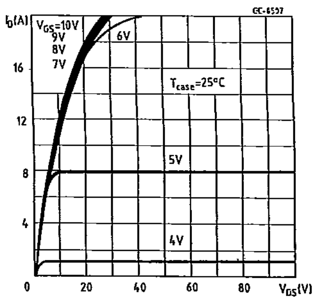
Derating curve (standard package)



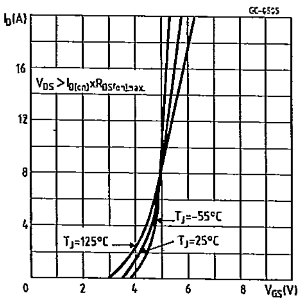
Output characteristics



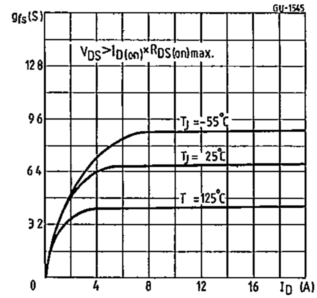
Output characteristics



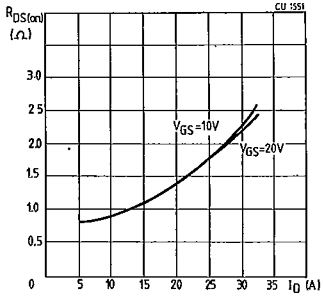
Transfer characteristics



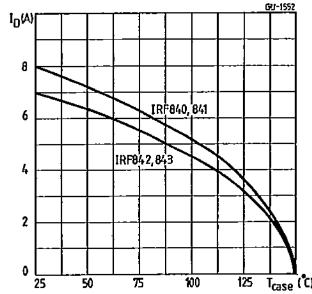
Transconductance



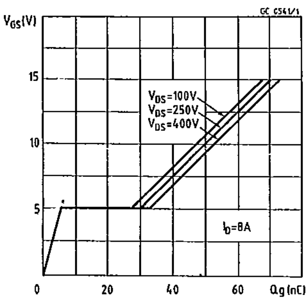
Static drain-source on resistance



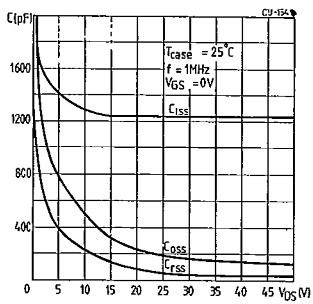
Maximum drain current vs temperature



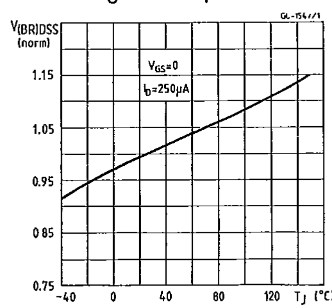
Gate charge vs gate-source voltage



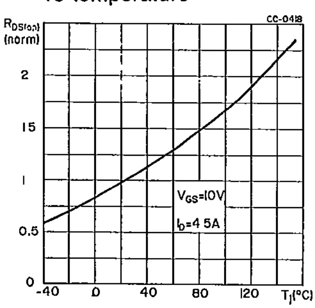
Capacitance variation



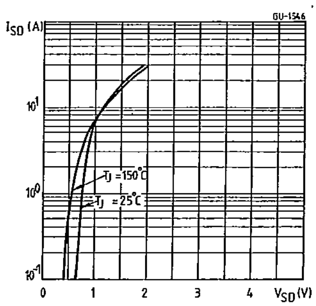
Normalized breakdown voltage vs temperature



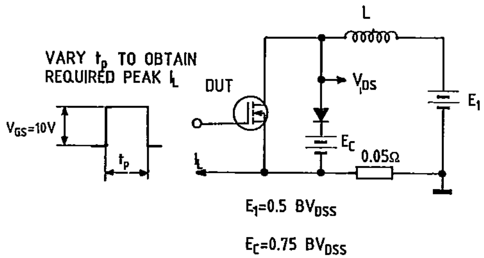
Normalized on resistance vs temperature



Source-drain diode forward characteristics

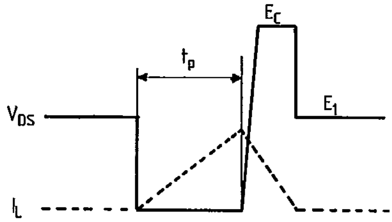


Clamped inductive test circuit



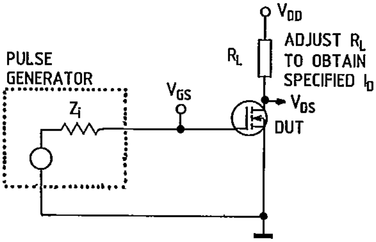
SC-0242

Clamped inductive waveforms



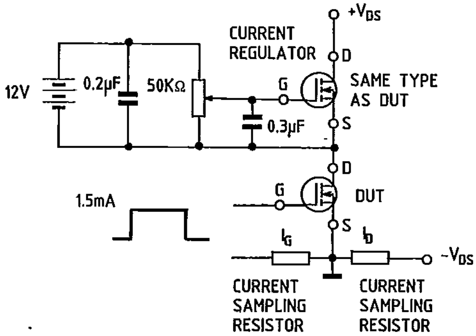
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)}\ (\text{at } 150°C)}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

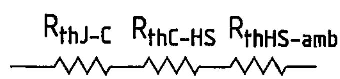
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

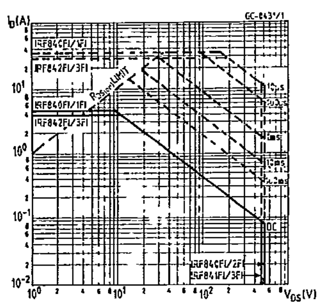
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

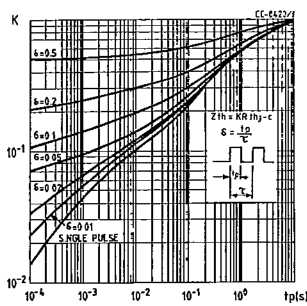


ISOWATT DATA

Safe operating areas



Thermal impedance



Derating curve