UNITRODE

bq2058

Lithium Ion Pack Supervisor for 3- and 4-Cell Packs

Features

- Protects and individually monitors three or four Li-Ion series cells for overvoltage, undervoltage
- Monitors pack for overcurrent
- Designed for battery pack integration
- Minimal external components
- Drives external FET switches
- Selectable overvoltage (V_{OV}) thresholds
  - Mask-programmable by Unitrode
  - Standard version–4.25V
- Supply current: 25µA typical
- Sleep current: 0.7µA typical
- 16-pin 150-mil narrow SOIC

General Description

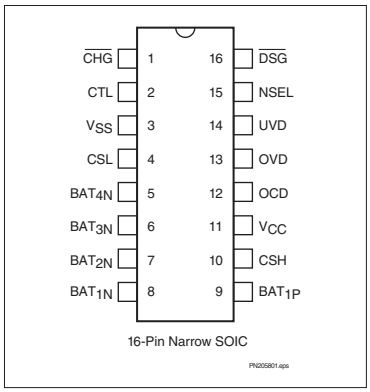
The bq2058 Lithium Ion Pack Supervisor is designed to control the charge and discharge cell voltages for three or four lithium ion (Li-Ion) series cells, accommodating battery packs containing series/parallel configurations. The low operating current does not overdischarge the cells during periods of storage and does not significantly increase the system discharge load. The bq2058 can be part of a low-cost Li-Ion charge control system within the battery pack.

The bq2058 controls two external FETs to limit the charge and discharge potentials. The bq2058 allows charging when each individual cell voltage is below V_{OV} (overvoltage limit). If the voltage on any cell exceeds V_{OV} for a user-configurable delay period (t_{OVD}), the $\overline{CHG}$ pin is driven high, shutting off charge to the battery pack. This safety feature prevents overcharge of any cell within the battery pack. After an overvoltage condition occurs, each cell must fall below V_{CE} (charge enable voltage) for the bq2058 to re-enable charging.

The bq2058 protects batteries from overdischarge. If the voltage on any cell falls below V_{UV} (undervoltage limit) for a user-configurable delay period (t_{UVD}), the $\overline{DSG}$ output is driven high, shutting off the battery discharge. This safety feature prevents overdischarge of any cell within the battery pack.

The bq2058 also stops discharge on detection of an overcurrent condition, such as a short circuit. If an overcurrent condition occurs for a user-configurable delay period (t_{OCD}), the $\overline{DSG}$ output is driven high, disconnecting the load from the pack. $\overline{DSG}$ remains high until removal of the short circuit or overcurrent condition.

Pin Connections



16-Pin Narrow SOIC

PN205801.eps

Pin Names

$\overline{CHG}$	Charge control output
CTL	Pack disable input
V_{SS}	Low potential input
CSL	Current sense low-side input
BAT_{4N}	Battery 4 negative input
BAT_{3N}	Battery 3 negative input
BAT_{2N}	Battery 2 negative input
BAT_{1N}	Battery 1 negative input
$\overline{DSG}$	Discharge control output
NSEL	3- or 4-cell selection
UVD	Undervoltage delay input
OVD	Overvoltage delay input
OCD	Overcurrent delay input
V_{CC}	High potential input
CSH	Current sense high-side input
BAT_{1P}	Battery 1 positive input

1/99 I

Pin Descriptions

$\overline{CHG}$ Charge control output

This push-pull output controls the charge path to the battery pack. Charging is allowed when low.

CTL Pack disable input

When high, this input allows an external source to disable the pack by making both $\overline{DSG}$ and $\overline{CHG}$ inactive. For normal operation, the CTL pin is low.

V_{SS} Low potential input

CSL Overcurrent sense low-side input

This input is connected between the low-side discharge FET (or sense resistor) and BAT_{4N} to enable overcurrent sensing in the battery pack's ground path.

BAT_{4N} Battery 4 negative input

This input is connected to the negative terminal of the cell designated BAT4 in Figure 2.

BAT_{3N} Battery 3 negative input

This input is connected to the negative terminal of the cell designated BAT3 in Figure 2.

BAT_{2N} Battery 2 negative input

This input is connected to the negative terminal of the cell designated BAT2 in Figure 2.

BAT_{1N} Battery 1 negative input

This input is connected to the negative terminal of the cell designated BAT1 in Figure 2. This input is connected to BAT_{1P} in a three-cell configuration.

$\overline{DSG}$ Discharge control output

This push-pull output controls the discharge path to the battery pack. Discharge is allowed when low.

NSEL Number of cells input

This input selects the number of series cells in the pack. NSEL should connect to V_{CC} for four cells and to V_{SS} for three cells.

UVD Undervoltage delay input

This input uses an external capacitor to V_{CC} to set the undervoltage delay timing.

OVD Overvoltage delay input

This input uses an external capacitor to V_{CC} to set the overvoltage delay timing.

OCD Overcurrent delay input

This input uses an external capacitor to V_{CC} to set the overcurrent delay timing.

V_{CC} High potential input

CSH Overcurrent sense high-side input

This input is connected between the high-side discharge FET (or sense resistor) and BAT_{1P} to enable overcurrent sense in the battery pack's positive supply path.

BAT_{1P} Battery 1 positive input

This input is connected to the positive terminal of the cell designated BAT1 in Figure 2.

Table 1. Pin Configuration for 3- and 4-Series Cells

Number of Cells	Configuration Pins	Battery Pins
3 cells	BAT_{1N} tied to BAT_{1P} NSEL = V_{SS}	BAT_{1N} – Positive terminal of first cell
		BAT_{2N} – Negative terminal of first cell
		BAT_{3N} – Negative terminal of second cell
		BAT_{4N} – Negative terminal of third cell
4 cells	NSEL = V_{CC}	BAT_{1P} – Positive terminal of first cell
		BAT_{1N} – Negative terminal of first cell
		BAT_{2N} – Negative terminal of second cell
		BAT_{3N} – Negative terminal of third cell
		BAT_{4N} – Negative terminal of fourth cell

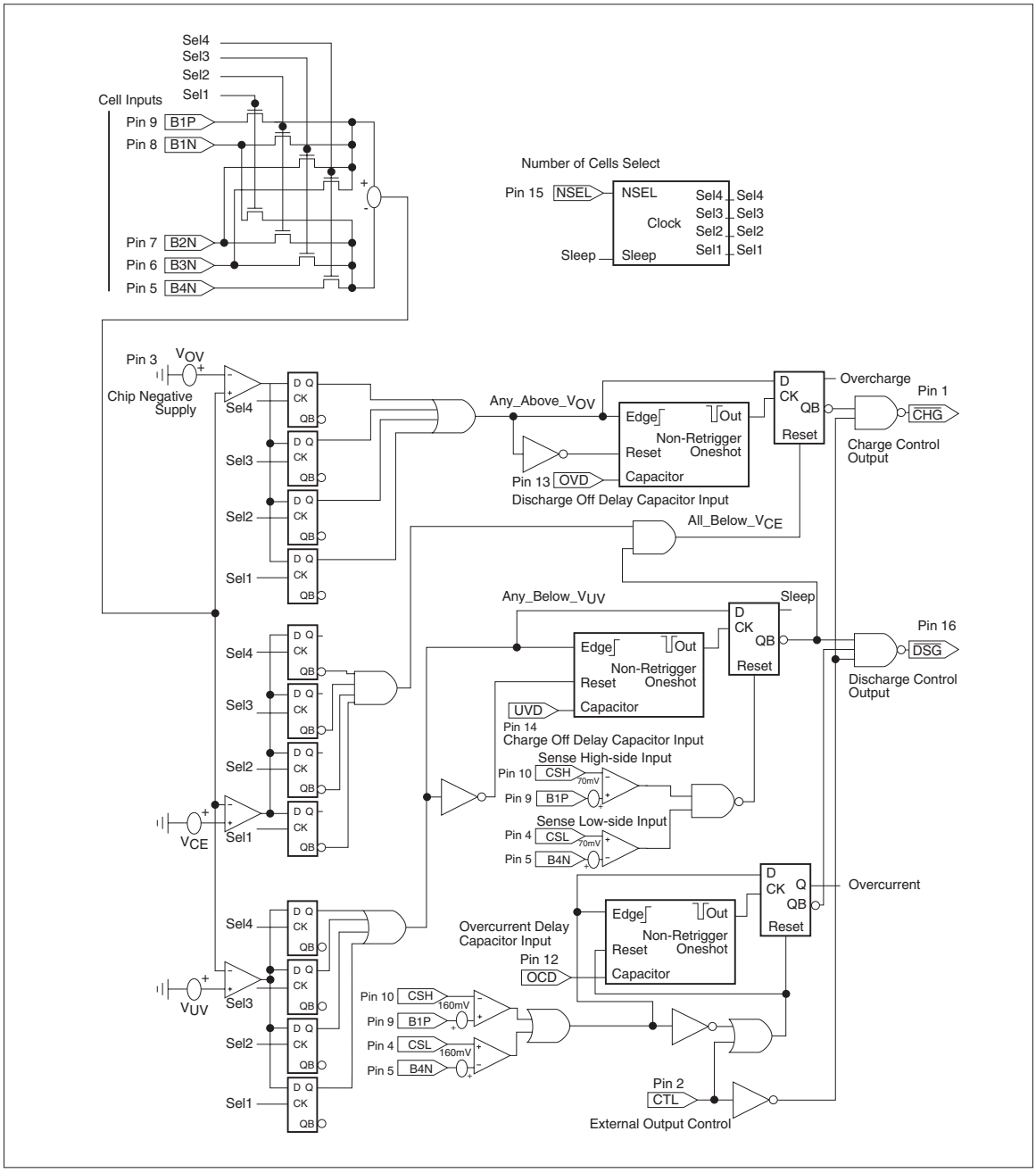


Figure 1. Block Diagram

Functional Description

Figure 1 is a block diagram outlining the major components of the bq2058. Figure 2 shows a 3- or 4-cell pack supervisor circuit. The following sections detail the various functional aspects of the bq2058.

Thresholds

The bq2058 monitors the lithium ion pack for the conditions listed below. Shown with these conditions are the respective thresholds used to determine if that condition exists:

- Overvoltage (V_{OV})
- Undervoltage (V_{UV})
- Overcurrent (V_{OCH}, V_{OCL})
- Charge Enable (V_{CE})
- Charge Detect (V_{CD})

The bq2058 samples a cell every 40ms (typical). Every sample is a fully differential measurement of each cell. During this sample period, the bq2058 compares the measurements with these thresholds to determine if any of the these conditions exist: V_{OV}, V_{UV}, and V_{CE}.

Overcurrent and charge detect are conditions that are not sampled, but are continuously monitored.

Initialization

On initial power-up, such as connecting the battery pack for the first time to the bq2058, the bq2058 enters the low-power sleep mode, disabling the $\overline{DSG}$ output. **It is recommended that a top to bottom cell connection be made at pack assembly for proper initialization.** A charging supply must be applied to the bq2058 circuit to enable the pack. See Low-Power Sleep Mode and Charge Detect sections.

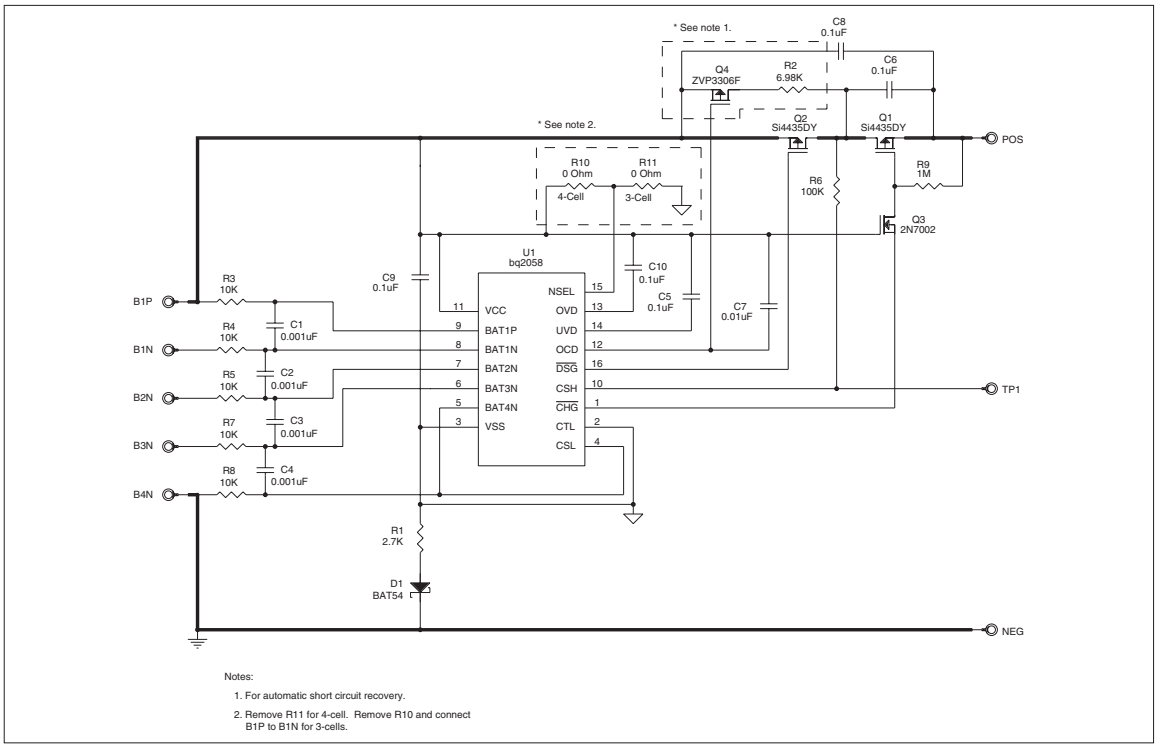


Figure 2. 3- or 4-Cell Li-Ion Battery Pack Supervisor

Low-Power Sleep Mode

The bq2058 enters the low-power sleep mode in two different ways:

1. On initial power-up.
2. After the detection of an undervoltage condition–V_{UV}.

When the bq2058 enters the low-power sleep mode, $\overline{DSG}$ is driven high and the device consumes 0.7µA (typical). The bq2058 only comes out of low-power sleep mode when a valid charge-detect condition exists.

Charge Detect

The bq2058 continuously monitors for a charge-detect condition. A valid charge-detect condition exists when either of the conditions are true:

$$CSL < BAT_{4N} - 70mV\ (V_{CD})$$

$$CSH > BAT_{1P} + 70mV\ (V_{CD})$$

A valid charge-detect enables the $\overline{DSG}$ output, allowing charging of the lithium ion cells. This is accomplished by applying the charging supply to the pack.

Undervoltage

Undervoltage (or overdischarge) protection is asserted when any cell voltage drops below the V_{UV} threshold and remains below the V_{UV} threshold for a time exceeding a user-configurable delay (t_{UVD}). The $\overline{DSG}$ output is driven high disabling the discharge of the pack. The bq2058 then enters the low-power sleep mode.

Overvoltage

Overvoltage (or overcharge) protection is asserted when any cell voltage exceeds the V_{OV} threshold and remains above the V_{OV} threshold for a time exceeding a user-configurable delay (t_{OVD}). The $\overline{CHG}$ pin is driven high, disabling charge into the battery pack. Charging is disabled until a valid charge enable exists. See Charge Enable section.

Important note: If any battery pin floats (BAT_{1P}, $BAT_{1N–4N}$), the bq2058 assumes an overvoltage has occurred.

Because of different manufacturers specifications for overvoltage thresholds, the bq2058 can be available with different V_{OV} options. Table 2 summarizes these different voltage thresholds.

Table 2. Overvoltage Threshold Options

Part No.	V_{OV} Limit
bq2058	4.25V
bq2058C	4.325
bq2058D	4.30V
bq2058G*	4.375V
bq2058R	4.35V
bq2058W	3.4V

The overvoltage threshold limits are programmed at Unitrode. The bq2058 is the standard option that is more readily available for sampling and prototyping purposes. Please contact Unitrode for other voltage threshold and tolerance options.

Charge Enable

A valid charge enable indicates that an overvoltage (overcharge) condition no longer exists and that the pack is ready to accept further charge. Once overvoltage protection is asserted, charging will not be enabled until all cell voltages fall below V_{CE}. The V_{CE} threshold is a function of V_{OV}, and changes with different V_{OV} limits.

$$V_{CE} = V_{OV} - 150mV$$

Overcurrent

The bq2058 detects an overcurrent (or short circuit) condition only in the discharge direction. Overcurrent protection is asserted when either of the conditions occurs and remain for a time exceeding a user-configurable delay (t_{OCD}):

$$CSL > BAT_{4N} + V_{OCL}$$

$$CSH < BAT_{1P} - V_{OCH}$$

where:

$$V_{OCL} = 160mV\ (\text{low-side detect})$$

$$V_{OCH} = 160mV\ (\text{high-side detect})$$

When either of these conditions occurs, $\overline{DSG}$ is driven high, disconnecting the load from the pack. $\overline{DSG}$ remains high until both of the voltage conditions are false, indicating removal of the short-circuit condition. The user can facilitate clearing these conditions by inserting the battery pack into a charger.

The low-side overcurrent sense can be disabled by connecting CSL to BAT_{4N}. This ensures that CSL is never greater than BAT_{4N}. If low-side detection is disabled, high-side detection must be used with CSH.

The FETs in the charge/discharge path controlled by the $\overline{CHG}$ and $\overline{DSG}$ pins affect the overcurrent level. The on-resistance of these FETs need to be taken into account when determining overcurrent levels.

Condition	$\overline{CHG}$ pin	$\overline{DSG}$ pin
Normal operation	Low	Low
Overvoltage	High	Low
Undervoltage	Low	High
Overcurrent	Low	High
Floating battery input	High	Indeterminate
CTL = high	High	High

$\overline{CHG}$ and $\overline{DSG}$ States

The $\overline{CHG}$ and $\overline{DSG}$ output truth table is shown below.

The polarities of $\overline{CHG}$ and $\overline{DSG}$ are mask programmable at Unitrode. Push-pull vs. open-drain configuration is also mask-configurable at Unitrode. Please contact Unitrode for availability of these variations.

Number of Cells

The user must configure the bq2058 for three- or four-series cell operation. For a three-cell pack, NSEL should be tied directly to V_{SS}. For a four-cell pack, N_{SEL} should be connected directly to V_{CC}.

Number of Series Cells	NSEL
3-cell	Tied to V_{SS}
4-cell	Tied to V_{CC}

Pack Disable Input–CTL

The CTL pin is used to electrically disconnect the battery from the pack terminals through an externally supplied signal. When CTL is taken high, $\overline{CHG}$ and $\overline{DSG}$ are driven high. Any load on the pack terminals will be interpreted as an overcurrent condition by the bq2058 with the overcurrent delay timer held in reset. When the CTL pin is driven low, the overcurrent delay timer is allowed to start. If the programmed delay (t_{OCD}) is too short, the overcurrent recovery circuit, if implemented, will be unable to correct the overcurrent situation prior to the delay time-out. It is recommended that a delay time of greater than 10ms ($C_{OCD} \geq 0.01\mu F$) be used if the CTL pin function is used.

Important note: If CTL floats, it is internally pulled high making both $\overline{DSG}$ and $\overline{CHG}$ inactive, thus disabling the pack. If CTL is not used, it should be tied to V_{SS}.

The polarity of CTL is mask programmable at Unitrode. Please contact Unitrode for other polarity options.

Protection Delay Timers

The delay time between the detection of an overcurrent, overvoltage, or undervoltage condition and the deactivation of the $\overline{CHG}$ and/or $\overline{DSG}$ outputs is user-configurable by the selection of capacitor values between V_{CC} and OCD, OVD, and UVD pins (respectively). See Table 3 below.

The fault condition must persist through the entire delay period, or the bq2058 may not deactivate either FET control output.

Figure 3 shows a step-by-step event cycle for the bq2058.

Table 3. Protection Delay Timers

Protection Feature	Delay Period	Capacitor from V_{CC} to:	Typical		Tolerance
			Capacitor	Time	
Overcurrent	t_{OCD}	OCD	0.010µF	12ms	±40%
Overvoltage	t_{OVD}	OVD	0.100µF	950ms	±40%
Undervoltage	t_{UVD}	UVD	0.100µF	950ms	±40%

Notes:
1. The delay time versus capacitance can be approximated by the following equations:.
   For t_{OCD}: $t_{(s)} \approx 1.2 * C_{(\mu f)}$, where $C \geq 0.001\mu F$
   For t_{OVD}, t_{UVD}: $t_{(s)} \approx 9.5 * C_{(\mu f)}$, where $C \geq 0.01\mu F$
2. Overvoltage and undervoltage conditions are sampled by the bq2058. The delay in Table 2 is in addition to the time required for the bq2058 to detect the violation, which may vary from 0 to 160 ms depending on where in the sampling period the violation occurs. Overcurrent is continuously monitored and is subject to a delay of approximately 1.5ms.

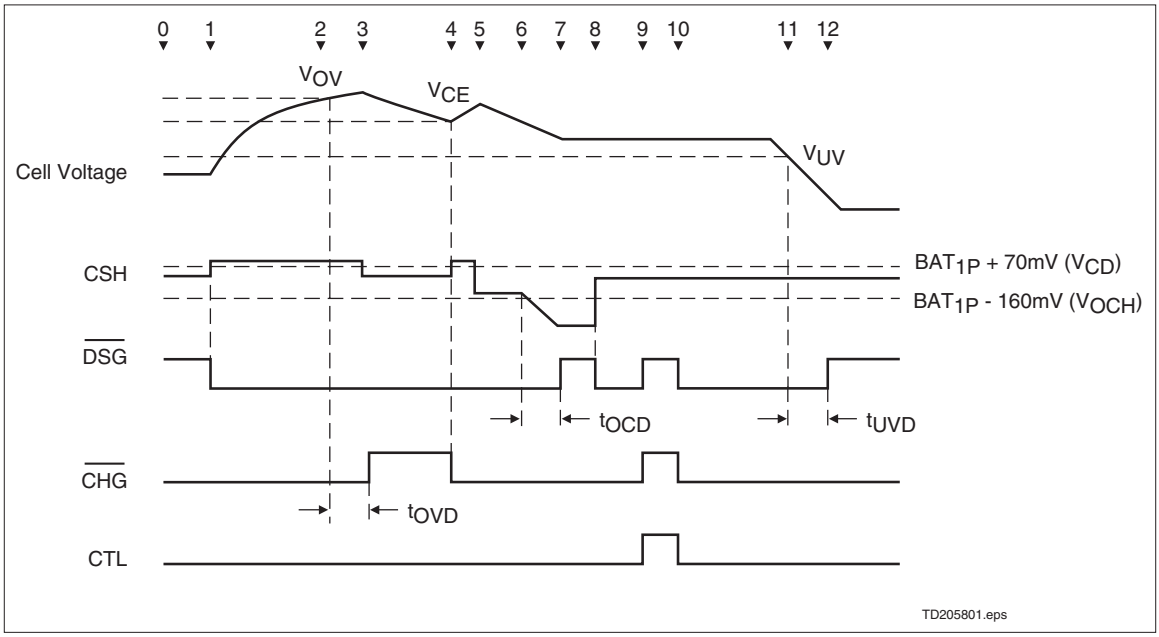


Figure 3. Protector Event Diagram

Event Definition:

0: The bq2058 is in the low-power sleep mode because one or more of the cell voltages are below V_{UV}.

1: A charger is applied to the pack, causing the difference between CSH and BAT_{1P} to become greater than 70mV. This awakens the bq2058, and the discharge pin $\overline{DSG}$ goes low.

2: One or more cells charge to a voltage equal to V_{OV}, initiating the overvoltage delay timer.

3: The overvoltage delay time expires, causing $\overline{CHG}$ to be driven high.

4: All cell voltages fall below V_{CE}, causing $\overline{CHG}$ to be driven low.

5: Stop charging, apply a load.

6: An overcurrent condition is detected, initiating the overcurrent delay timer.

7: The overcurrent delay time expires, causing $\overline{DSG}$ to be driven high.

8: The overcurrent condition is no longer present; $\overline{DSG}$ is driven low.

9: Pin CTL is driven high; both $\overline{DSG}$ and $\overline{CHG}$ are driven high.

10: Pin CTL is driven low; both $\overline{DSG}$ and $\overline{CHG}$ resume their normal function.

11: One or more cells fall below V_{UV}, initiating the overdischarge delay timer.

12: Once the overdischarge delay timer expires, if any of the cells is below V_{UV}, the bq2058 drives $\overline{DSG}$ high and enters the low-power sleep mode.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	Supply voltage	18	V	Relative to V_{SS}
T_{OPR}	Operating temperature	-30 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{IN}	Maximum input current	±100	µA	All pins except V_{CC}, V_{SS}

Notes: 1 Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

2. Internal protection diodes are in place on every pin relative to V_{CC} and V_{SS}. See Figure 4.

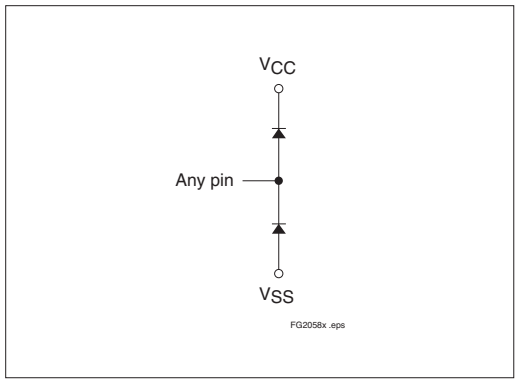


Figure 4. Internal Protection Diodes

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
V_{OH}	Output high voltage	V_{CC} - 0.5	-	-	V	I_{OH} = 10µA, $\overline{CHG}$, $\overline{DSG}$
V_{OL}	Output low voltage	-	-	V_{SS} + 0.5	V	I_{OL} = 10µA, $\overline{CHG}$, $\overline{DSG}$
V_{OP}	Operating voltage	4	-	18.0	V	V_{CC} relative to V_{SS}
V_{IL}	Input low voltage	-	-	V_{SS} + 0.5	V	Pin CTL
V_{IH}	Input high voltage	V_{SS} + 2.0	-	-	V	Pin CTL
V_{IL}	Input low voltage	-	-	V_{SS} + 0.5	V	Pin NSEL
V_{IH}	Input high voltage	V_{CC} - 0.5	-	-	-	Pin NSEL
I_{CCA}	Active current	-	25	40	µA	
I_{CCS}	Sleep current	-	0.7	1.5	µA	

DC Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Value	Unit	Tolerance	Conditons
V_{OV}	Overvoltage threshold (See Figure 5)	4.25	V	±50mV	See note 1
		4.375	V	±55mV	For bq2058G only See note 3
		Table 2			Customer option
V_{CE}	Charge enable threshold	V_{OV} - 150mV	V	±50mV	
		V_{OV} - 200mV	V	±50mV	For bq2058W only
V_{UV}	Undervoltage threshold	2.25	V	±100mV	
		2.10	V	±100mV	For bq2058W only
V_{OCH}	Overcurrent detect high-side	160	mV	±35mV	
V_{OCL}	Overcurrent detect low-side	160	mV	±35mV	
V_{CD}	Charge detect threshold	70	mV	-60mV, +80mV	
t_{OVD}	Overvoltage delay threshold	950	ms	±40%	C_{OVD} = 0.100µF, T_A = 30°C See note 2
t_{UVD}	Undervoltage delay threshold	950	ms	±40%	C_{UVD} = 0.100µF, T_A = 30°C See note 2
t_{OCD}	Overcurrent delay threshold	12	ms	±40%	C_{OCD} = 0.01µF, T_A = 30°C

Notes:
1. Standard device. Contact Unitrode for different thresholds and tolerance options.
2. Does not include cell sampling delay, which may add up to 160ms of additional delay until the condition is detected.
3. bq2058G is designed only for 3-cell applications.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_{CELL}	Input impedance	-	10	-	MΩ	Pins BAT_{1P}, BAT_{1N-4N}, CSH, CSL

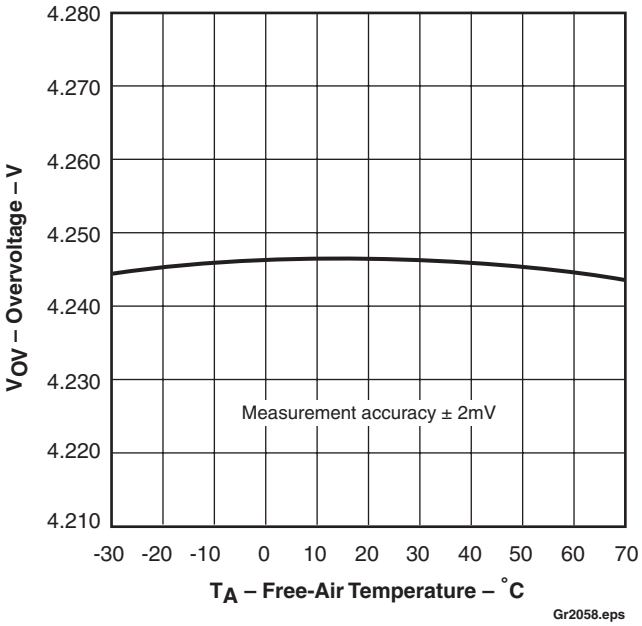


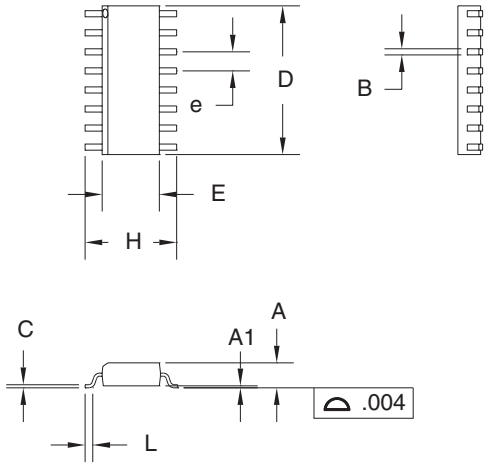
Figure 5. bq2058 4.25V Overvoltage Threshold vs. Free-Air Temperature

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	1, 2, 5	PACK+, PACK-	Pins renamed to CSH and CSL respectively
1	1	Pin description	Added CSH/CSL description
1	3	Block diagram	Update Block diagram
1	4	Figure 2	Update typical application circuit
1	4	Configuration description	Correction to description
1, 2	5	Overcurrent limits	Was: V_{OCH} = 150mV ± 25mV V_{OCL} = 85mV ± 25mV Is: V_{OCH} = 160mV ± 25mV V_{OCL} = 100mV ± 25mV
1	7	Figure 3	Update Event diagram
1, 2	9	DC threshold	Was: V_{OCH} = 150mV ± 25mV V_{OCL} = 100mV ± 80mV V_{CD} = 70mV -60, +50mV Is: V_{OCH} = 160mV ± 25mV V_{OCL} = 100mV ± 25mV V_{CD} = 70mV -60, +80mV
3	1, 3, 5	High-side overcurrent monitored	Was: Between V_{CC} and CSH, Is: Between BAT_{1P} and CSH
3	4	Overvoltage threshold options	Added bq2058R
3	3, 5	Overcurrent limit	Was: V_{OCL} = 100mV, Is: V_{OCL} = 150mV
4	4	Figure 2	Corrected schematic
4	6, 8	Protection Delay Times	Was: t_{OCD} = 10ms ±30% t_{OVD} = 800ms ±30% t_{UVD} = 800ms ±40% Is: t_{OCD} = 12ms ±40% t_{OVD} = 950ms ±40% t_{UVD} = 950ms ±40%
4	10	Overcurrent limits	Was: V_{OCH} = 160mV ±25mV V_{OCL} = 150mV ±25mV Is: V_{OCH} = 160mV ±35mV V_{OCL} = 160mV ±35mV
5	5, 9	Overvoltage threshold Charge enable threshold Undervoltage threshold	Added bq2058W
6	9	DC electrical characteristics	Was: Minimum V_{OP} = 0V, Is: Minimum V_{OP} = 4V
7	5, 9	Overvoltage threshold	Added bq2058C and bq2058G
8	4	Reference circuit amended	Moved D1 to new location

Notes: Change 1 = Feb. 1997 B changes from Jan. 1997 A. Change 2 = April 1997 C changes from Feb. 1997 B.
Change 3 = June 1997 D changes from April 1997 C. Change 4 = July 1997 E changes from June 1997 D.
Change 5 = Feb. 1998 F changes from July 1997 E. Change 6 = May 1998 G changes from Feb. 1998 F.
Change 7 = June 1998 H changes from May 1998 G.
Change 8 = Jan. 1999 I changes from June 1998 H.

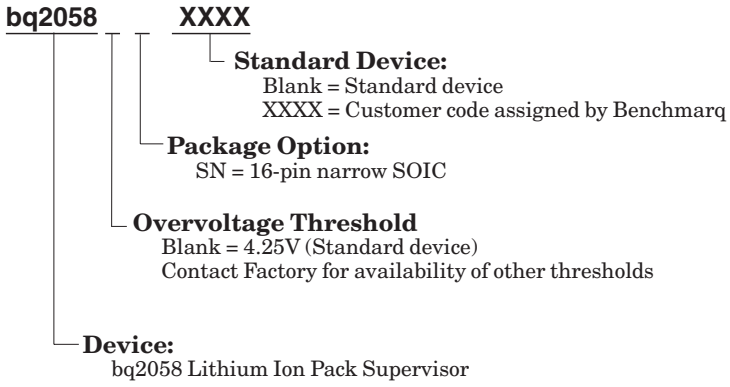
SN: 16-Pin SN (0.150" SOIC)



16-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.385	0.400	9.78	10.16
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

Ordering Information



Package Devices		
T_A	V_{OV} Threshold	16-pin Narrow SOIC (SN)
-30°C To +70°C	3.4V	bq2058WSN
	4.15V	bq2058MSN
	4.20V	bq2058FSN
	4.225V	bq2058KSN
	4.25V	bq2058SN
	4.325V	bq2058CSN
	4.30V	bq2058DSN
	4.35V	bq2058RSN
	4.36V	bq2058JSN
	4.375V	bq2058GSN

Notes: bq2058SN is Standard Device.
Contact factory for availability of other thresholds and tolerances.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.