HOLT INC.
INTEGRATED CIRCUITS

August 2014

DESCRIPTION

The HI-8588 is an ARINC 429 bus interface receiver and is available in a SO 8 pin package. The technology is analog/digital CMOS. The circuitry requires only a 5 volt supply.

The ARINC bus can be connected directly to the chip. The typical 10 volt differential signal is translated and input to a window comparator and latch. The comparator levels are just below the standard 6.5 volt minimum ARINC data threshold and just above the standard 2.5 volt maximum ARINC null threshold.

The TESTA and TESTB inputs bypass the analog for testing purposes. Also if TESTA and TESTB are both taken high, the analog powers down and the digital outputs tri-state allowing wire-or possibilities.

Please refer to the HI-8588-10 for applications where an external resistance in series with the ARINC inputs is required for lightning protection or when the digital outputs need to be a logic zero rather than open circuit when TESTA and TESTB are both high.

See Holt Application Note AN-300 for more information on lightning protection.

FEATURES

- Direct ARINC 429 line receiver interface in a small outline package

- Receiver input hystersis at least 2 volts

- Test inputs that bypass analog input and can power down and tri-state outputs

- Plastic and ceramic package options - surface mount and DIP

PIN CONFIGURATION

VCC - 1
TESTA - 2
RINB - 3
RINA - 4

8588PS

8 - TESTB
7 - ROUTB
6 - ROUTA
5 - GND
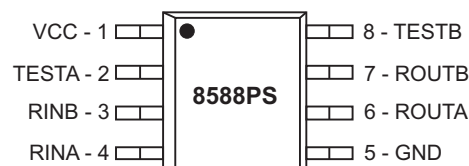
8 - PIN PLASTIC NARROW BODY SOIC

SUPPLY VOLTAGES

VCC = 5.0V ± 5%

FUNCTION TABLE

RECEIVER

RINA	RINB	TESTA	TESTB	ROUTA	ROUTB
-1.25V to 1.25V	-1.25V to 1.25V	0	0	0	0
-3.25V to -6.5V	3.25V to 6.5V	0	0	0	1
3.25V to 6.5V	-3.25V to -6.5V	0	0	1	0
X	X	0	1	0	1
X	X	1	0	1	0
X	X	1	1	HI-Z	HI-Z

PIN DESCRIPTION TABLE

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	VCC	SUPPLY	5 VOLT SUPPLY
2	TESTA	LOGIC INPUT	CMOS
3	RINB	ARINC INPUT	RECEIVER B INPUT
4	RINA	ARINC INPUT	RECEIVER A INPUT
5	GND	POWER	GROUND
6	ROUTA	LOGIC OUTPUT	RECEIVER CMOS OUTPUT A
7	ROUTB	LOGIC OUTPUT	RECEIVER CMOS OUTPUT B
8	TESTB	LOGIC INPUT	CMOS

FUNCTIONAL DESCRIPTION

RECEIVER

Figure 1 shows the general architecture of the ARINC 429 receiver. The receiver operates off the VCC supply only. The inputs RINA and RINB each have series resistors, typically 35K ohms. They connect to level translators whose resistance to Ground is typically 10K ohms. Therefore, any series resistance added to the inputs will affect the voltage translation.

After level translation, the inputs are buffered and become inputs to a differential amplifier. The amplitude of the differential signal is compared to levels derived from a divider between VCC and Ground. The nominal settings correspond to a One/Zero amplitude of 6.0V and a Null amplitude of 3.3V.

The status of the ARINC receiver input is latched. A Null input resets the latches and a One or Zero input sets the latches.

The logic at the output is controlled by the test signal which is generated by the logical OR of the TESTA and TESTB pins. If TESTA and TESTB are both One, then the receiver is powered down and the output pins float. The powerdown does not disconnect the internal resistors at the ARINC input.
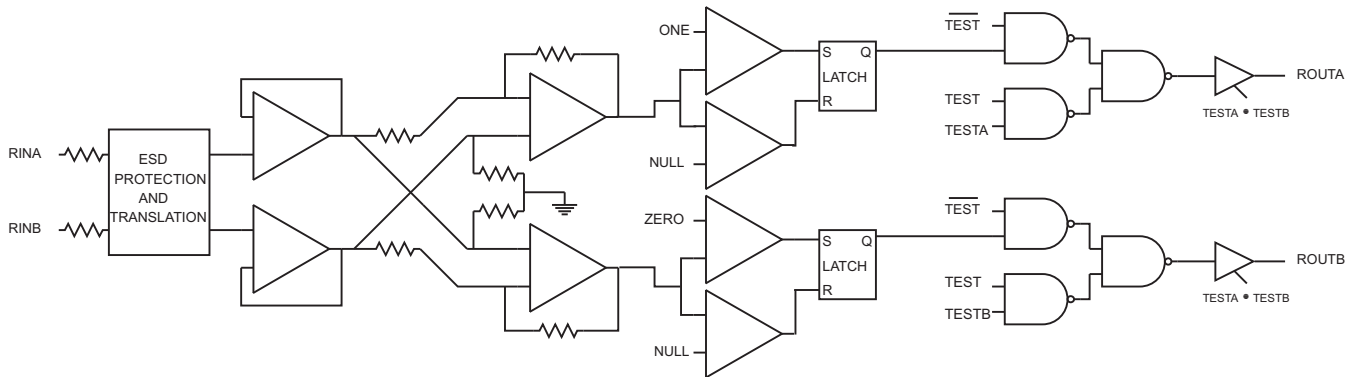

FIGURE 1 - RECEIVER BLOCK DIAGRAM

APPLICATION INFORMATION

Figure 2 shows a possible application of the HI-8588 interfacing an ARINC receive channel to the HI-6010 which in turn interfaces to an 8-bit bus.
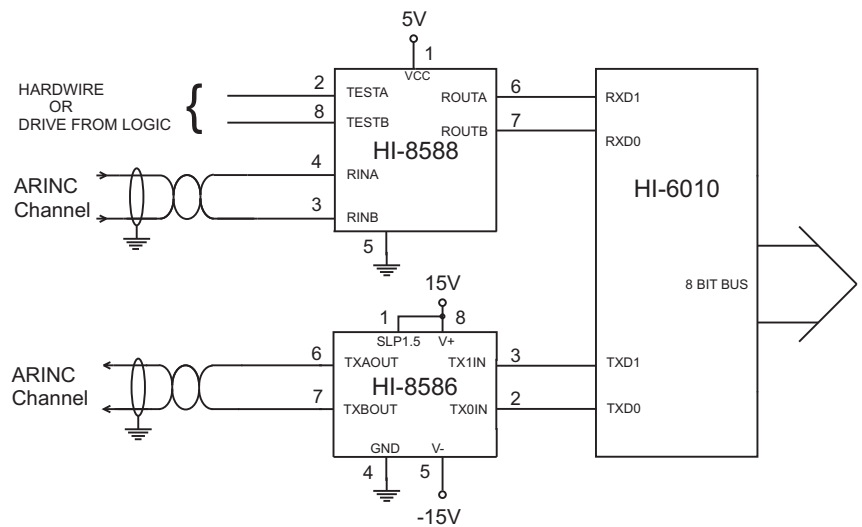

FIGURE 2 - APPLICATION DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground

Supply voltages   VCC...7V
ARINC input - pins 3 & 4   Voltage at either pin......+120V to -120V
DC current per input pin.................. ±10mA

Power dissipation at 25°C
    plastic DIP............0.7W
    ceramic DIP..........0.5W

Solder Temperature (reflow) ....260°C
Storage Temperature .... -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltages   VCC...5V ± 5%

Temperature Range
    Industrial Screening........-40°C to +85°C
    Hi-Temp Screening.......-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

OPERATING TEMPERATURE RANGE,   VCC = 5.0V UNLESS OTHERWISE STATED

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS

ARINC input voltage
    one or zero
    null
    common mode
	V_{DIN}
	V_{NIN}
	V_{COM}
		differential voltage, pins 3 & 4
		    " " "
		with respect to Ground
			6.5
			-
			-
				10
				-
				-
					13
					2.5
					5.0
						volts
						volts
						volts

logic input voltage
    high
    low
	V_{IH}
	V_{IL}
			3.5
			-
				-
				-
					-
					1.5
						volts
						volts

ARINC input resistance
    RINA to RINB
    RINA or RINB to Gnd or VCC
	R_{DIFF}
	R_{SUP}
		supplies floating
		    " "
			30
			19
				75
				40
					-
					-
						Kohm
						Kohm

logic input current
    source
    sink
	I_{IH}
	I_{IL}
		V_{IN} = 0 V
		V_{IN} = 5 V
			-
			-
				-
				-
					0.1
					0.1
						µA
						µA

logic output drive current
    one
    zero
	I_{OH}
	I_{OL}
		V_{OH}= 4.6V
		V_{OL} = 0.4V
			-
			3.6
				-1.6
				5.6
					-0.8
					-
						mA
						mA

Current drain
    operating
    powerdown
	I_{CC1}
	I_{CC2}
		pins 2, 8 = 0V; pins 3, 4 open
		pins 2, 8 = 5V; pins 3, 4 open
			-
			-
				2.3
				0.36
					6.3
					0.6
						mA
						mA

AC ELECTRICAL CHARACTERISTICS

OPERATING TEMPERATURE RANGE,   VCC = 5.0V UNLESS OTHERWISE STATED

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Receiver propagation delay		defined in Figure 3, C_L= 50pF				
Output high to low	t_{phlr}		-	600	-	ns
Output low to high	t_{plhr}		-	600	-	ns
Receiver output transition times						
Output high to low	t_{fr}		-	50	80	ns
Output low to high	t_{rr}		-	50	80	ns
Input capacitance (1)						
ARINC differential	C_{AD}		-	5	10	pF
ARINC single ended to Ground	C_{AS}		-	-	10	pF
Logic	C_{IN}		-	-	10	pF

Notes: 1. Guaranteed but not tested

FIGURE 3 - RECEIVER TIMING
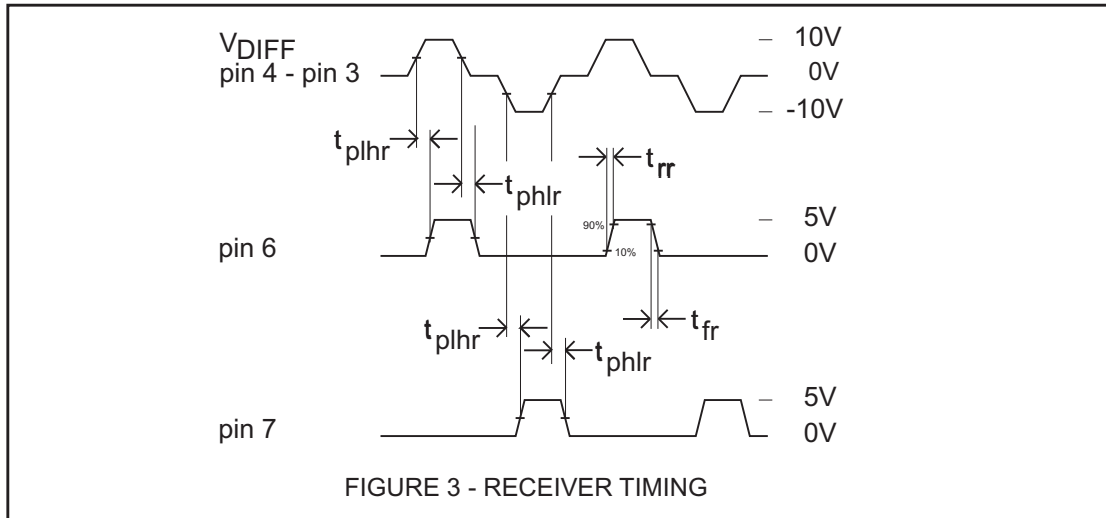
ORDERING INFORMATION

HI - 8588 xx x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No
M	-55°C TO +125°C	M	Yes

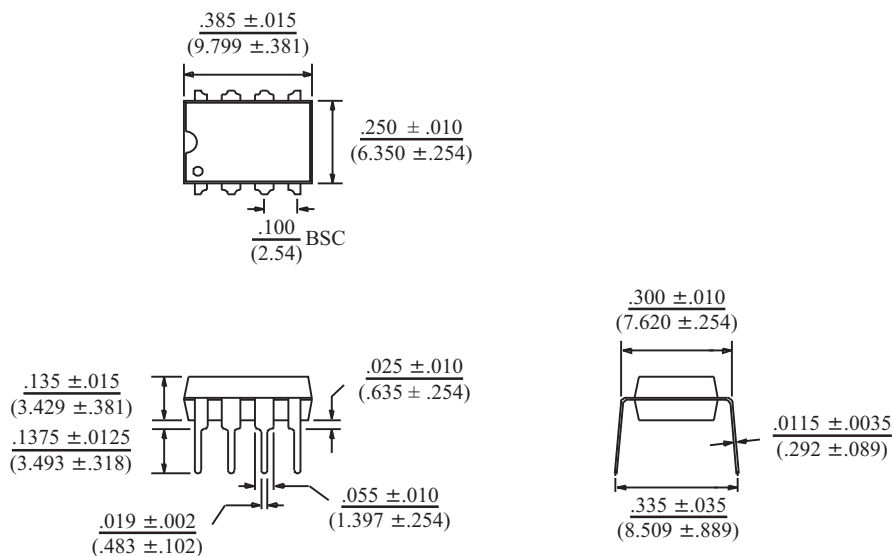| PART NUMBER	PACKAGE DESCRIPTION
PD	8 PIN PLASTIC DIP (8P) not available with "M" flow
PS	8 PIN PLASTIC NARROW BODY SOIC (8HN)
CR	8 PIN CERDIP (8D) not available Pb-free

REVISION HISTORY

P/N	Rev	Date	Description of Change
DS8488	E	08/05/14	Update ARINC input pins 3 & 4 Absolute Maximum Rating to +/-120V. Update solder reflow temperature. Remove Mil. temperature rating. Update SOIC-8 (8HN) package drawing.

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8-PIN PLASTIC DIP

inches (millimeters)

Package Type: 8P

.385 ±.015
(9.799 ±.381)

.250 ± .010
(6.350 ±.254)

.100
(2.54) BSC

.135 ±.015
(3.429 ±.381)

.1375 ±.0125
(3.493 ±.318)

.019 ±.002
(.483 ±.102)

.025 ±.010
(.635 ± .254)

.055 ±.010
(1.397 ±.254)

.300 ±.010
(7.620 ±.254)
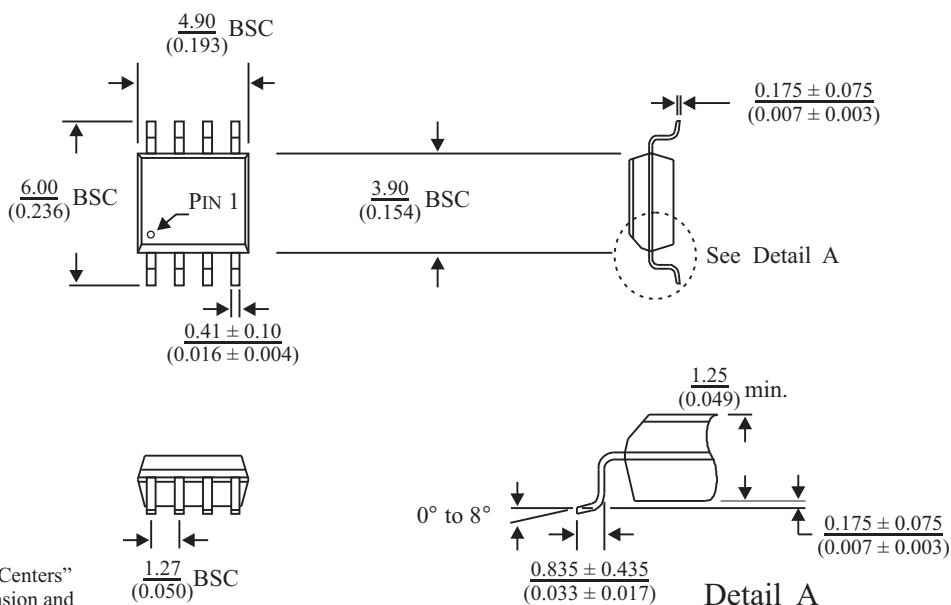
.0115 ±.0035
(.292 ±.089)

.335 ±.035
(8.509 ±.889)

BSC = "Basic Spacing between Centers"
is theoretical true position dimension and
has no tolerance. (JEDEC Standard 95)

8-PIN PLASTIC SMALL OUTLINE (SOIC) - NB
(Narrow Body)

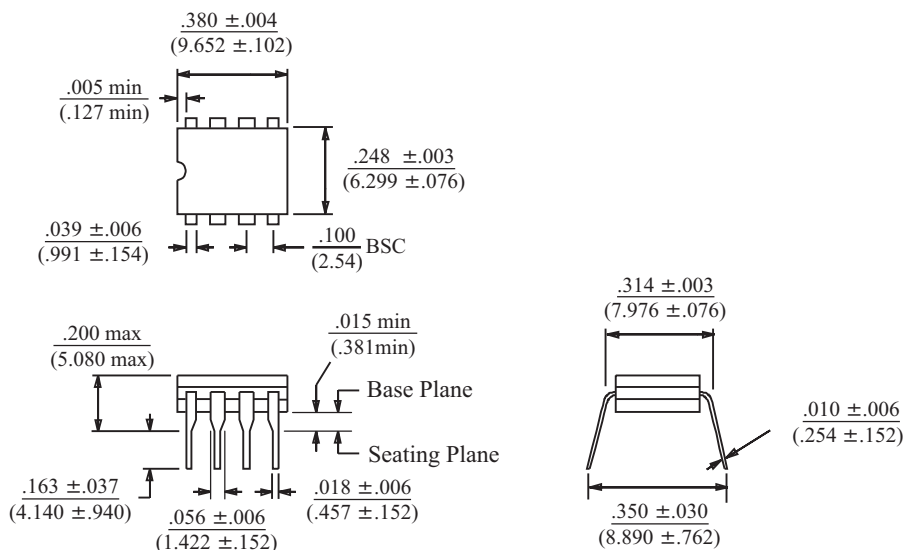*millimeters (inches)*

Package Type: 8HN

4.90
(0.193) BSC

6.00
(0.236) BSC

PIN 1

3.90
(0.154) BSC

0.41 ± 0.10
(0.016 ± 0.004)

0.175 ± 0.075
(0.007 ± 0.003)

See Detail A

1.25
(0.049) min.

0° to 8°

0.175 ± 0.075
(0.007 ± 0.003)

0.835 ± 0.435
(0.033 ± 0.017)

Detail A

1.27
(0.050) BSC

BSC = "Basic Spacing between Centers"
is theoretical true position dimension and
has no tolerance. (JEDEC Standard 95)

8-PIN CERDIP

inches (millimeters)

Package Type: 8D

.380 ±.004
(9.652 ±.102)

.005 min
(.127 min)

.248 ±.003
(6.299 ±.076)

.039 ±.006
(.991 ±.154)

.100
(2.54) BSC

.200 max
(5.080 max)

.015 min
(.381min)

Base Plane

Seating Plane

.163 ±.037
(4.140 ±.940)

.056 ±.006
(1.422 ±.152)

.018 ±.006
(.457 ±.152)

.314 ±.003
(7.976 ±.076)

.010 ±.006
(.254 ±.152)

.350 ±.030
(8.890 ±.762)

BSC = "Basic Spacing between Centers"
is theoretical true position dimension and
has no tolerance. (JEDEC Standard 95)