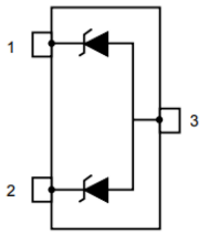
ESDAxxWY

Datasheet

Automotive dual-line unidirectional ESD protection in SOT323

SOT 323-3L (Jedec SC-70)



Pin layout

Product status link
ESDA5WY, ESDA14WY, ESDA18WY, ESDA37WY

Features

- AEC-Q101 qualified and PPAP capable
- Dual-line unidirectional ESD and EOS protection
- Very low leakage current at V_{RM} (I_R < 50 nA)
- Up to 300 W peak pulse power (8/20 µs)
- High ESD protection level: up to 30 kV
- Fast turn-on and low clamping voltage
- Operating T_j max: 175 °C
- SOT323-3L package
- ECOPACK2 RoHS compliant component
- Complies with the following standards:
  - J-STD-020 MSL level 1 and UL94, V0
  - IPC7531 footprint and JEDEC registered package
- Complies with ISO 10605 - C = 150 pF, R = 330 Ω:
  - ±30 kV (air discharge)
  - > ±25 kV (contact discharge)
- Complies with ISO 10605 - C = 330 pF, R = 330 Ω:
  - ±30 kV (air discharge)
  - > ±20 kV (contact discharge)
- Complies with ISO 7637-3:
  - Pulse 3a : -150 V; pulse 3b : +150 V
  - Pulse 2a: +/- 85 V

Application

Low speed and DC automotive applications where electrostatic discharges and other transients must be suppressed such as:

- MCUs and integrated circuits (SBC, DSP) low speed data lines and power lines
- MOSFET gate protection
- Switches and buttons
- Audio lines
- I2C, SPI communication bus

Description

ESDAxxWY series, automotive unidirectional transient voltage suppressor (TVS), has been designed for use in harsh environments to protect sensitive electronics from damage or latch-up due to electrical overstress (EOS), lightning surge and ESD without ageing effect and performance drifts.

It can therefore advantageously replace MOV (metal oxide varistor) or MLV (multi-layer varistor) as well as zener diodes, which are optimized for voltage regulation. It is the right choice for high reliability and quality systems.

In addition, this product is available in a small popular SOT323-3L (Jedec SC-70) with 2.1 mm x 2.0 mm package, ideal for space constrained applications.

1 Characteristics

1.1 Pin configuration and function

Table 1. ESDAxxWY series pin description

Pin #	Type	Description
1	I/O1	ESD protection cathode 1
2	I/O2	ESD protection cathode 2
3	GND	Common anode

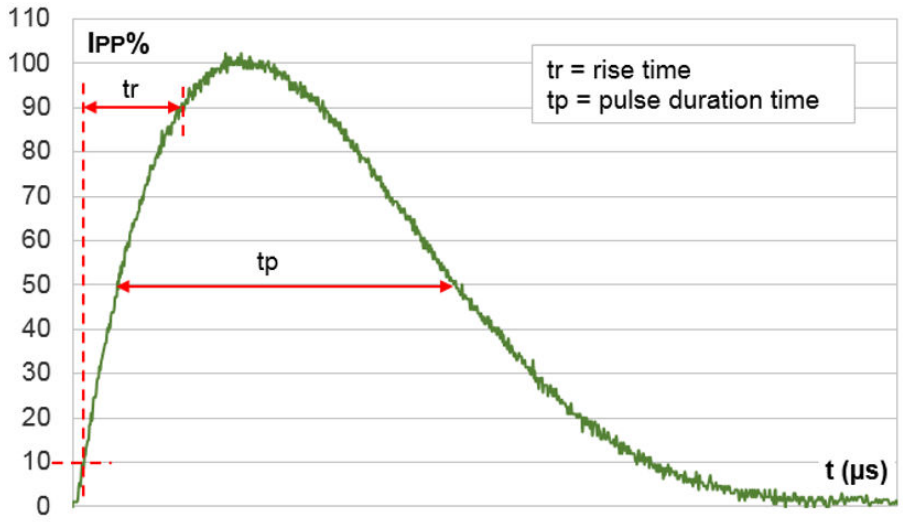
Figure 1. ESDAxxWY series pinout (top view)

1.2 Absolute maximum ratings

Table 2. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter			Value	Unit
V_{ESD}	Electrostatic discharge	ISO 10605 - C = 150 pF, R = 330 Ω: Contact discharge Air discharge	ESDA5WY	±25 ±30	kV
			ESDA14WY	±30 ±30	
			ESDA18WY		
			ESDA37WY		
		ISO 10605 - C = 330 pF, R = 330 Ω: Contact discharge Air discharge	ESDA5WY	±20 ±30	
			ESDA14WY	±30 ±30	
			ESDA18WY		
			ESDA37WY		
P_{PP}	Peak pulse power	IEC 61000-4-5 (2 Ω) – t_p = 8/20 µs	ESDA5WY	175	W
			ESDA14WY	250	
			ESDA18WY	290	
			ESDA37WY	300	
I_{PP}	Peak pulse current	IEC 61000-4-5 (2 Ω) – t_p = 8/20 µs	ESDA5WY	12	A
			ESDA14WY	13	
			ESDA18WY	11	
			ESDA37WY	6.3	
T_j	Operating junction temperature range			-55 to +175	°C
T_{stg}	Storage temperature range			-65 to +175	
T_L	Maximum lead temperature for soldering during 10 s			260	

Figure 2. Pulse definition for electrical characteristics



1.3 Electrical characteristics

Figure 3. **ESDA5WY - Electrical characteristics (definitions)**

V_{RM} Stand-off voltage
I_{RM} Leakage current @ VRM
V_{TRIG} Triggering voltage
V_H Holding voltage
V_{CL} Clamping voltage
I_{PP} Peak pulse current
V_F Forward voltage
I_F Current at V_F
R_D Dynamic resistance
C_L Line capacitance

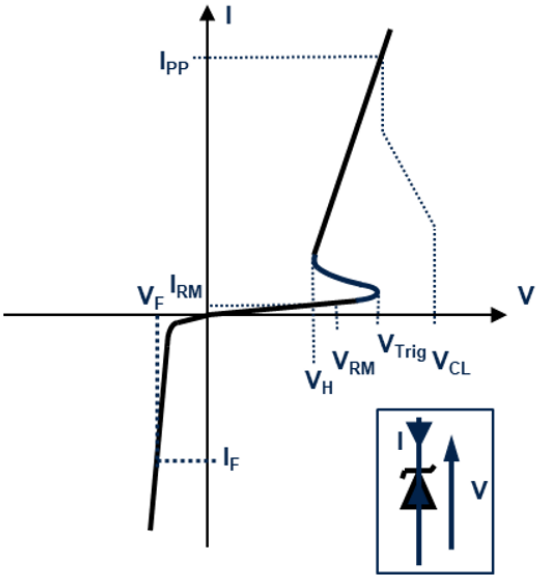


Table 3. **ESDA5WY - Electrical characteristics (T_{amb} = 25 °C, unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{RM}	Reverse stand-off voltage	Any I/O pin to GND			5.5	V
I_{RM}	Reverse leakage current at V_{RM}	V_{RM} = 5.5 V Any I/O pin to GND		3	50	nA
V_{TRIG}	Triggering voltage	Higher voltage than V_{TRIG} guarantees the protection turn-on Any I/O pin to GND	6.0		10	V
V_H	Holding voltage	Lower voltage than VH guarantees the protection turn-off Any I/O pin to GND	5.5			V
V_F	Forward voltage	I_F = 200 mA GND to any I/O pin		1.05	1.2	V
V_{CL}(1)	ESD clamping voltage	TLP measurement, t_P = 100 ns, I_{PP} = 16 A Any I/O pin to GND		14.0		V
	EOS clamping voltage	IEC 61000-4-5 surge, t_P = 8/20 µs, I_{PP} = 12 A Any I/O pin to GND			14.5	V
R_d(1)	Dynamic resistance	8/20 µs waveform Any I/O pin to GND		0.59		Ω
$C_{I/O-GND}$(1)	Line capacitance	V_R = 0 V, F = 1 MHz, V_{OSC} = 30 mV Any I/O pin to GND		4.0	4.8	pF
αT(1)(2)	Temperature coefficient	Any I/O pin to GND			3.5	10^{-4}/°C

1. *Specified by design – Not tested in production.*
2. *$\Delta V_{BR} = \alpha T \times (T_{amb} - 25\ °C) \times V_{BR}$ (25 °C)*

Figure 4. **Electrical characteristics - parameter definitions**

V_{RM}	Maximum stand-off voltage
I_{RM}	Maximum leakage current at V_{RM}
V_{BR}	Breakdown voltage at I_{BR}
I_{BR}	Breakdown current
V_{CL}	Clamping voltage at I_{PP}
I_{PP}	Peak pulse current
V_F	Forward voltage drop at I_F
I_F	Forward current
R_D	Dynamic resistance
αT	Voltage temperature coefficient

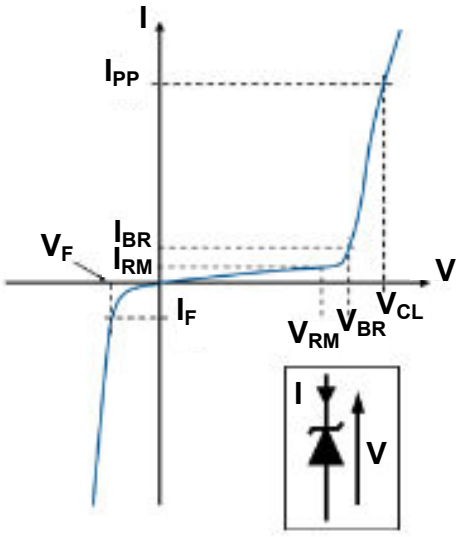


Table 4. **Electrical characteristics - parameter values (T_{amb} = 25 °C, unless otherwise specified)**

Type	I_{RM} at V_{RM}		V_{BR} at I_{BR}				8 / 20 µs(1)(2)			TLP 100 ns	C_L		αT(1)(3)	V_F at I_F	
							V_{CL}(4)	I_{PP}	R_D	V_{CL} at 16 A					
	Max.		Min.	Typ.	Max.		Max.	Max.	Typ.	Typ.	Typ.	Max.	Max.	Max.	
	µA	V	V	V	V	mA	V	A	Ω	V	pF	pF	10^{-4}/ °C	V	mA
ESDA14WY	0.05	12	14.2	15.4	16.8	1	23	13	0.41	17.5	125	150	8.7	1.2	200
ESDA18WY	0.05	16	18	19.3	20.5	1	27.7	11	0.61	21.7	95	120	8.7	1.2	200
ESDA37WY	0.1	36	37	41	43.3	1	61.3	6.3	2.4	50.5	48	58	11	0.9	10

1. *Specified by design – not tested in production.*
2. *Measured from pin 1 to 3 or pin 2 to pin 3, in accordance with IEC 61000-4-5 (8/20 µs current waveform).*
3. *To calculate V_{BR} or V_{CL} versus junction temperature, use the following formulas:*
   - *V_{BR} at T_J = V_{BR} at 25 °C x (1 + αT x (T_J - 25))*
   - *V_{CL} at T_J = V_{CL} at 25 °C x (1 + αT x (T_J - 25)).*
4. *To calculate maximum clamping voltage at other surge level, use the following formula:*
   - *V_{CL} max = V_{BR} max + R_D x $I_{PPappli}$*

   Where $I_{PPappli}$ is the surge current in the application.

1.4 Characteristics (curves)

Figure 5. Maximum peak current versus initial junction temperature

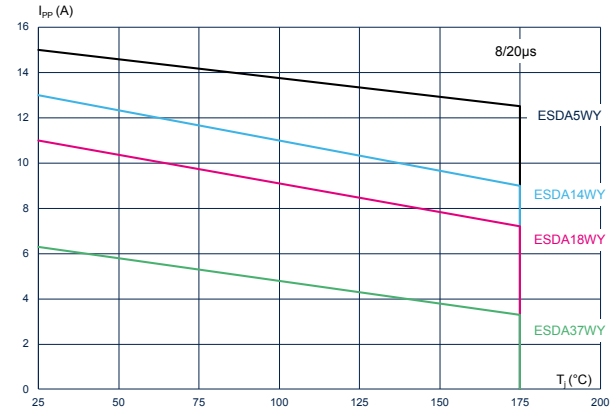


Figure 6. Maximum forward peak current versus initial junction temperature

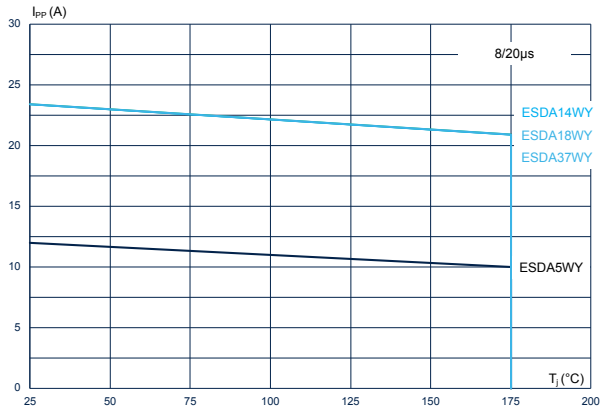


Figure 7. Maximum peak pulse current versus exponential pulse duration

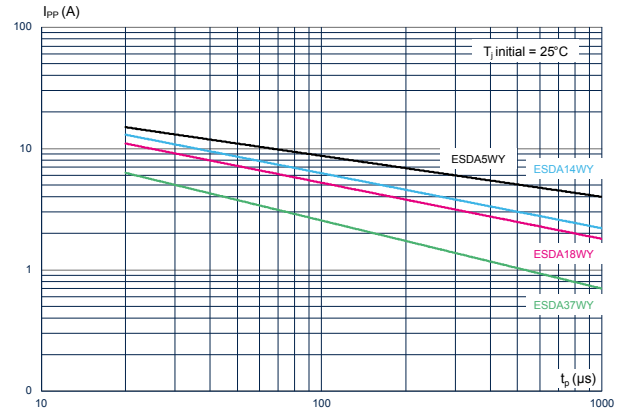


Figure 8. Maximum forward peak pulse current versus exponential pulse duration

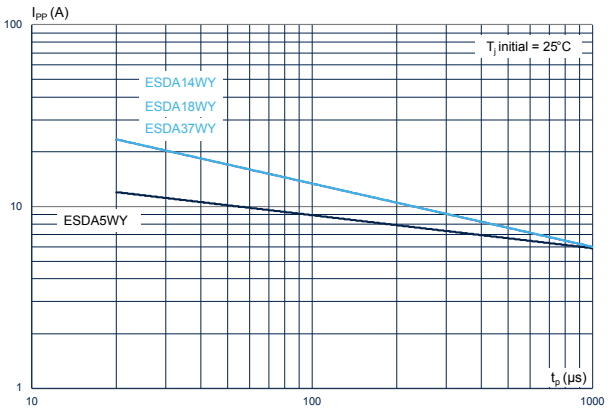


Figure 9. Peak pulse current versus clamping voltage (t_p = 8/20 µs)

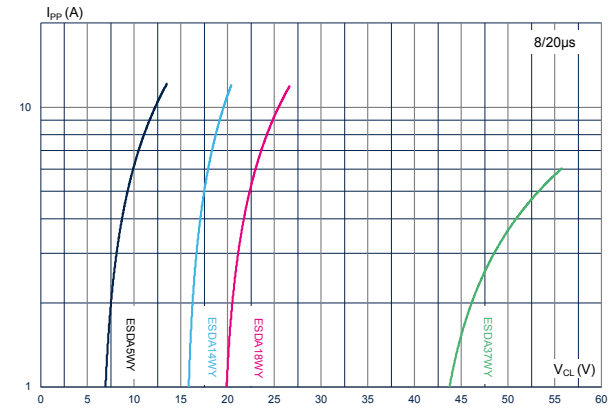


Figure 10. Peak forward current versus forward voltage drop (t_p = 8/20 µs)

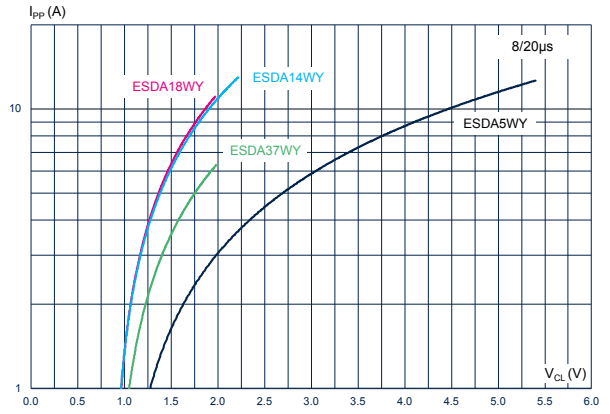


Figure 11. Junction capacitance versus reverse applied voltage

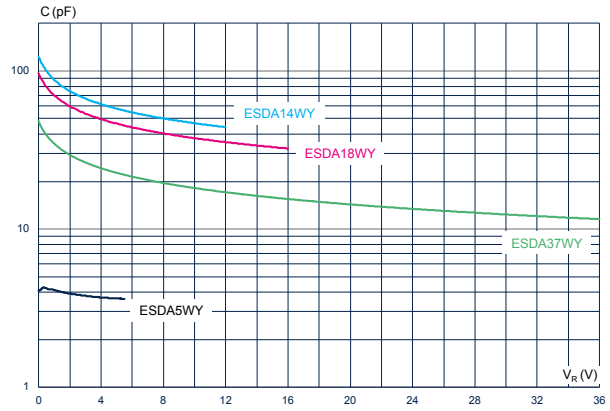


Figure 12. Leakage current at V_{RM} versus junction temperature

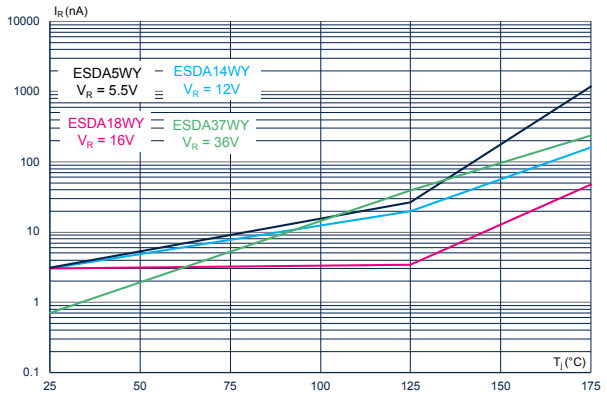


Figure 13. TLP characteristic - reverse

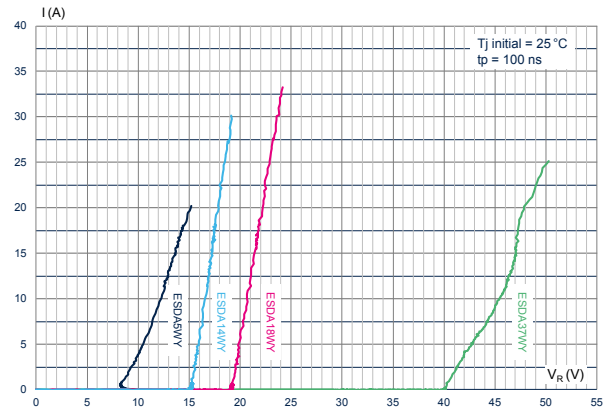


Figure 14. TLP characteristic - forward

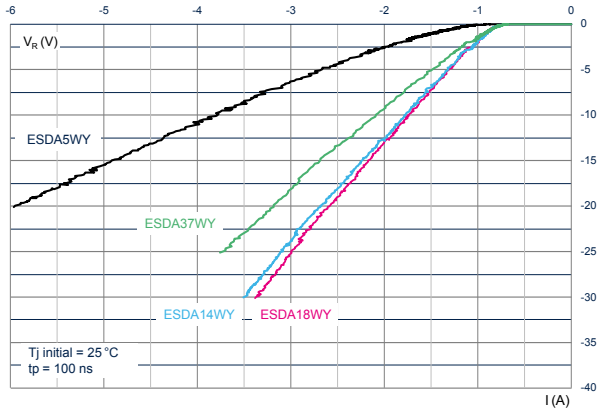


Figure 15. ESDA5WY Reponse to ISO 10605 C = 150 pF, R = 330 Ω (+8 kV contact)

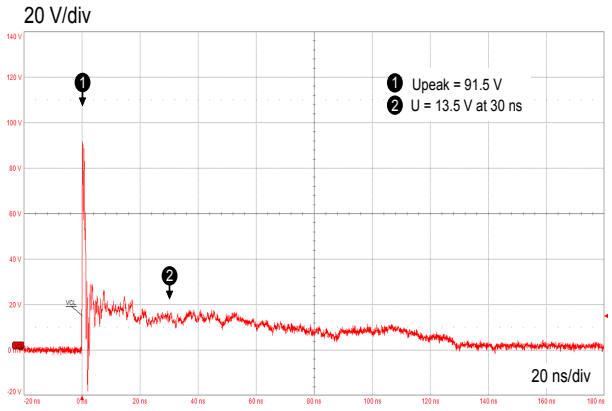


Figure 16. ESDA5WY Reponse to ISO 10605 C = 150 pF, R = 330 Ω (-8 kV contact)

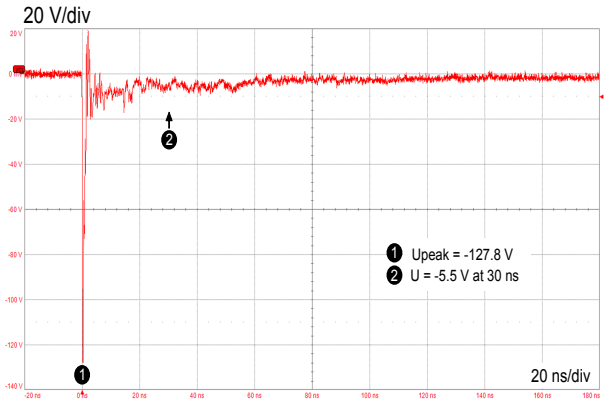


Figure 17. ESDA14WY / ESDA18WY Reponse to ISO 10605 C = 150 pF, R = 330 Ω (+8 kV contact)

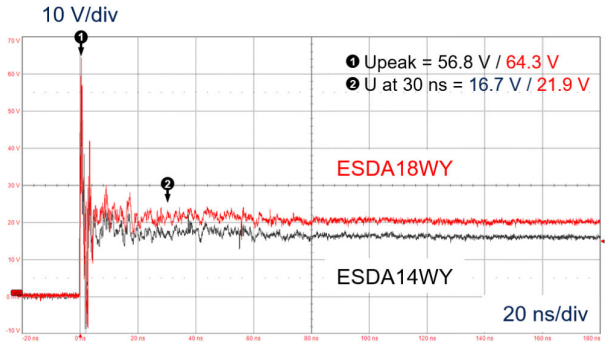


Figure 18. ESDA14WY / ESDA18WY Reponse to ISO 10605 C = 150 pF, R = 330 Ω , R = 330 Ω (-8 kV contact)

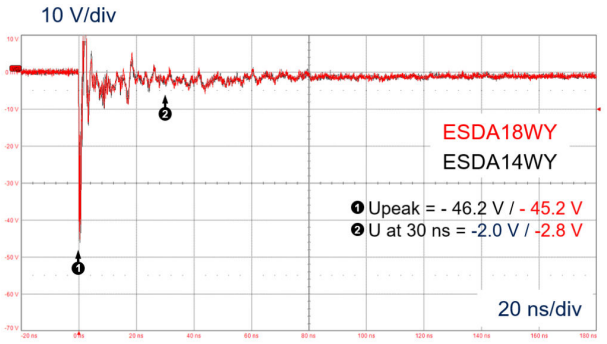


Figure 19. ESDA37WY - Reponse to ISO 10605 C = 150 pF, R = 330 Ω (+8 kV contact)

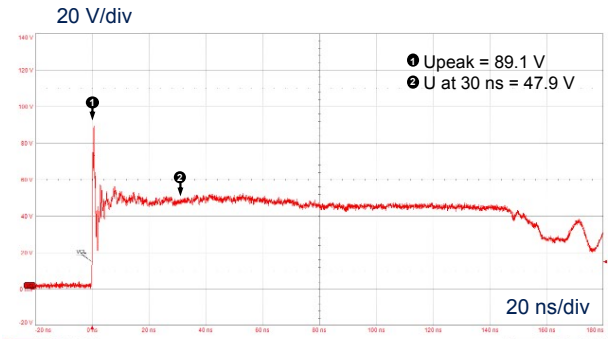


Figure 20. ESDA37WY - Reponse to ISO 10605 C = 150 pF, R = 330 Ω (-8 kV contact)

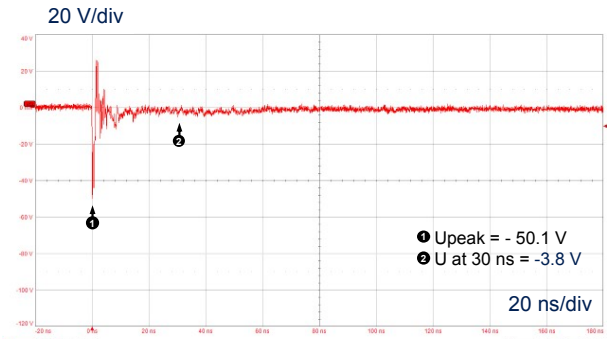


Figure 21. **ESDA5WY - Response to ISO 7637-3 Pulse 3a: -150 V**

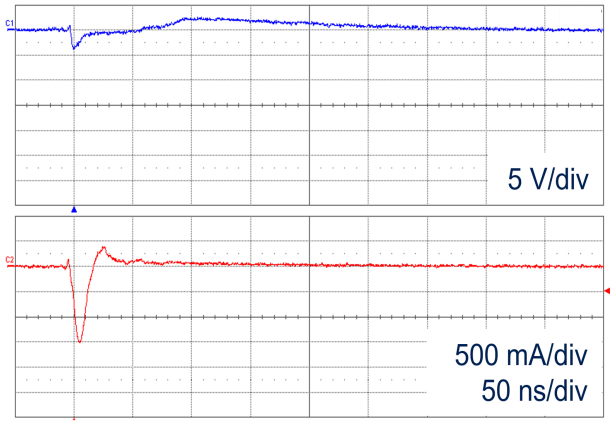


Figure 22. **ESDA5WY - Response to ISO 7637-3 Pulse 3b: +150 V**

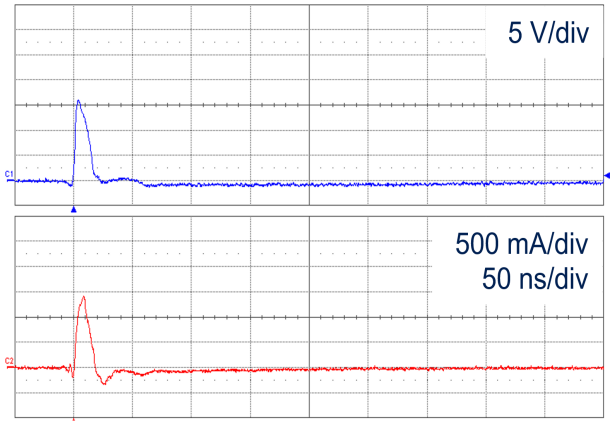


Figure 23. **ESDA14WY / ESDA18WY Response to ISO 7637-3 Pulse 3a: -150 V**

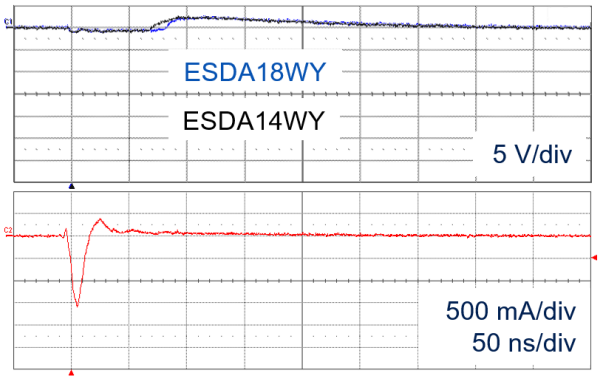


Figure 24. **ESDA14WY / ESDA18WY Response to ISO 7637-3 Pulse 3b: +150 V**

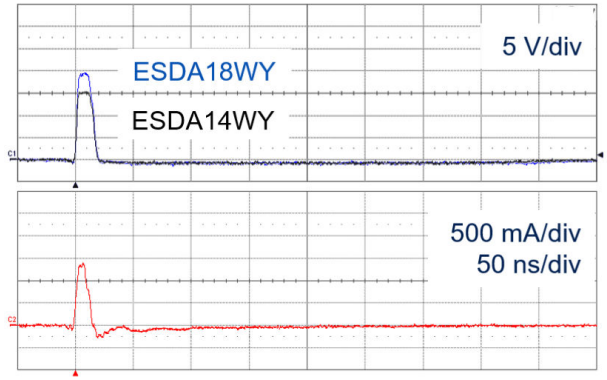


Figure 25. **ESDA37WY - Response to ISO 7637-3 Pulse 3a: -150 V**

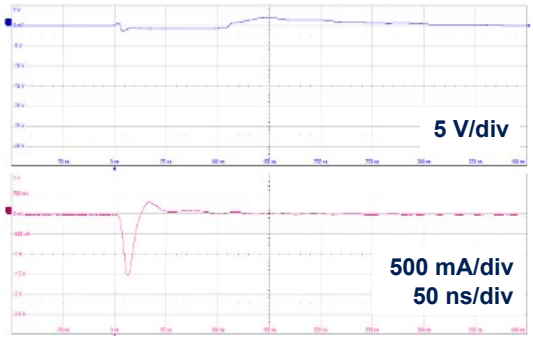


Figure 26. **ESDA37WY - Response to ISO 7637-3 Pulse 3b: +150 V**

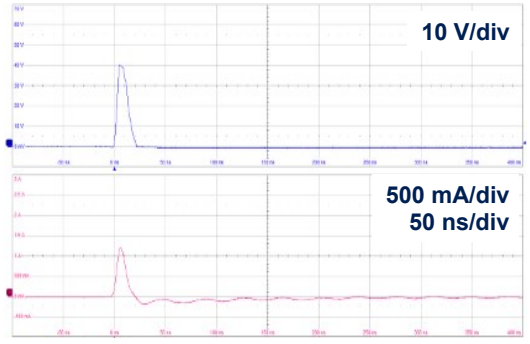


Figure 27. ESDA5WY - Response to ISO 7637-3 Pulse 2a: -85 V

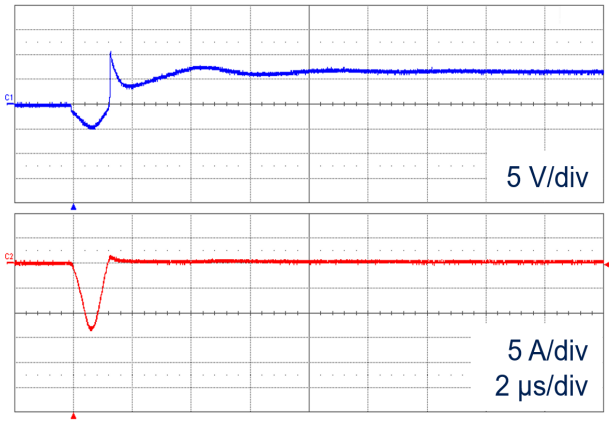


Figure 28. ESDA5WY - Response to ISO 7637-3 Pulse 2a: +85 V

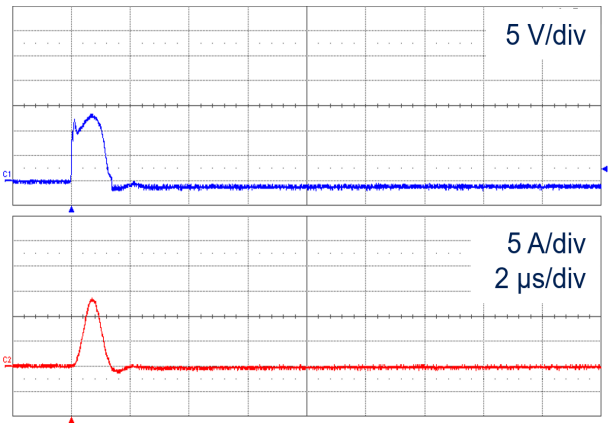


Figure 29. ESDA14WY / ESDA18WY Response to ISO 7637-3 Pulse 2a: -85 V

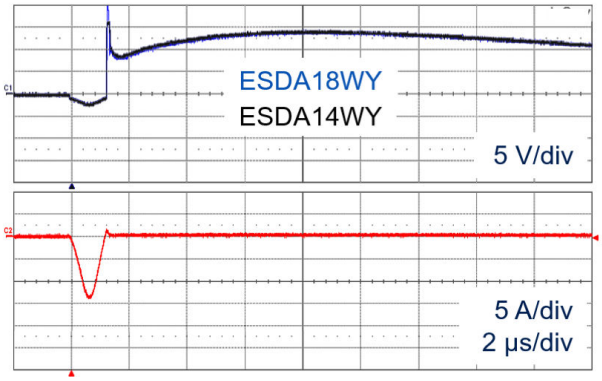


Figure 30. EESDA14WY / ESDA18WY Response to ISO 7637-3 Pulse 2a: +85 V

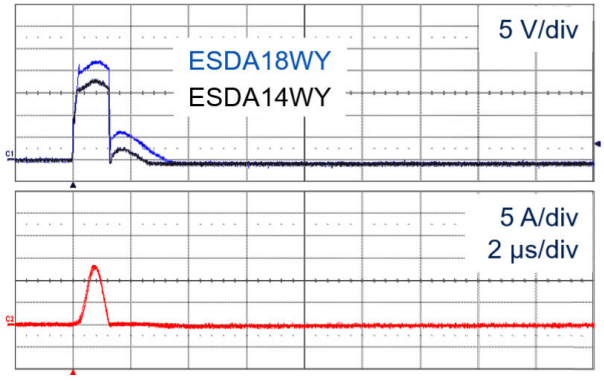


Figure 31. ESDA37WY - Response to ISO 7637-3 Pulse 2a: -85 V

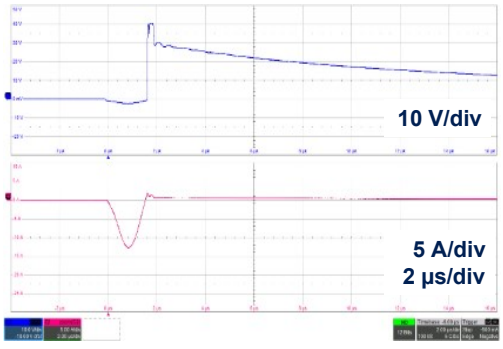
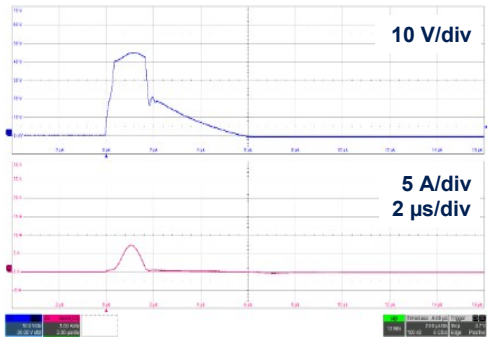


Figure 32. ESDA37WY - Response to ISO 7637-3 Pulse 2a: +85 V



Note: For additional recommendations, you can refer to STMicroelectronics application note AN2689:Protection of automotive electronics from electrical hazards, guidelines for design and component selection.

Note: DCC (direct capacitive coupling) for Figure 21 to Figure 32.

2 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 SOT323-3L package information

- Epoxy meets UL 94,V0
- Lead-free package

Figure 33. SOT323-3L package outline

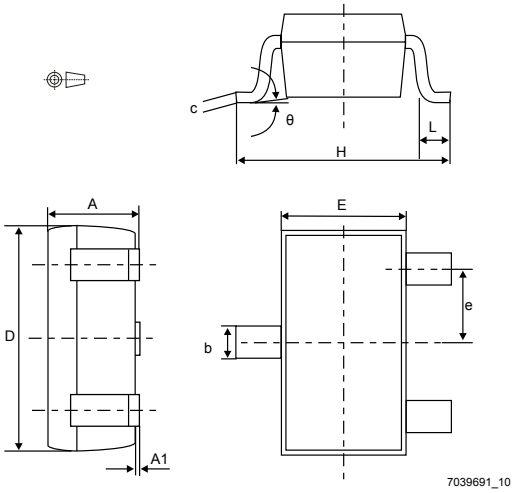


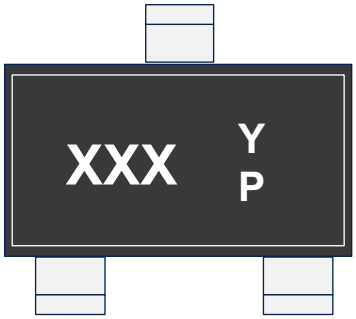
Table 5. SOT323-3L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.031		0.043
A1	0.00		0.10	0.000		0.003
b	0.25		0.40	0.0098		0.0157
c	0.10		0.26	0.003		0.0102
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.0452	0.0492	0.0531
e	0.60	0.65	0.70	0.024	0.026	0.028
H	1.80	2.10	2.40	0.070	0.082	0.094
L	0.10	0.20	0.30	0.004	0.008	0.012
Θ	0		30°	0		30°

1. *Values in inches are converted from mm and rounded to 3 or 4 decimal digits.*

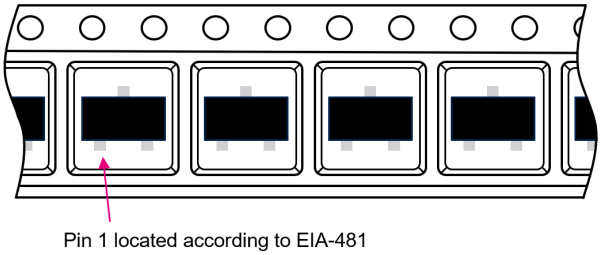
2.2 Packing and marking information

Figure 34. Marking layout



Y : Year
P : Assembly location
XXX: Marking value
Refer to Ordering information table

Figure 35. Package orientation in reel



Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale
Only pin 1 must be used to orient the component
for its placement on a PCB.

Figure 36. Reel dimensions (mm)

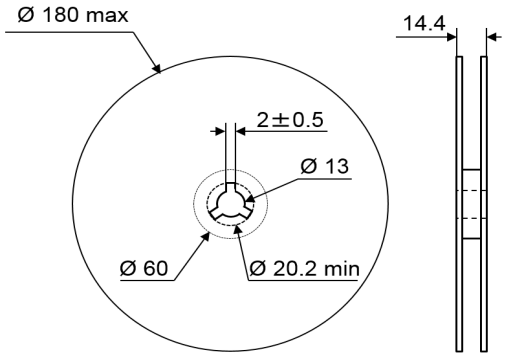


Figure 37. Tape and reel orientation

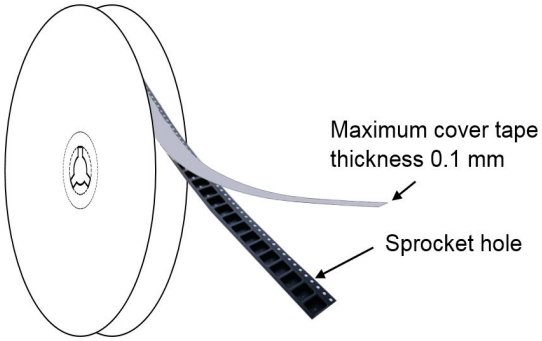


Figure 38. Inner box dimensions (mm)

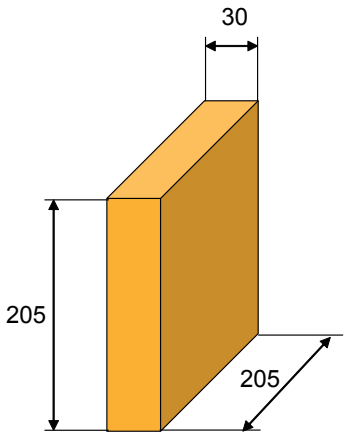
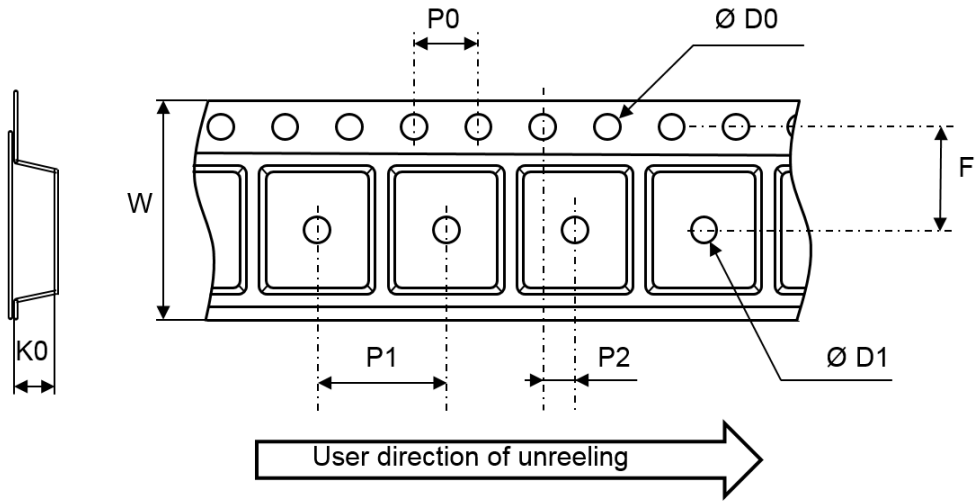


Figure 39. **Tape outline**

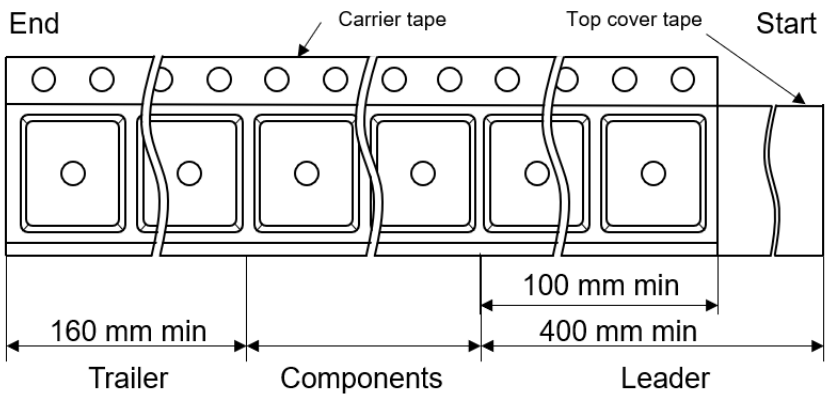


Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 6. **Tape and reel mechanical data**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
D0	1.50	1.55	1.60
D1	1.00		
F	3.45	3.50	3.55
K0	1.12	1.22	1.32
P0	3.90	4.00	4.10
P1	3.90	4.00	4.10
P2	1.95	2.00	2.05
W	7.90	8.00	8.30

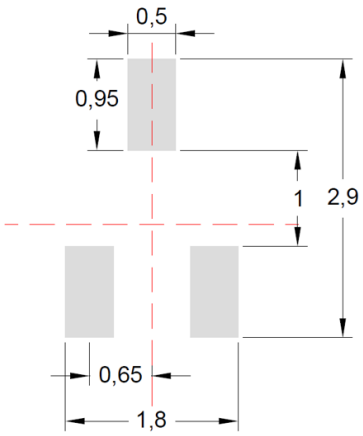
Figure 40. **Tape leader and trailer dimensions**



3 Recommendations on PCB assembly

3.1 Recommended footprint

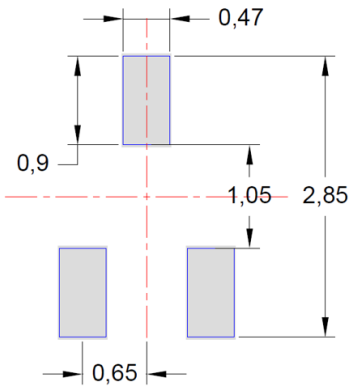
Figure 41. **Recommended footprint in mm**



3.2 Stencil opening design

- Stencil opening thickness: 75 µm to 125 µm / 3 mils to 5 mils
- Stencil opening ratio : 90%

Figure 42. **Stencil opening recommendations**



3.3 Solder paste

1. Halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Tack force high enough to resist component displacement during PCB movement.
4. Particles size 20-38 µm per IPCJ STD-005.

3.4 Placement

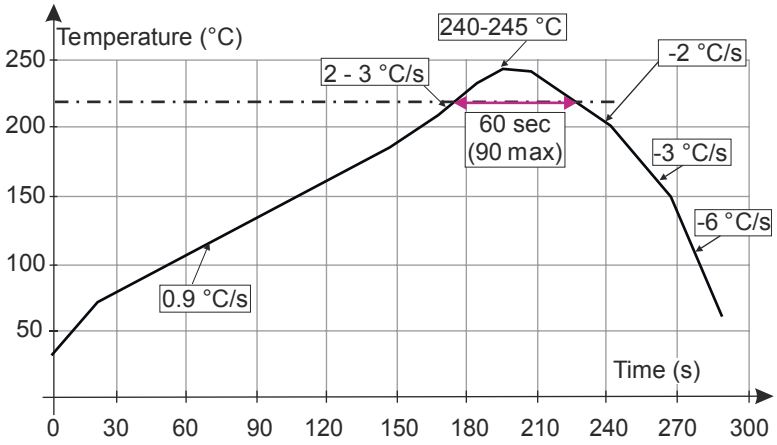
1. It is recommended to use leads recognition instead of package outline for accurate placement on footprint with adequate resolution tool.
2. Tolerance of ±50 µm is recommended.
3. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
4. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. Any via around or inside the footprint area must be closed to avoid solderpaste migration in the via.
2. Position and dimensions of the tracks should be well balanced. A symmetrical layout is recommended to prevent assembly troubles.

3.6 Reflow profile

Figure 43. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. O_2 rate inside the oven must be below 500 ppm. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 44. **Ordering information scheme**

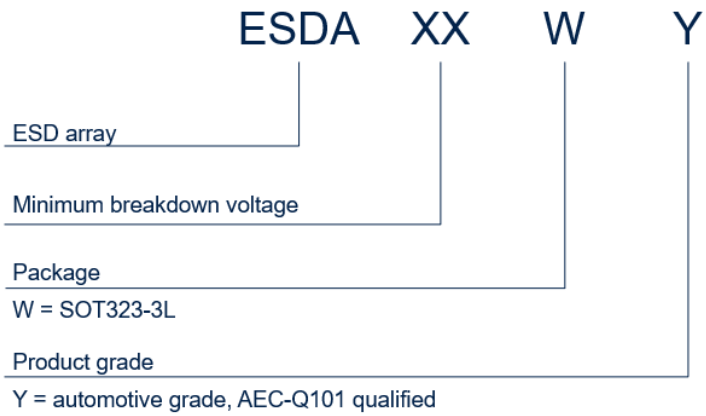


Table 7. **Ordering information**

Order code	Marking (1)	Package	Weight	Base qty.	Delivery mode
ESDA5WY	E5Y	SOT323-3L	6 mg	3000	Tape and reel
ESDA14WY	Y14		6.6 mg		
ESDA18WY	Y18				
ESDA37WY	E3Y				

1. *The marking can be rotated by multiples of 90° to differentiate assembly location*

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
16-Sep-2024	1	Initial release.
18-Jun-2025	2	Inserted ESDA5WY, and ESDA37WY products.
20-Jun-2025	3	Updated Table 7.

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