16-BIT SCRATCH PAD MEMORY CELL

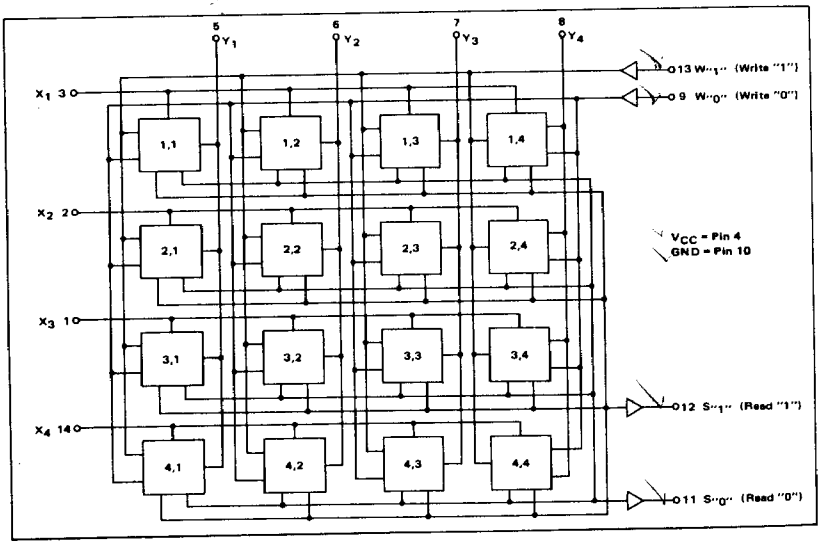
MC4004F,L*
MC4005F,L*

ADVANCE INFORMATION / NEW PRODUCT

The MTTL 16-Bit Memory Cell can serve as the basic building block for scratch pad memory systems having cycle times of less than 100 ns. The basic cell provides 16 words of one-bit memory operating in the non-destructive readout (NDRO) mode.

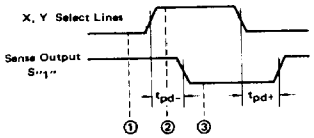
The memory circuit operates from a nominal 5.0 volt power supply and is designed with inputs and outputs compatible with MTTL and MDTL logic circuits.

The MTTL 16-Bit Memory Chip contains 16 flip-flops arranged in a four-by-four matrix. A single bit of the matrix is selected by driving one of four X select lines and one of four Y select lines above the select threshold. Two sense amplifiers are shared by all 16 bits and provide a double rail output from the selected bit. The sense output of many chips can be "wired ORed" together since the output stage does not have a pullup resistor or network. Two write amplifiers allow a "1" or a "0" to be written into a selected bit.



—OPERATING SEQUENCE—

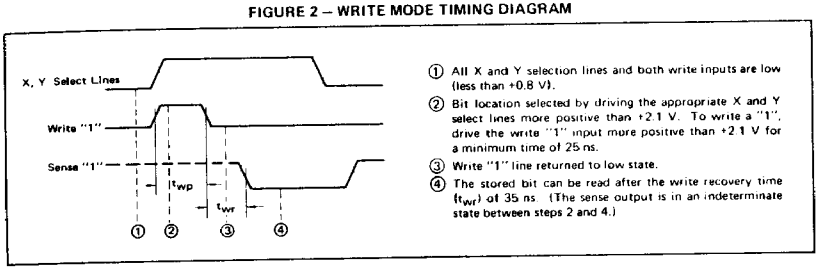
FIGURE 1 – READ MODE TIMING DIAGRAM



1. All X and Y selection lines and both write inputs are low (less than +0.8 V).
2. Desired bit selected by driving the appropriate X and Y select lines more positive than +2.1 V.
3. After the turn-on delay time (t_{pd-}), the S"1" output will be low (less than +0.45 V) and the S"0" output will be high (more than +2.5 V), providing that a "1" is stored in the selected bit.

*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in line package (Case 632)

FIGURE 2 – WRITE MODE TIMING DIAGRAM



① All X and Y selection lines and both write inputs are low (less than +0.8 V).
② Bit location selected by driving the appropriate X and Y select lines more positive than +2.1 V. To write a "1", drive the write "1" input more positive than +2.1 V for a minimum time of 25 ns.
③ Write "1" line returned to low state.
④ The stored bit can be read after the write recovery time (t_{wr}) of 35 ns. (The sense output is in an indeterminate state between steps 2 and 4.)

MAXIMUM RATINGS

RATING	VALUE	UNIT
Supply Voltage	7.0	Vdc
Supply Operating Voltage Range	4.5 to 5.5	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range	0 to +75	°C
Storage Temperature Range	-65 to +200	°C

POWER CHARACTERISTICS

V_{CC} = 5.0 V
I_{Supply} = 65 mA max @ 25°C, all inputs grounded.
Power Dissipation (P_D) = 250 mW typical

APPLICATION

The memory cell offers 16 words of one bit memory. A scratch pad memory constructed from the cell can be expanded in multiples of 16 words, and by paralleling cells, can have any bit length. A 64 word by 4 bit memory would require 16 cells.

OPERATING CHARACTERISTICS

SELECTION	CHARACTERISTIC	VALUE
X, Y	Address line logic "0" input forward current	11 mA max.
X, Y	Address line logic "1" input leakage current	0.4 mA max.
X, Y	Address line threshold voltage for writing or reading	2.1 Vdc min.
X, Y	Address line threshold voltage to inhibit writing	0.8 Vdc min.
X, Y	Address line threshold voltage to inhibit reading	1.0 Vdc max.
WRITE MODE	Write amplifier logic "0" input forward current	1.33 mA max.
	Write amplifier logic "0" input leakage current	0.1 mA max.
	Write amplifier logic "1" threshold voltage	2.1 Vdc
	Write amplifier logic "0" threshold voltage	1.0 Vdc
	Write pulse (t_{wp})	25 ns min.
	Write recovery time (t_{wr})	35 ns max.
READ MODE	Sense output logic "0" voltage	0.45 V max.
	Turn-on delay (t_{pd-})	20 ns max.
	Turn-off delay (t_{pd+})	20 ns max.
	SENSE AMPLIFIER DRIVE CAPABILITIES	
	MC4004 – 40 mA @ +0.45 V max.	
	MC4005 – 20 mA @ +0.45 V max.	

The DSP56008 signals that may be programmed as General Purpose I/O are listed with their primary function in **Table 3-9**.

Table 3-9 DSP56002 General Purpose I/O Pin Identification in PGA Package

Pin Number	Primary Function	Port	GPIO ID
E11	H0	B	PB0
D11	H1		PB1
C11	H2		PB2
E10	H3		PB3
D10	H4		PB4
B12	H5		PB5
A11	H6		PB6
B11	H7		PB7
C9	HA0		PB8
B9	HA1		PB9
A9	HA2		PB10
D9	$\overline{\text{HR/W}}$		PB11
B10	$\overline{\text{HEN}}$		PB12
C10	$\overline{\text{HREQ}}$		PB13
A10	$\overline{\text{HACK}}$		PB14
C12	RXD	C	PC0
D12	TXD		PC1
E12	SCLK		PC2
F11	SC0		PC3
G12	SC1		PC4
F13	SC2		PC5
F12	SCK		PC6
G13	SRD		PC7
G11	STD		PC8
H11	TIO	No port assigned	