

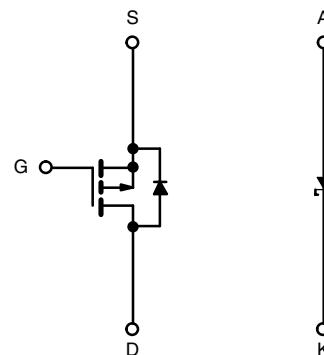
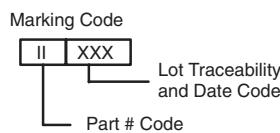
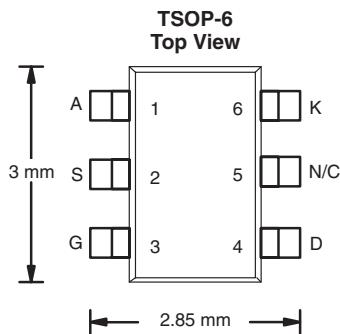
P-Channel 20-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 20	0.084 at $V_{GS} = - 10$ V	- 3.3	4 nC
	0.108 at $V_{GS} = - 4.5$ V	- 2.9	
	0.175 at $V_{GS} = - 2.5$ V	- 2.3	

SCHOTTKY PRODUCT SUMMARY

V_{KA} (V)	V_f (V) Diode Forward Voltage	I_F (A) ^a
20	0.5 at 1 A	2



Ordering Information: Si3805DV-T1-E3 (Lead (Pb)-free)
Si3805DV-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- LITTLE FOOT® Plus Schottky Power MOSFET
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- HDD
 - DC-DC Converter

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage (MOSFET)	V_{DS}	- 20	V
Reverse Voltage (Schottky)	V_{KA}	20	
Gate-Source Voltage (MOSFET)	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) (MOSFET)	$T_C = 25^\circ\text{C}$	I _D	- 3.3
	$T_C = 70^\circ\text{C}$		- 2.7
	$T_A = 25^\circ\text{C}$		- 3.0 ^{b, c}
	$T_A = 70^\circ\text{C}$		- 2.4 ^{b, c}
Pulsed Drain Current (MOSFET)	I _{DM}	- 15	A
Continuous Source-Drain Diode Current (MOSFET Diode Conduction)	$T_C = 25^\circ\text{C}$	I _S	- 1.2
	$T_A = 25^\circ\text{C}$		- 0.9 ^{b, c}
Average Forward Current (Schottky)	I _F	2 ^b	
Pulsed Forward Current (Schottky)	I _{FM}	5	W
Maximum Power Dissipation (MOSFET)	$T_C = 25^\circ\text{C}$	P _D	1.4
	$T_C = 70^\circ\text{C}$		0.9
	$T_A = 25^\circ\text{C}$		1.1 ^{b, c}
	$T_A = 70^\circ\text{C}$		0.7 ^{b, c}
Maximum Power Dissipation (Schottky)	$T_C = 25^\circ\text{C}$	P _D	1.4
	$T_C = 70^\circ\text{C}$		0.9
	$T_A = 25^\circ\text{C}$		1.1 ^{b, c}
	$T_A = 70^\circ\text{C}$		0.7 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{std}	- 55 to 150	°C

Si3805DV

Vishay Siliconix



THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET) ^{b, d}	$t \leq 5 \text{ s}$	R_{thJA}	93	110	°C/W
Maximum Junction-to-Foot (Drain) (MOSFET)	Steady State	R_{thJF}	75	90	
Maximum Junction-to-Ambient (Schottky) ^{b, e}	$t \leq 5 \text{ s}$	R_{thJA}	97	115	
Maximum Junction-to-Foot (Drain) (Schottky)	Steady State	R_{thJF}	78	95	

Notes:

- a. Based on $T_C = 25 \text{ °C}$.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. $t = 5 \text{ s}$
- d. Maximum under Steady State conditions is 150 °C/W.
- e. Maximum under Steady State conditions is 155 °C/W.

SPECIFICATIONS $T_J = 25 \text{ °C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = - 250 \mu\text{A}$	- 20			V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = - 250 \mu\text{A}$		- 20		mV/°C	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			3			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = - 250 \mu\text{A}$	- 0.6		- 1.5	V	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = - 20 \text{ V}, V_{GS} = 0 \text{ V}$			- 1	μA	
		$V_{DS} = - 20 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55 \text{ °C}$			- 10		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq 5 \text{ V}, V_{GS} = - 4.5 \text{ V}$	- 15			A	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = - 10 \text{ V}, I_D = - 3.0 \text{ A}$		0.070	0.084	Ω	
		$V_{GS} = - 4.5 \text{ V}, I_D = - 2.6 \text{ A}$		0.090	0.108		
		$V_{GS} = - 2.5 \text{ V}, I_D = 2.1 \text{ A}$		0.140	0.175		
Forward Transconductance ^a	g_{fs}	$V_{DS} = - 10 \text{ V}, I_D = - 3.0 \text{ A}$		6		S	
Dynamic^b							
Input Capacitance	C_{iss}	$V_{DS} = - 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		330		pF	
Output Capacitance	C_{oss}			80			
Reverse Transfer Capacitance	C_{rss}			57			
Total Gate Charge	Q_g	$V_{DS} = - 10 \text{ V}, V_{GS} = - 10 \text{ V}, I_D = - 3.0 \text{ A}$		8	12	nC	
Gate-Source Charge	Q_{gs}			4	6		
Gate-Drain Charge	Q_{gd}	$V_{DS} = - 10 \text{ V}, V_{GS} = - 4.5 \text{ V}, I_D = - 3.0 \text{ A}$		0.8			
Gate Resistance	R_g			1.4			
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = - 10 \text{ V}, R_L = 4.2 \Omega$ $I_D \equiv - 2.4 \text{ A}, V_{GEN} = - 10 \text{ V}, R_g = 1 \Omega$		1.2	6	12	Ω
Rise Time	t_r				3	6	
Turn-Off DelayTime	$t_{d(off)}$				10	20	
Fall Time	t_f				16	24	
Turn-On Delay Time	$t_{d(on)}$				8	15	
Rise Time	t_r	$V_{DD} = - 10 \text{ V}, R_L = 4.2 \Omega$ $I_D \equiv - 2.4 \text{ A}, V_{GEN} = - 4.5 \text{ V}, R_g = 1 \Omega$			18	27	ns
Turn-Off DelayTime	$t_{d(off)}$				40	60	
Fall Time	t_f				18	27	
					10	15	

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			- 1.2	A
Pulse Diode Forward Current	I_{SM}				- 15	
Body Diode Voltage	V_{SD}	$I_S = -1.0\text{ A}$, $V_{GS} = 0\text{ V}$		- 0.75	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -2.4\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$		23	35	ns
Body Diode Reverse Recovery Charge	Q_{rr}			14	21	nC
Reverse Recovery Fall Time	t_a			11		ns
Reverse Recovery Rise Time	t_b			12		

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

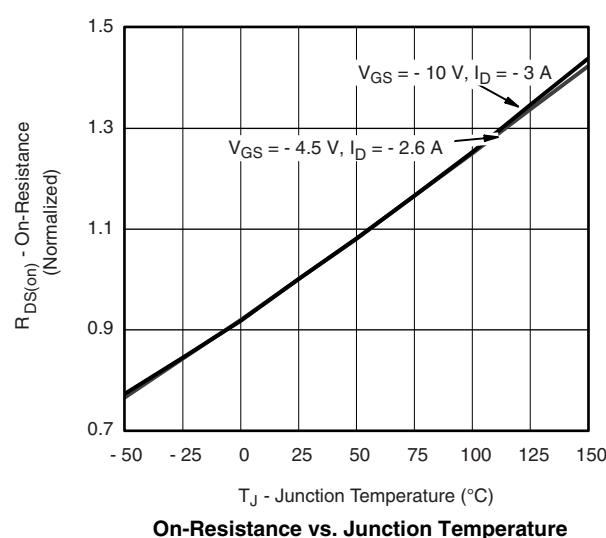
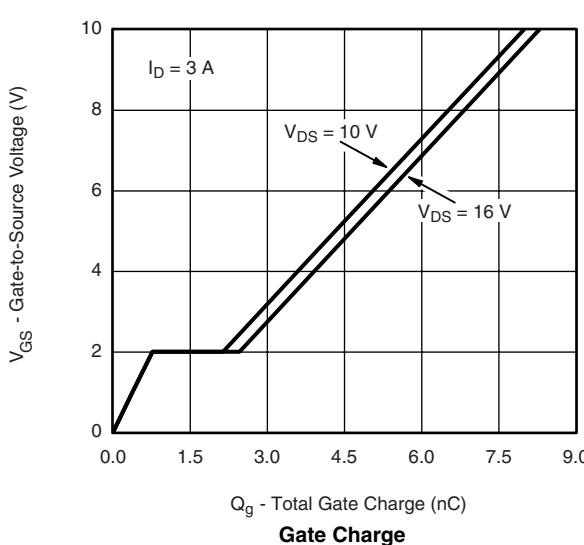
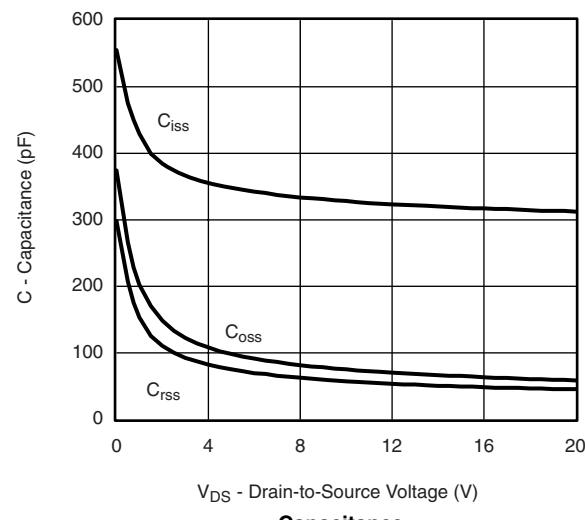
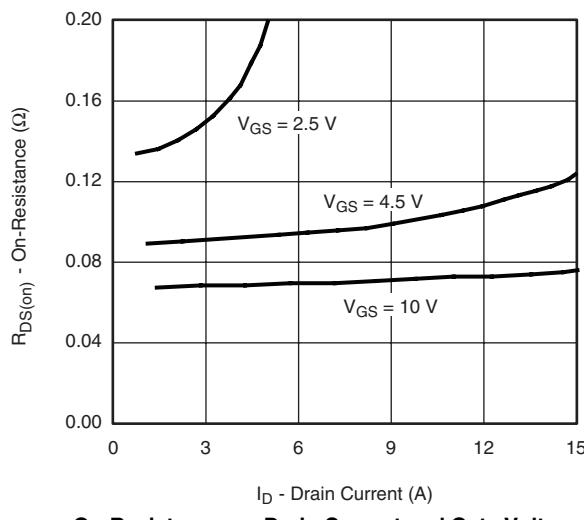
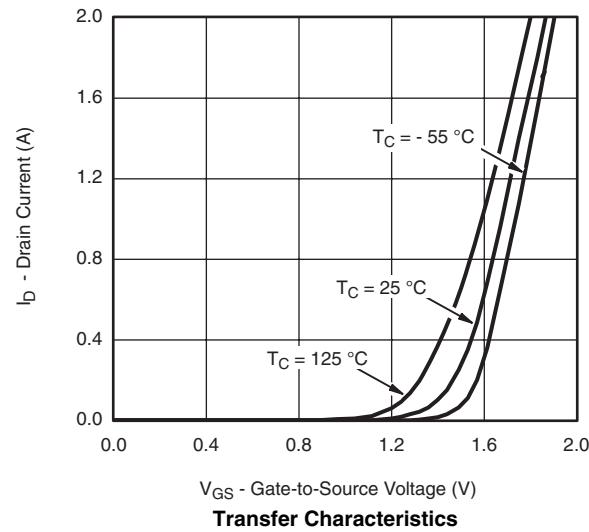
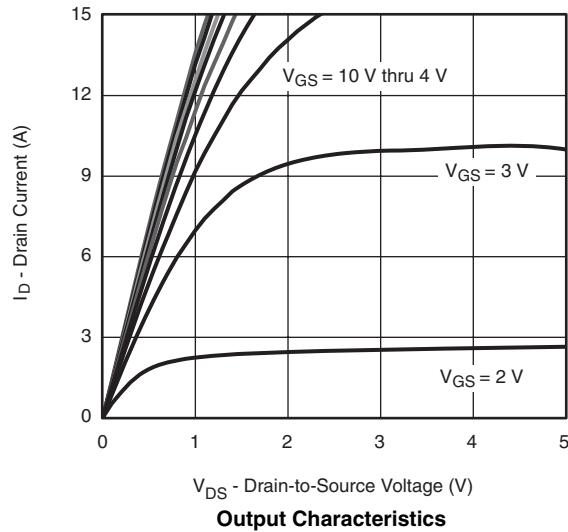
SCHOTTKY SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

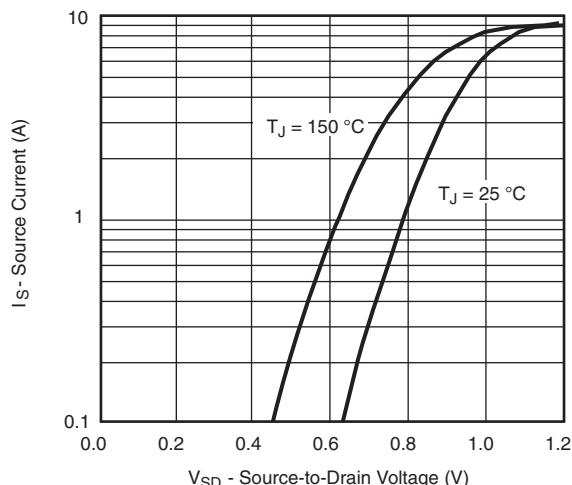
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Forward Voltage Drop	V_F	$I_F = 1\text{ A}$		0.42	0.50	V
		$I_F = 1\text{ A}$, $T_J = 125^\circ\text{C}$		0.36	0.43	
Maximum Reverse Leakage Current	I_{rm}	$V_r = 5\text{ V}$		0.015	0.08	mA
		$V_r = 5\text{ V}$, $T_J = 85^\circ\text{C}$		0.50	5.00	
		$V_r = 20\text{ V}$		0.02	0.10	
		$V_r = 20\text{ V}$, $T_J = 85^\circ\text{C}$		0.7	7.00	
		$V_r = 20\text{ V}$, $T_J = 125^\circ\text{C}$		5	50	
Junction Capacitance	C_T	$V_r = 10\text{ V}$		60		pF

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

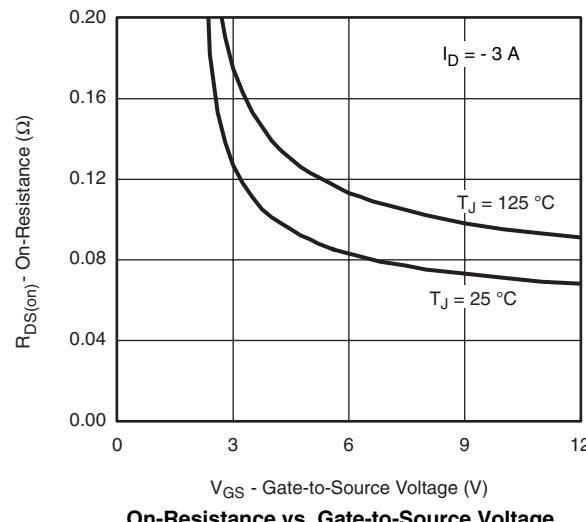
Si3805DV

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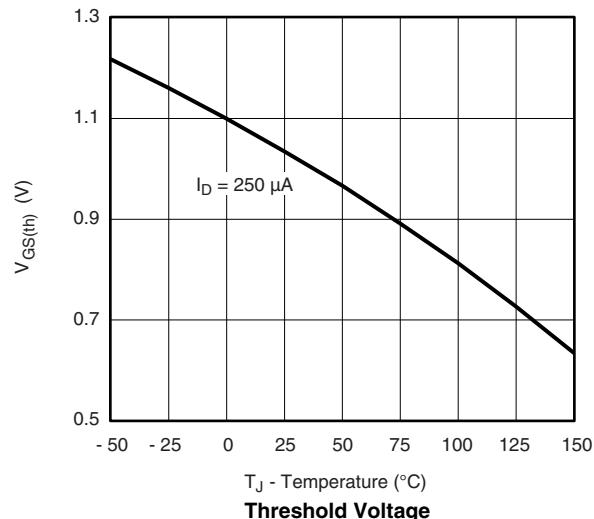
**MOSFET TYPICAL CHARACTERISTICS** $T_A = 25^\circ\text{C}$, unless otherwise noted

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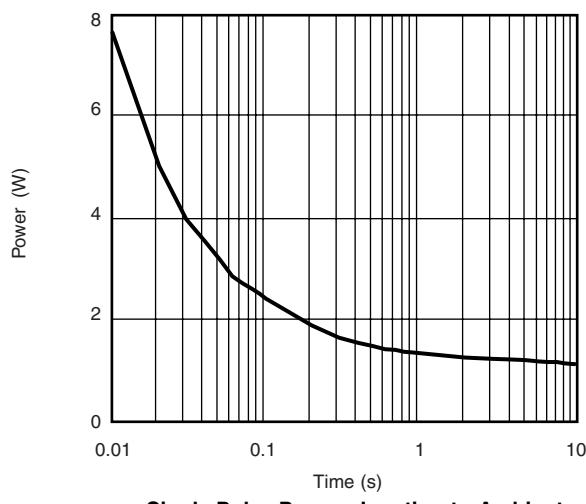
Source-Drain Diode Forward Voltage



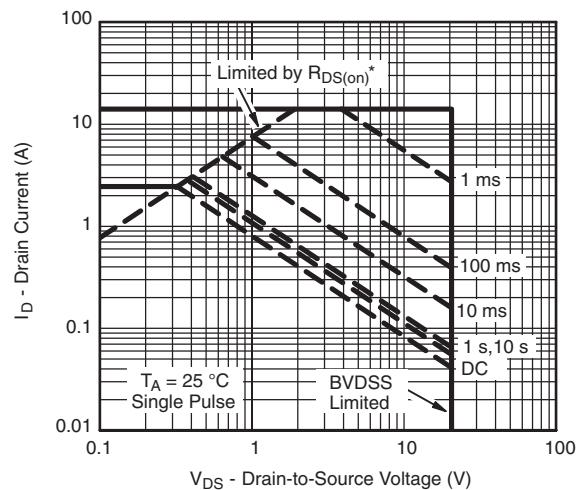
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



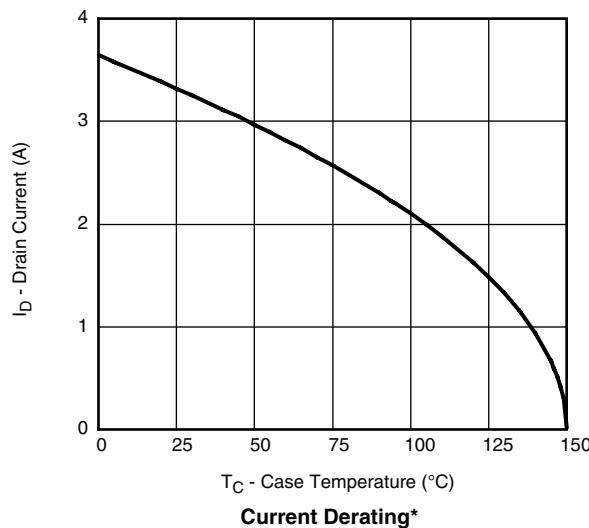
Single Pulse Power, Junction-to-Ambient

* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

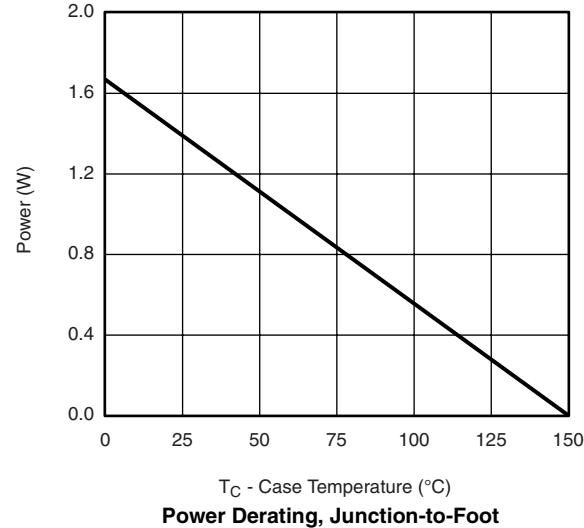
Safe Operating Area, Junction-to-Case

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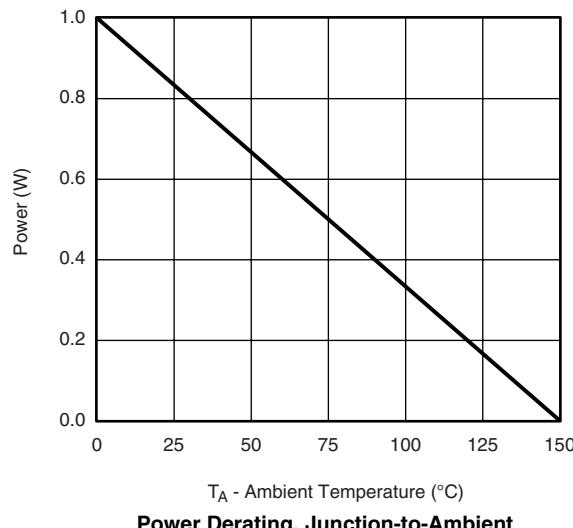
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**MOSFET TYPICAL CHARACTERISTICS** $T_A = 25^\circ\text{C}$, unless otherwise noted

Current Derating*



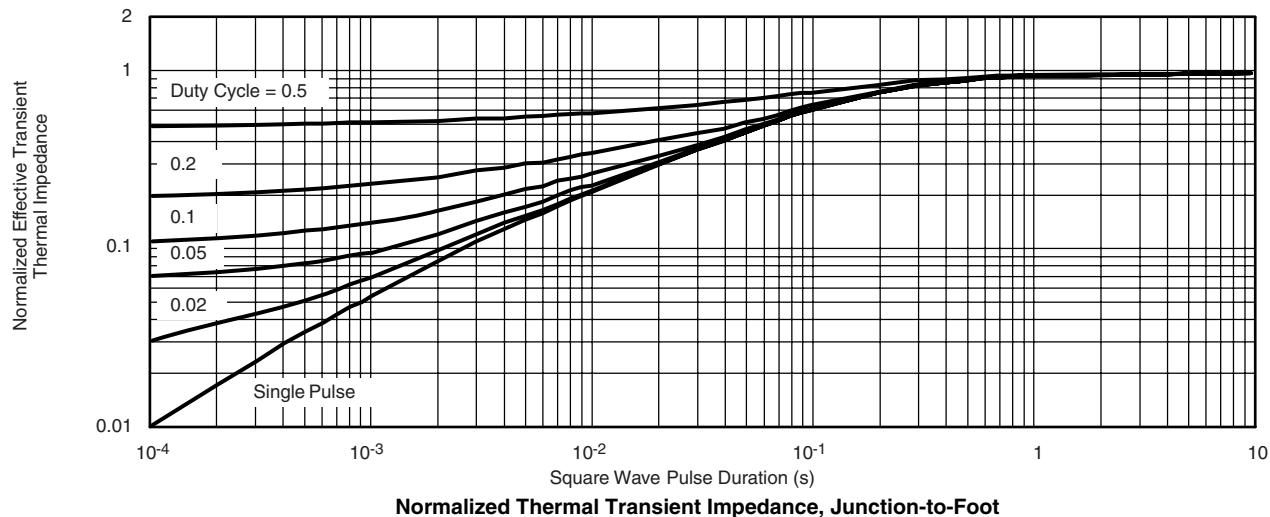
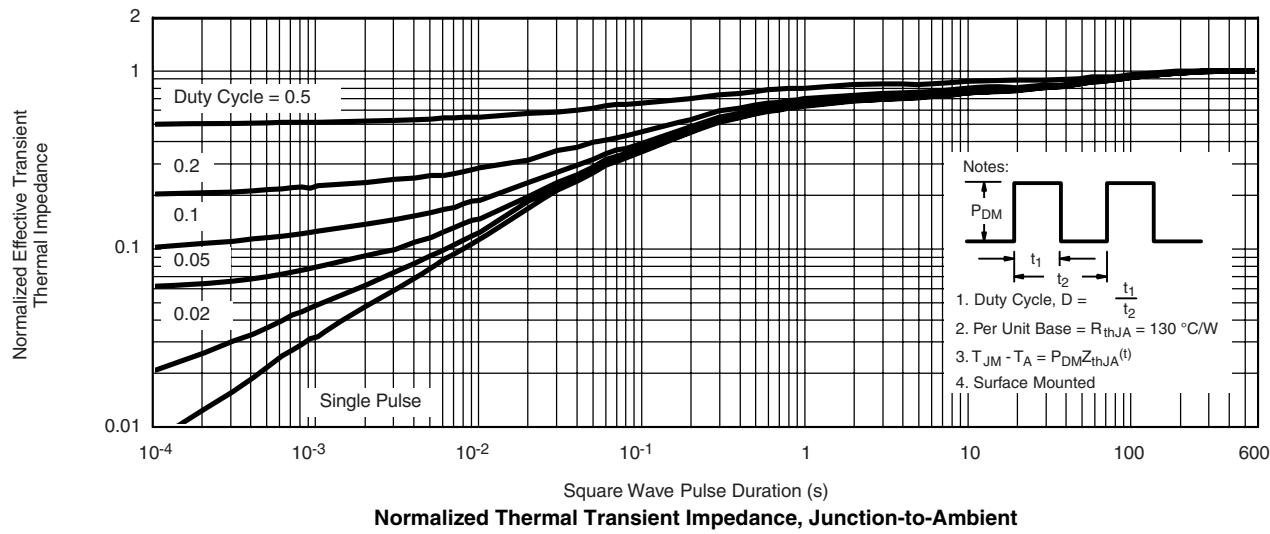
Power Derating, Junction-to-Foot



Power Derating, Junction-to-Ambient

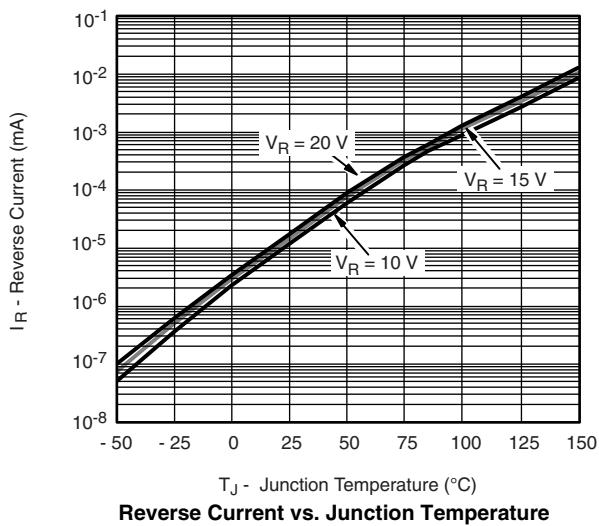
* The power dissipation P_D is based on $T_{J(\text{max})} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

MOSFET TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted

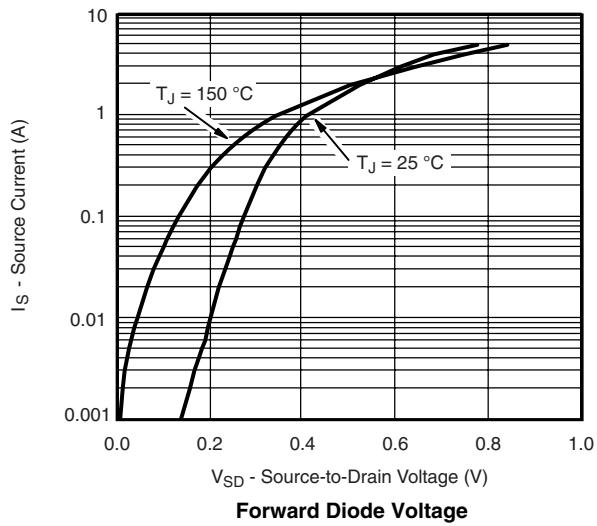


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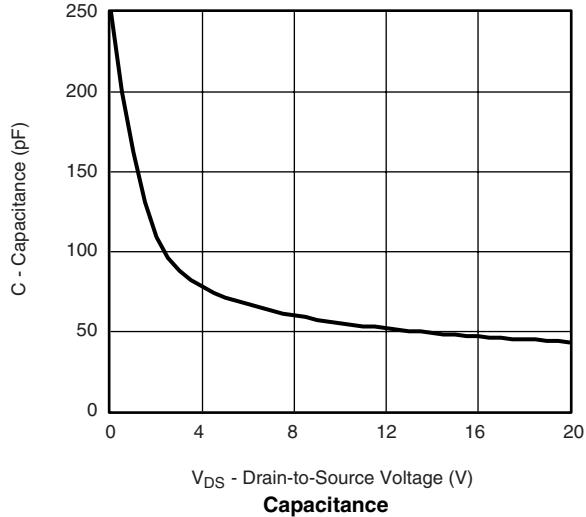
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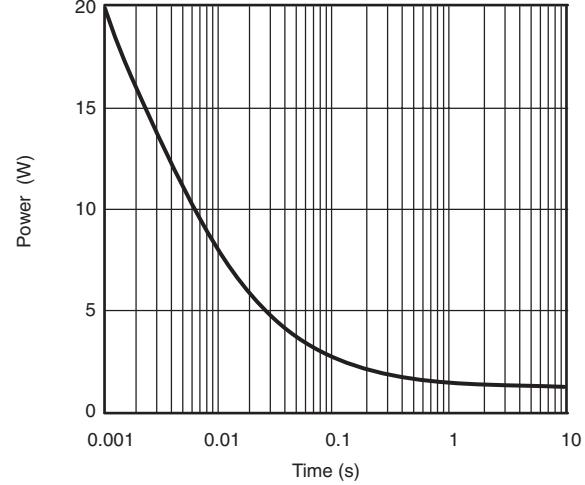
Reverse Current vs. Junction Temperature



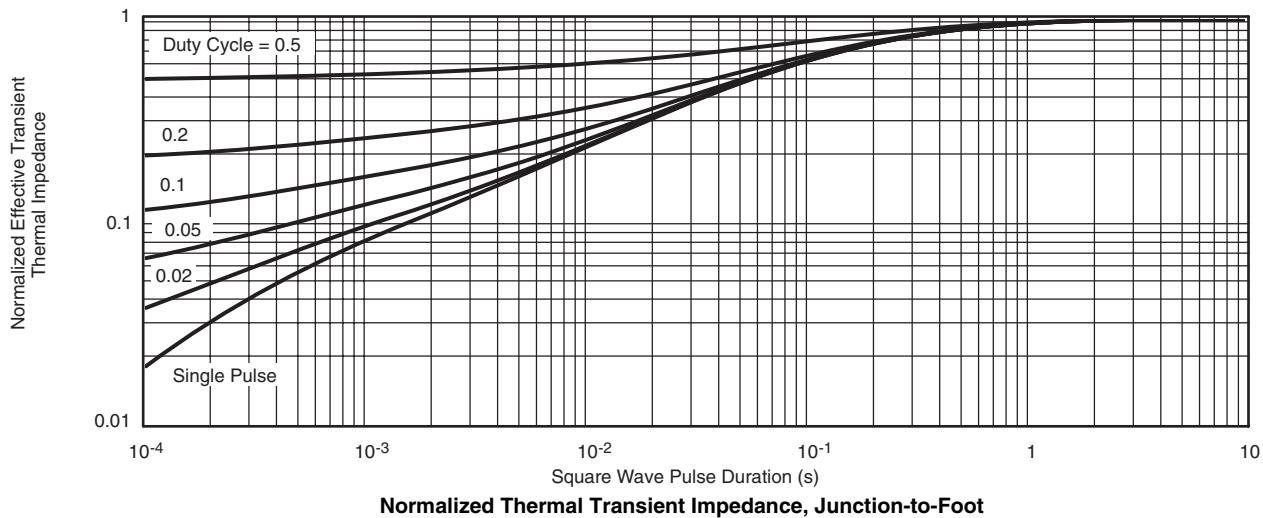
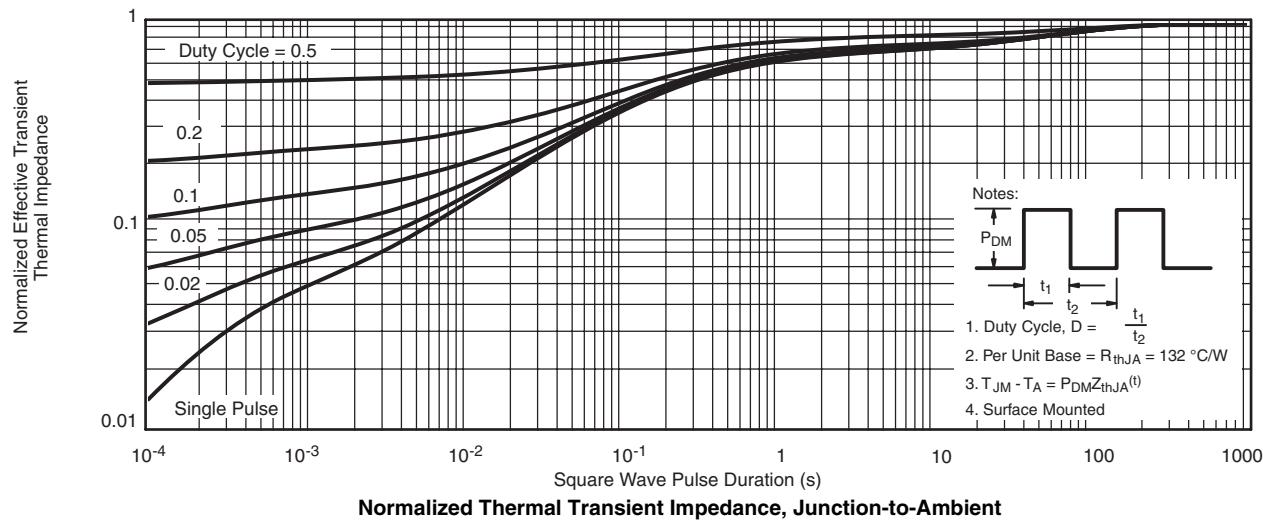
Forward Diode Voltage



Capacitance



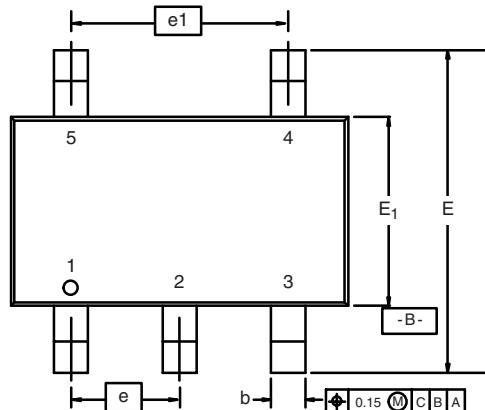
Single Pulse Power, Junction-to-Ambient

SCHOTTKY TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted


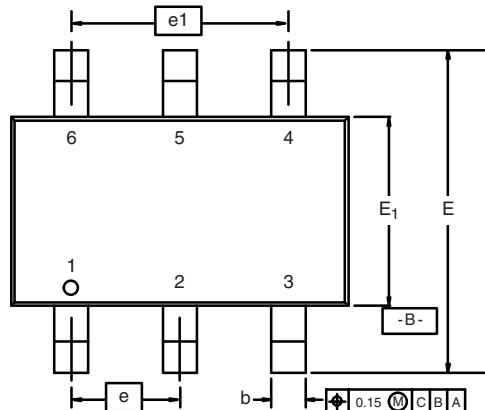
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68912.

TSOP: 5/6-LEAD

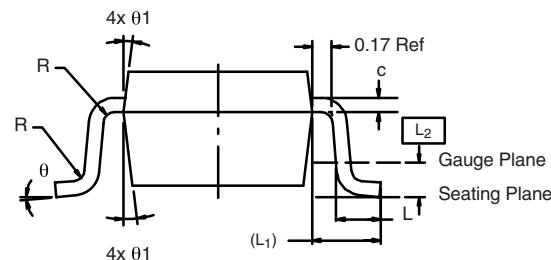
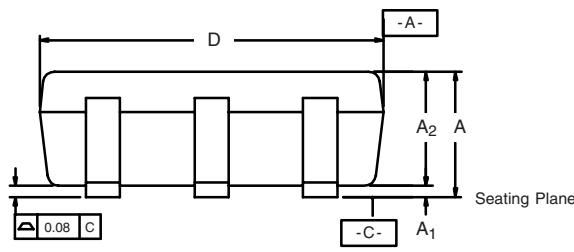
JEDEC Part Number: MO-193C



5-LEAD TSOP



6-LEAD TSOP



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A₁	0.01	-	0.10	0.0004	-	0.004
A₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L₁	0.60 Ref			0.024 Ref		
L₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ₁	7° Nom			7° Nom		

ECN: C-06593-Rev. I, 18-Dec-06

DWG: 5540

Mounting LITTLE FOOT® TSOP-6 Power MOSFETs

Surface mounted power MOSFET packaging has been based on integrated circuit and small signal packages. Those packages have been modified to provide the improvements in heat transfer required by power MOSFETs. Leadframe materials and design, molding compounds, and die attach materials have been changed. What has remained the same is the footprint of the packages.

The basis of the pad design for surface mounted power MOSFET is the basic footprint for the package. For the TSOP-6 package outline drawing see <http://www.vishay.com/doc?71200> and see <http://www.vishay.com/doc?72610> for the minimum pad footprint. In converting the footprint to the pad set for a power MOSFET, you must remember that not only do you want to make electrical connection to the package, but you must make thermal connection and provide a means to draw heat from the package, and move it away from the package.

In the case of the TSOP-6 package, the electrical connections are very simple. Pins 1, 2, 5, and 6 are the drain of the MOSFET and are connected together. For a small signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

Figure 1 shows the copper spreading recommended footprint for the TSOP-6 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlays the basic pattern on pins 1, 2, 5, and 6. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. Notice that the planar copper is shaped like a "T" to move heat away from the drain leads in all directions. This pattern uses all the available area underneath the body for this purpose.

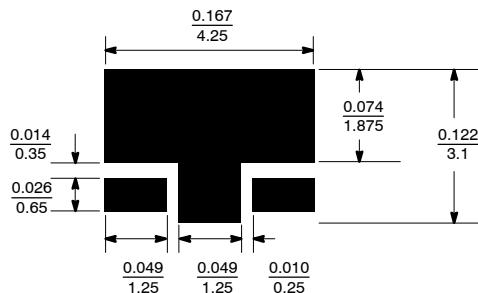


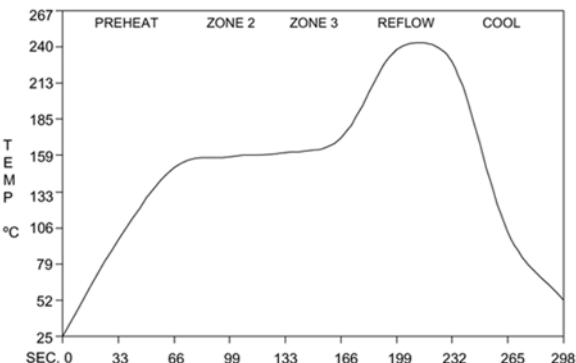
FIGURE 1. Recommended Copper Spreading Footprint

Since surface mounted packages are small, and reflow soldering is the most common form of soldering for surface mount components, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

REFLOW SOLDERING

Vishay Siliconix surface-mount packages meet solder reflow reliability requirements. Devices are subjected to solder reflow as a test preconditioning and are then reliability-tested using temperature cycle, bias humidity, HAST, or pressure pot. The solder reflow temperature profile used, and the temperatures and time duration, are shown in Figures 2 and 3.



Ramp-Up Rate	+6°C/Second Maximum
Temperature @ 155 ± 15°C	120 Seconds Maximum
Temperature Above 180°C	70 – 180 Seconds
Maximum Temperature	240 +5/-0°C
Time at Maximum Temperature	20 – 40 Seconds
Ramp-Down Rate	+6°C/Second Maximum

FIGURE 2. Solder Reflow Temperature Profile

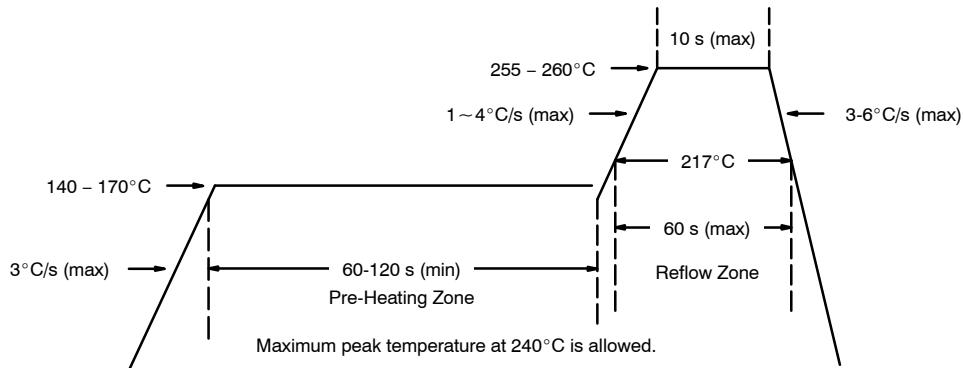


FIGURE 3. Solder Reflow Temperature and Time Durations

Thermal Performance

A basic measure of a device's thermal performance is the junction-to-case thermal resistance, $R_{\theta_{jc}}$, or the junction-to-foot thermal resistance, $R_{\theta_{jf}}$. This parameter is measured for the device mounted to an infinite heat sink and is therefore a characterization of the device only, in other words, independent of the properties of the object to which the device is mounted. Table 1 shows the thermal performance of the TSOP-6.

TABLE 1.	
Equivalent Steady State Performance—TSOP-6	
Thermal Resistance $R_{\theta_{jf}}$	30°C/W

System and Electrical Impact of TSOP-6

In any design, one must take into account the change in MOSFET $r_{DS(on)}$ with temperature (Figure 4).

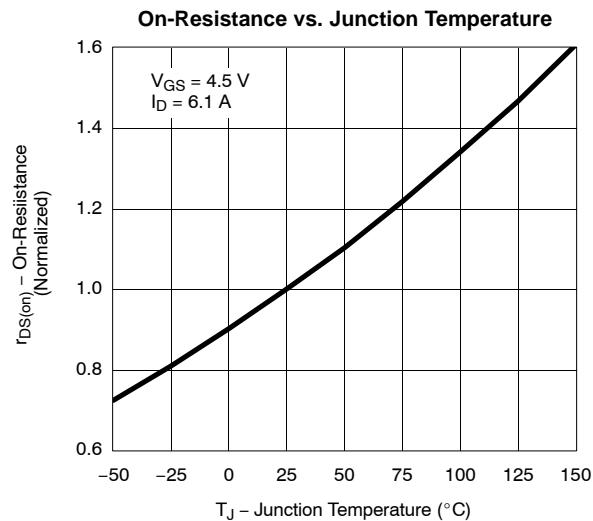
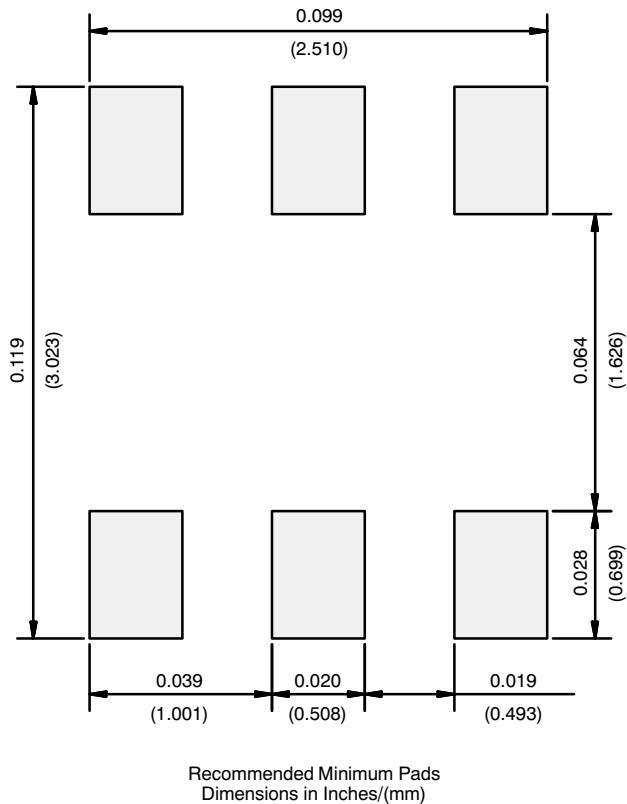


FIGURE 4. Si3434DV

RECOMMENDED MINIMUM PADS FOR TSOP-6



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