

# **W682510/ W682310**

## **DUAL-CHANNEL VOICEBAND CODECS**

Datasheet  
Revision A11

## 1. GENERAL DESCRIPTION

The W682510 and W682310 are general-purpose dual channel PCM CODECs with pin-selectable  $\mu$ -Law or A-Law companding. The device is compliant with the ITU G.712 specification. It operates from a single power supply (+5V for the W682510, +3V for the W682310) and is available in 20-pin SSOP, and 24-pin SOP package options. Functions performed include digitization and reconstruction of voice signals, and band limiting and smoothing filters required for PCM systems. The filters are compliant with ITU G.712 specification. The W682510 and W682310 performance is specified over the industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

The W682510 includes an on-chip precision voltage reference and receive output buffer amplifiers, capable of driving  $600\Omega$  loads (line transformers.) The analog section is fully differential, reducing noise and improving the power supply rejection ratio. The data transfer protocol supports either parallel or serial synchronous communications for PCM applications. The W682510 and W682310 have a build in PLL that eliminates the need for a master clock and automatically determines the division ratio for the required internal clock.

For fast evaluation and prototyping purposes, the W682510DK & W682310DK development kits are available.

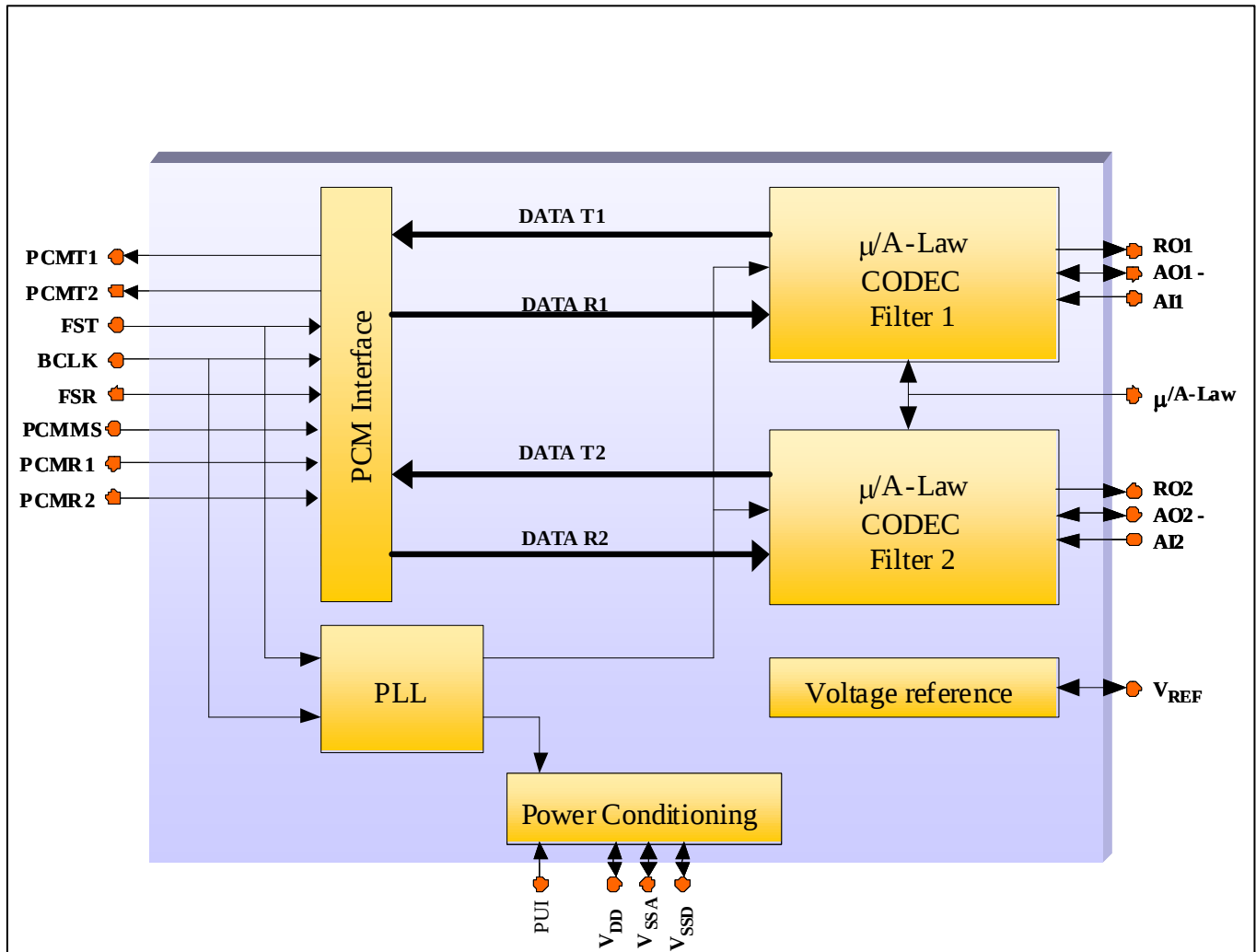
## 2. FEATURES

- Single power supply
  - o 4.5V to 5.5V (W682510)
  - o 2.7V to 3.8V (W682310)
- Typical power dissipation of 35 mW, power-down mode of 5  $\mu\text{W}$
- Fully-differential analog circuit design
- On-chip precision reference-
  - o W682510: 1.73V for a 0.8 dBm OTLP at  $600\Omega$
  - o W682310: 1.41V reference for a OTLP of  $-3.8\text{ dBm}$  into  $1200\Omega$
- Pin-selectable  $\mu$ -Law and A-Law companding (compliant with ITU G.711)
- CODEC A/D and D/A filtering compliant with ITU G.712
- Industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
- Three packages: 20-pin SSOP, 20-pin and 24-pin SOP
- Pb-Free / RoHS package options available

## APPLICATIONS

- Digital Telephone Systems
- Central Office Equipment (Gateways, Switches, Routers)
- PBX Systems (Gateways, Switches)
- PABX/SOHO Systems
- Hands free system
- Speakerphone devices
- VoIP Terminals
- Enterprise Phones
- ISDN Terminals
- Analog line cards

### 3. BLOCK DIAGRAM



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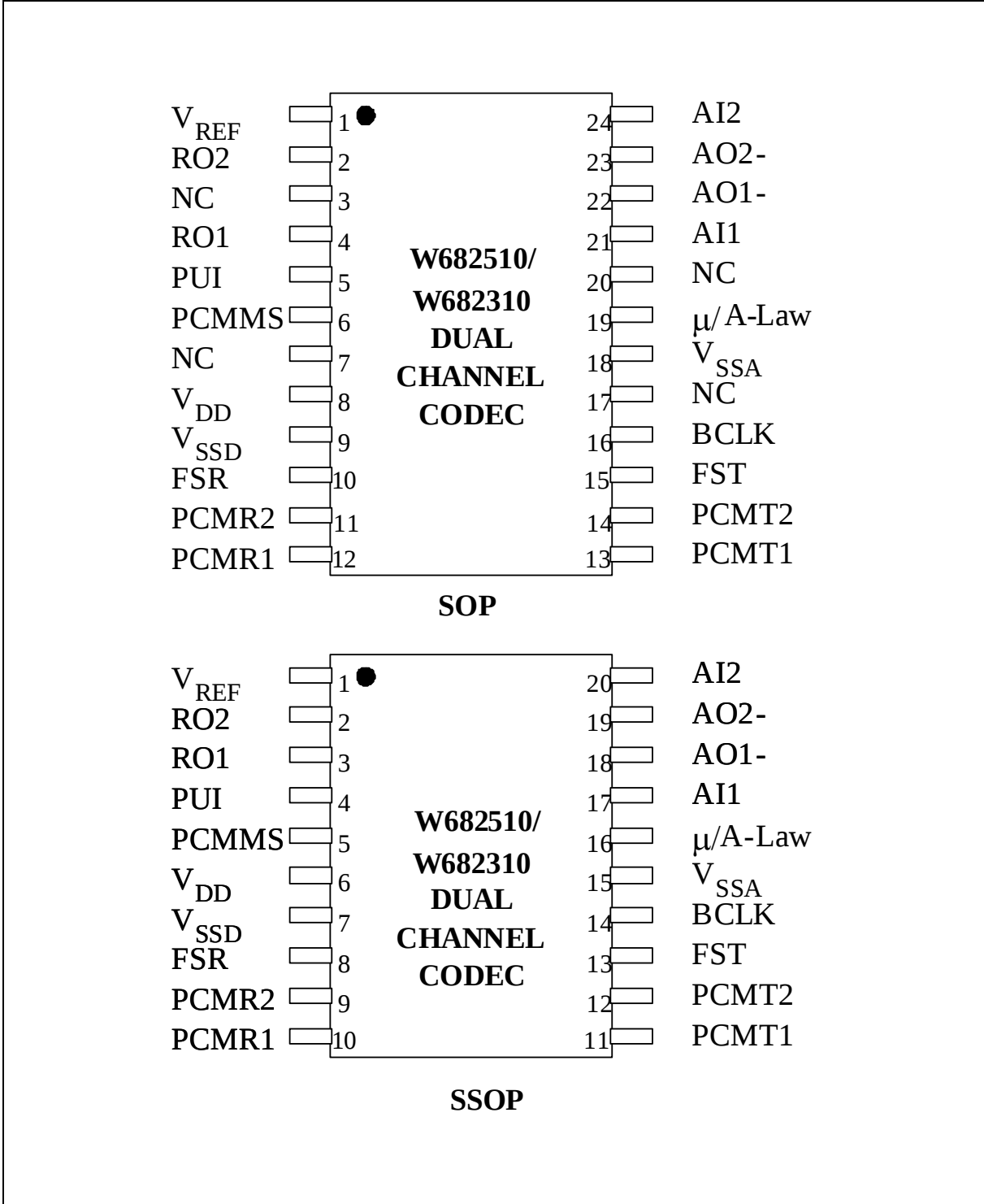
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5. PIN CONFIGURATION



## 6. PIN DESCRIPTION

| Pin Name         | Pin # SSOP | Pin # SOP | Functionality<br>(CH1 = Channel 1, CH2 = Channel 2)                                                                                                                                         |
|------------------|------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>REF</sub> | 1          | 1         | This pin is used to bypass the signal ground. It needs to be decoupled to V <sub>SS</sub> through a 0.1 $\mu$ F ceramic decoupling capacitor. No external loads should be tied to this pin. |
| RO2              | 2          | 2         | CH2 Non-Inverting output of the receive smoothing filter. This pin can typically drive a 600 $\Omega$ load (W682510) or 1200 $\Omega$ load (W682310).                                       |
| RO1              | 3          | 4         | CH1 Non-Inverting output of the receive smoothing filter. This pin can typically drive a 600 $\Omega$ load (W682510) or 1200 $\Omega$ load (W682310)..                                      |
| PUI              | 4          | 5         | Power up input signal. When this pin is HIGH (tied to V <sub>DD</sub> ) the part is powered up. When LOW (tied to V <sub>SS</sub> ) the part is powered down.                               |
| PCMMS            | 5          | 6         | PCM mode select input (serial or parallel data interface) HIGH = Parallel, LOW = Serial                                                                                                     |
| V <sub>DD</sub>  | 6          | 8         | Power supply. This pin should be decoupled to V <sub>SS</sub> with a 0.1 $\mu$ F ceramic capacitor.                                                                                         |
| V <sub>SSD</sub> | 7          | 9         | This is the digital supply ground. This pin should be connected to 0V.                                                                                                                      |
| FSR              | 8          | 10        | 8 kHz Frame Sync input for the PCM receive section. It can also be connected to the FST pin when transmit and receive are synchronous operations.                                           |
| PCMR2            | 9          | 11        | CH2 PCM input data receive pin. The data needs to be synchronous with the FSR and BCLK pins.                                                                                                |
| PCMR1            | 10         | 12        | CH1 PCM input data receive pin. The data needs to be synchronous with the FSR and BCLK pins.                                                                                                |
| PCMT1            | 11         | 13        | CH1 PCM output data transmit pin. The output data is synchronous with the FST and BCLK pins.                                                                                                |
| PCMT2            | 12         | 14        | CH2 PCM output data transmit pin. The output data is synchronous with the FST and BCLK pins.                                                                                                |
| FST              | 13         | 15        | 8 kHz transmit frame sync input. This pin synchronizes the transmit data bytes.                                                                                                             |
| BCLK             | 14         | 16        | PCM transmit and receive bit clock input pin for CH1 and CH2 transmit.                                                                                                                      |

| Pin Name         | Pin #<br>SSOP | Pin #<br>SOP | Functionality<br>(CH1 = Channel 1, CH2 = Channel 2)                                                                                                                                |
|------------------|---------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>SSA</sub> | 15            | 18           | This is the analog supply ground. This pin should be connected to 0V.                                                                                                              |
| μ/A-Law          | 16            | 19           | Compander mode select pin. μ-Law companding is selected when this pin is LOW (tied to V <sub>SS</sub> .) A-Law companding is selected when pin is HIGH (tied to V <sub>DD</sub> .) |
| AI1              | 17            | 21           | CH1 Non-Inverting input of the first gain stage in the transmit path.                                                                                                              |
| AO1-             | 18            | 22           | CH1 Inverting analog output of the first gain stage in the transmit path.                                                                                                          |
| AO2-             | 19            | 23           | CH2 Inverting analog output of the first gain stage in the transmit path                                                                                                           |
| AI2              | 20            | 24           | CH2 Non-Inverting input of the first gain stage in the transmit path.                                                                                                              |

## 7. FUNCTIONAL DESCRIPTION

W682510/W682310 is a single-rail, dual channel PCM CODEC for voiceband applications. The CODEC complies with the specifications of the ITU-T G.712 recommendation. The CODEC includes two complete  $\mu$ -Law and A-Law companders. The  $\mu$ -Law and A-Law companders are designed to comply with the specifications of the ITU-T G.711 recommendation.

The block diagram in section 3 shows the main components of the W682510/W682310. The chip consists of a PCM interface, which can process the data in parallel or serial formats. The PLL of the chip provides the internal clock signals and synchronizes the CODEC sample rate with the external frame sync frequency. The power-conditioning block provides the internal power supply for the digital and the analog section, while the voltage reference block provides a precision analog ground voltage for the analog signal processing.

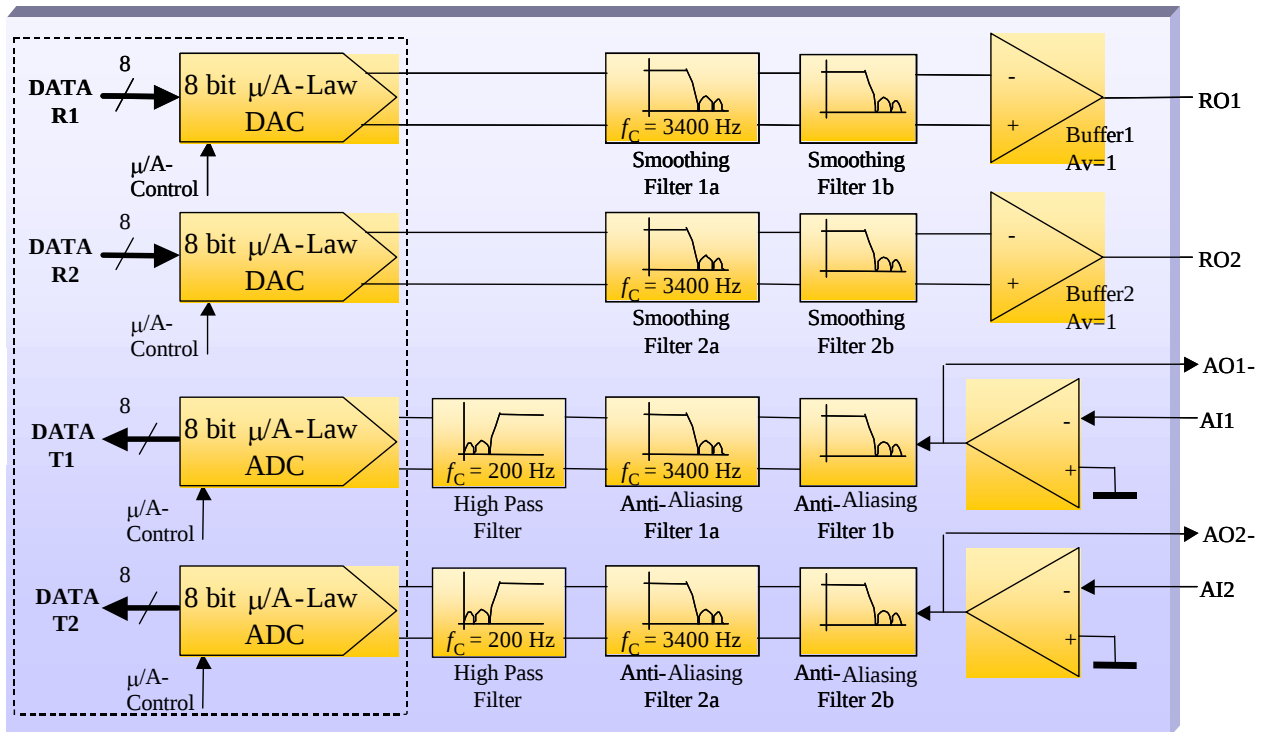


FIGURE 7.1: THE W682510 AND W682310 SIGNAL PATH

### 7.1. TRANSMIT PATH

The A-to-D path of the CODEC contains an analog input amplifier with externally configurable gain setting (see application examples in section 11). The transmit amplifier output is the input to the encoder section.

The output of the input amplifier is fed through a low-pass filter to prevent aliasing at the switched capacitor 3.4 kHz low pass filter. The 3.4 kHz switched capacitor low pass filter prevents aliasing of input signals above 4 kHz, due to the sampling at 8 kHz. The output of the 3.4 kHz low pass filter is filtered by a high pass filter with a 200 Hz cut-off frequency. The filters are designed according to the recommendations in the G.712 ITU-T specification. From the output of the high pass filter the signal is digitized. The signal is converted into a compressed 8-bit digital representation with either  $\mu$ -Law or A-Law format. The  $\mu$ -Law or A-Law format is pin-selectable through the  $\mu$ /A-Law pin. The compression format can be selected according to Table 7.1.

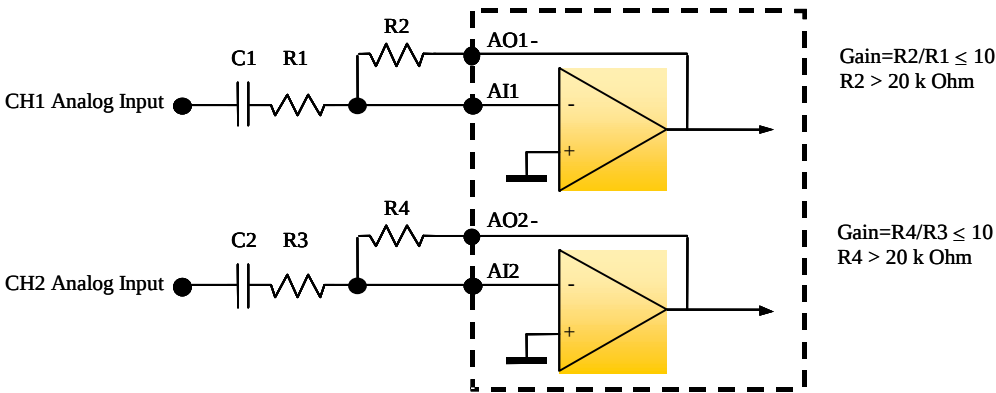
**TABLE 7.1: PIN-SELECTABLE COMPRESSION FORMAT**

| $\mu$ /A-Law Pin | Format     |
|------------------|------------|
| $V_{DD}$ (HIGH)  | A-Law      |
| $V_{SSA}$ (LOW)  | $\mu$ -Law |

The digital 8-bit  $\mu$ -Law or A-Law samples are fed to the PCM interface for serial or parallel transmission at the sample rate supplied by the external frame sync FST.

#### 7.1.1.1. AI1, AI2, AO1-, AO2-

AI1 and AI2 are the transmit analog inputs for channels 1 and 2. AO1- and AO2- are the transmit level feedback for channels 1 and 2. AI1 and AI2 are inverting inputs for the Op-Amps. AO1- and AO2- are connected to the outputs of the Op-Amps and are used to set the level, as illustrated below. When AI1 and AI2 are not used, connect AI1 to AO1- and AI2 to AO2-. During power saving mode and power down mode, the AO1- and AO2- outputs are tied weakly to  $V_{SSA}$  on the W682510 or are high impedance on the W682310 (See table on page 14).



### 7.1.2. PCMT1

The PCM signal output of channel 1 when the parallel mode is selected. The PCM output signal is sent from PCMT1 in a sequential order, synchronizing with the rising edge of the BCLK signal. The MSB may be output at the rising edge of the FST signal, based on the timing between BCLK and FST. This output pin is in a high impedance state except during 8-bit PCM output. It is also in a high impedance state during power-saving state or power-down. When serial operation is selected, this pin is configured to be the output of the serial multiplexed two channel PCM signal. A pull-up resistor must be connected to this pin, as it is an open drain output. This device is compatible with the ITU-T coding law and output coding format recommendation.

**TABLE 7.15: PCM CODES FOR ZERO AND FULL SCALE**

| Level        | $\mu$ -Law |            |           | A-Law    |            |           |
|--------------|------------|------------|-----------|----------|------------|-----------|
|              | Sign bit   | Chord bits | Step bits | Sign Bit | Chord Bits | Step Bits |
| + Full Scale | 1          | 000        | 0000      | 1        | 010        | 1010      |
| + Zero       | 1          | 111        | 1111      | 1        | 101        | 0101      |
| - Zero       | 0          | 111        | 1111      | 0        | 101        | 0101      |
| - Full Scale | 0          | 000        | 0000      | 0        | 010        | 1010      |

### 7.1.3. PCMT2

The PCM signal output for channel 2 when the parallel mode is selected. The PCM output signal is sent from PCMT2 in a sequential order, synchronized with the rising edge of the BCLK signal. The MSB may be output at the rising edge of the FST signal, based on the timing between BCLK and FST. This pin is in a high impedance state except during 8-bit PCM output. It is also in a high impedance state during power-saving state or power-down. When the serial operation is selected, this pin is left open. A pull-up resistor must be connected to this pin, as it is an open drain output. This device is compatible with the ITU-T coding law and output coding format recommendation.

## 7.2. RECEIVE PATH

The 8-bit digital input samples for the D-to-A path are serially shifted in by the PCM interface and converted to parallel data bits. During every cycle of the frame sync FSR, the parallel data bits are fed through the pin-selectable  $\mu$ -Law or A-Law expander and converted to analog samples. The mode of expansion is selected by the  $\mu$ /A-Law pin as shown in Table 7.2. The analog samples are filtered by a low-pass smoothing filter with a 3.4 kHz cut-off frequency, according to the ITU-T G.712 specification. A  $\sin(x)/x$  compensation is integrated with the low pass smoothing filter. The output of this filter is buffered to provide the receive output signal RO.

### 7.2.1. RO1, RO2

RO1 and RO2 are the receive analog outputs for channel 1 and channel 2. The output signal of the W682510 has an amplitude of 3.46 Vpp (2.03 Vpp for W682310) around the signal ground voltage ( $V_{REF}$ ). When the digital PCM signal of +3 dBm0 is presented to PCMR1 or PCMR2, it can drive a load



of 600 Ohms or more at 5 V supply voltage for the W682510 and 1200 Ohms at 3V supply for the W682310. During power saving mode, these outputs are at the voltage level of  $V_{REF}$  with a high impedance. These outputs have a feature that reduces audio “pop” noises when switching between active and inactive states and back.

### **7.2.2. PCMR1**

The PCM signal input for channel 1 when in the parallel mode. D/A conversion is performed on the serial PCM signal input to this pin. The FSR signal, synchronous with the serial PCM signal, and the BCLK signal, processes the code. Then the analog output is output from the RO1 pin. The data rate of the PCM signal is equal to the frequency of the BCLK signal.

The PCM signal is shifted in on the falling edge of the BCLK signal. It is latched into the internal 8-bit register. The start of the PCM data (MSB) is synchronized with the rising edge of FSR. In the serial mode, this pin is not used and should be connected to GND (0V).

### **7.2.3. PCMR2**

PCM signal input for channel 2 when the parallel mode is selected. D/A conversion is performed with the serial PCM signal input to this pin, the FSR signal, synchronous with the serial PCM signal, and the BCLK signal, and then the analog output is output from the RO2 pin. The data rate of the PCM signal is equal to the frequency of the BCLK signal. The PCM signal is shifted at the falling edge of the BCLK signal and latched into the internal register when shifted by eight bits. The start of the PCM data (MSB) is identified at the rising edge of FSR. In the serial mode this pin is used for the two channel multiplexed PCM signal input.

## **7.3. POWER SIGNALS**

### **7.3.1. $V_{DD}$**

The power supply for the analog and digital parts of the W682510 must be 5V +/- 10% and 2.7V to 3.8V for the W682310. This supply voltage is connected to the  $V_{DD}$  pin. The  $V_{DD}$  pin needs to be decoupled to ground through a 0.1  $\mu$ F ceramic capacitor. A power supply for an analog circuit in the system to which the device is applied should be used. A bypass capacitor of 0.1  $\mu$ F to 1  $\mu$ F with good high-frequency characteristics (Low ESR) and a capacitor of 10  $\mu$ F to 20  $\mu$ F should be connected between this pin and the  $V_{SSA}$  pin if needed.

### **7.3.2. $V_{SSA}$**

Ground for the analog signal circuits. This ground is separate from the digital signal ground. The  $V_{SSA}$  pin must be connected to the  $V_{SSD}$  pin on the printed circuit board to make a common ground. However, it's advised to connect the PCB traces of these pins at the main supply hookup of the PCB and run the  $V_{SSA}$  and  $V_{SSD}$  traces separately to the device.

### **7.3.3. $V_{SSD}$**

Ground for the digital signal circuits. This ground is separate from the analog signal ground. The  $V_{SSD}$  pin must be connected to the  $V_{SSA}$  pin on the printed circuit board to make a common ground. However, it's advised to connect the PCB traces of these pins at the main supply hookup of the PCB and run the  $V_{SSA}$  and  $V_{SSD}$  traces separately to the device

#### 7.3.4. $V_{REF}$

This pin carries the signal ground voltage level and requires a bypass capacitor. A 0.1 $\mu$ F ceramic (with low ESR for good high frequency response) capacitor needs to be connected between the  $V_{SSA}$  pin and the  $V_{REF}$  pin.

#### 7.3.5. PUI

Power up input signal. When the PUI pin is set to logic “0” level, the CODEC will go into power down mode.

### 7.4. PCM INTERFACE

The PCM interface is controlled by pins PCMMS, BCLK, FSR & FST. The input data is received through the PCMR pin and the output data is transmitted through the PCMT pin. The modes of operation of the interface are shown in Table 7.2.

**TABLE 7.2: PCM INTERFACE MODE SELECTIONS**

| PCMMS              | PCM Mode      | Data Available                                                                                                                    |
|--------------------|---------------|-----------------------------------------------------------------------------------------------------------------------------------|
| $V_{DD}$<br>[HIGH] | Parallel Mode | CH1 data on PCMT1 & PCMR1<br>CH2 data on PCMT2 and PCMR2 (same timing as CH1)                                                     |
| $V_{SS}$<br>[LOW]  | Serial Mode   | CH1 data followed by CH2 receive data on PCMR2 (total 16 bits)<br>CH1 data followed by CH2 transmit data on PCMT1 (total 16 bits) |

#### 7.4.1. $\mu$ /A-Law

This pin selects the desired companding law. The CODEC will operate in the  $\mu$ -law when this pin is at a logic “0” level and in the A-law when at a logic “1” level. The CODEC operates  $\mu$ -law if the pin is left open, since this pin is internally pulled down.

**TABLE 7.25: PIN-SELECTABLE COMPRESSION FORMAT**

| $\mu$ /A-Law pin           | Format     |
|----------------------------|------------|
| HIGH ( $V_{DD}$ )          | A-Law      |
| LOW ( $V_{SS}$ ), Floating | $\mu$ -Law |

#### 7.4.2. BCLK

This is the shift clock signal input for the PCMR1, PCMR2, PCMT1, and PCMT2 signals. The frequency, equal to the data rate, is 64, 96, 128, 192, 256, 384, 512, 768, 1024, 1536, 1544, 2048 or 200 kHz. Setting this signal to a steady logic “1” or “0” sets both transmit and receive circuits to the power saving state.

#### **7.4.3. FSR**

This is the receive synchronizing signal input. The required eight-bits of PCM data are selected from the PCM data signal to the PCMR1 and PCMR2 pins by the receive synchronizing signal. All timing signals in the receive section are synchronized by this synchronizing signal. This signal must be in phase with the BCLK. The frequency should be  $8\text{ kHz} \pm 50\text{ ppm}$  to guarantee the AC characteristics. This device can operate in the range of 6 kHz to 9 kHz, but the electrical characteristics specified in the data sheet are not guaranteed.

#### **7.4.4. FST**

The transmit synchronizing signal input. The PCM output signal from PCMT1 and PCMT2 is sent in synchronization with this transmit synchronizing signal. This FST signal triggers the PLL and synchronizes all timing signals of the transmit section. The synchronizing signal must be in phase with BCLK. The frequency should be  $8\text{ kHz} \pm 50\text{ ppm}$  to guarantee the AC characteristics. This device can operate in the range of 6 kHz to 9 kHz sample rates, but the electrical characteristics are not guaranteed. Setting this signal to logic HIGH or LOW drives both transmit and receive circuits to power saving state.

#### **7.4.5. PCMMS**

The control signal for mode selection of the PCM input and output. When this signal is HIGH, the PCM input and output are in the parallel mode. The PCM data of CH1 and CH2 is input to PCMR1 and PCMR2, and output from PCMT1 and PCMT2, with the same timing. When this signal is at a LOW level, the PCM input and output are in the serial mode. The PCM data of CH1 and CH2 is input to PCMR2 and output from PCMT1 as two serial 8-bit bytes.

### **7.5. POWER STATE MODES**

#### **7.5.1. Power Save Mode**

In the power save mode, all internal analog circuits except the internal reference are powered down. The CODEC automatically enters the power save mode when the FST or BCLK signal is set to digital "1" or digital "0";

Upon power up with FST and BCLK signals present, it will take 2 to 10 milliseconds for the internal PLL to lock. In addition to the PLL lock-in time, the analog outputs will be set to the internal signal ground for 1 millisecond. This will avoid power up glitches at the outputs. The digital open drain outputs will remain at high impedance during this power up delay.

#### **7.5.2. Power Down Mode**

When the power up indicator pin, PUI, is set LOW all internal circuits will go into the power down state. It will take 2 to 10 milliseconds for the PLL to lock when operation is resumed with the FST and BCLK signals applied and PUI set HIGH. An additional 1-millisecond delay is used to set the analog outputs to the signal ground reference in order to avoid power up glitches. The digital open drain outputs will remain at high impedance during this power up delay.

### 7.5.3. Power Save/Down Output pin state

The following table shows the states of the output pins in the power save or power down mode.

**TABLE 7.5: OUTPUT PIN STATES**

| Product Name | Output Pin       |               |
|--------------|------------------|---------------|
|              | AO1-, A02-       | RO1, RO2      |
| W682510      | V <sub>SSA</sub> | Signal Ground |
| W682310      | High Z           | Signal Ground |

8. TIMING DIAGRAMS

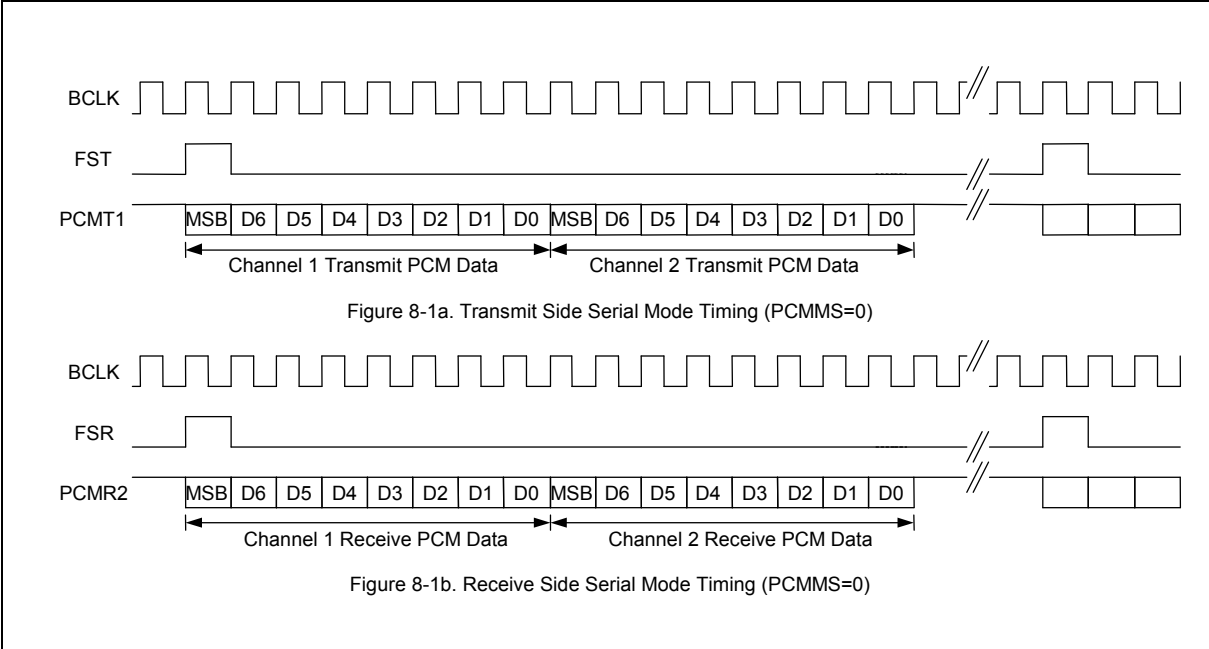


FIGURE 8.1: SERIAL MODE PCM TIMING

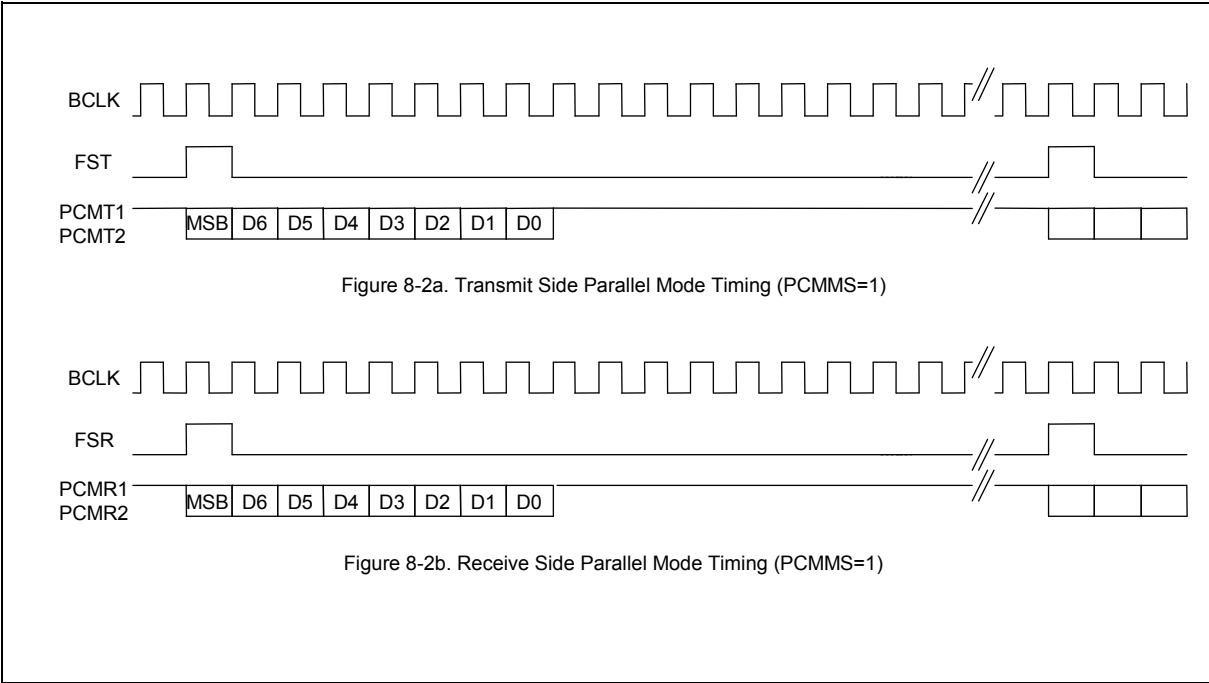


FIGURE 8.2: PARALLEL MODE PCM TIMING

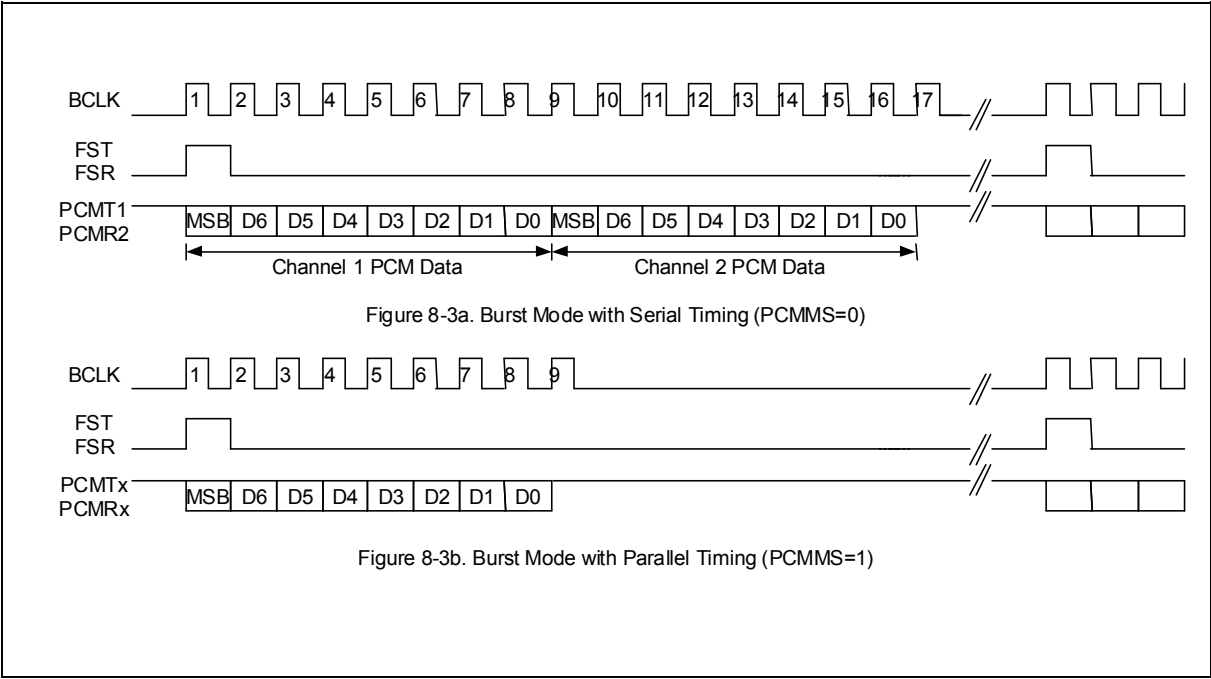


FIGURE 8.3: BURST MODE PCM TIMING

TABLE 8.1: PCM SYNCHRONIZATION PARAMETERS

| SYMBOL     | DESCRIPTION                                              | MIN                                                               | TYP | MAX | UNIT       |
|------------|----------------------------------------------------------|-------------------------------------------------------------------|-----|-----|------------|
| $f_{FS}$   | FST, FSR frequency                                       | ---                                                               | 8   | --- | KHz        |
| $t_{WS}$   | FST, FSR Pulse Width                                     | 1                                                                 | --- | 7   | $T_{BCLK}$ |
| $t_j$      | FST, FSR allowable jitter                                | 0                                                                 | --- | 500 | nsec       |
| $f_{BCLK}$ | BCLK frequency                                           | 64, 128, 256, 512, 1024, 2048, 96, 192, 384, 768, 1536, 1544, 200 |     |     | kHz        |
| $D_C$      | BCLK Duty Cycle                                          | 40                                                                | 50  | 60  | %          |
| $t_{lr}$   | FSR, FST, BCLK, PCMR1, PCMR2, PUI, PCMMS input rise time | ---                                                               | --- | 50  | nsec       |
| $t_{lf}$   | FSR, FST, BCLK, PCMR1, PCMR2, PUI, PCMMS input fall time | ---                                                               | --- | 50  | nsec       |

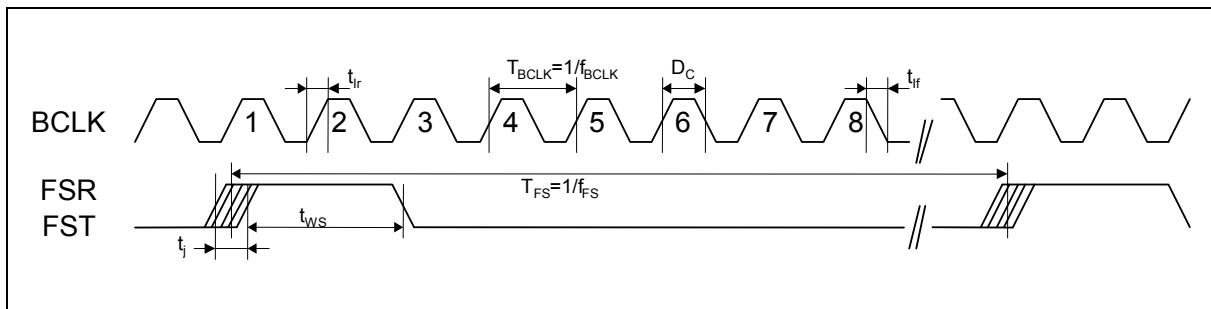


FIGURE 8.4: PCM SYNCHRONIZATION PARAMETERS

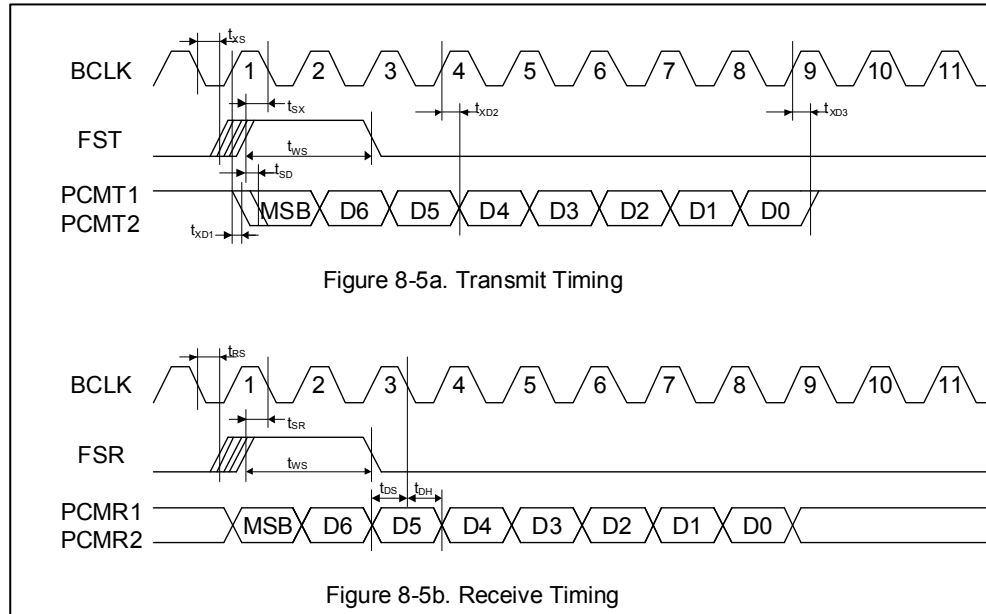


FIGURE 8.5 PCM TIMING PARAMETERS

| SYMBOL    | DESCRIPTION                               | MIN        | TYP | MAX       | UNIT |
|-----------|-------------------------------------------|------------|-----|-----------|------|
| $t_{WS}$  | FST, FSR Pulse Width                      | $T_{BCLK}$ | --- | 100 $\mu$ | sec  |
| $t_{XS}$  | BCLK low to FST high setup time           | 100        | --- | ---       | nsec |
| $t_{SX}$  | FST high to BCLK low hold time            | 100        | --- | ---       | nsec |
| $t_{SD}$  | PCMT1, PCMT2 output delay; $C_I = 100$ pF | 20         | --- | 200       | nsec |
| $t_{XD1}$ | PCMT1, PCMT2 output delay; $C_I = 100$ pF | 20         | --- | 200       | nsec |
| $t_{XD2}$ | PCMT1, PCMT2 output delay; $C_I = 100$ pF | 20         | --- | 200       | nsec |
| $t_{XD3}$ | PCMT1, PCMT2 output delay; $C_I = 100$ pF | 20         | --- | 200       | nsec |
| $t_{RS}$  | BCLK low to FSR high setup time           | 100        | --- | ---       | nsec |
| $t_{SR}$  | FSR high to BCLK low hold time            | 100        | --- | ---       | nsec |
| $t_{DS}$  | PCMR1, PCMR2 Data in setup time           | 100        | --- | ---       | nsec |
| $t_{DH}$  | PCMR1, PCMR2 Data in hold time            | 100        | --- | ---       | nsec |
| $R_{TL}$  | PCMT1, PCMT2 Pull-up resistor             | 500        | --- | ---       | Ohm  |
| $C_{TL}$  | PCMT1, PCMT2 Load capacitance             | ---        | --- | 100       | pF   |

TABLE 8.2: PCM TIMING PARAMETERS

## 9. ABSOLUTE MAXIMUM RATINGS

TABLE 9.1: ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)

| Condition                                                      | Value                                                |
|----------------------------------------------------------------|------------------------------------------------------|
| Junction temperature                                           | 150 <sup>0</sup> C                                   |
| Storage temperature range                                      | -65 <sup>0</sup> C to +150 <sup>0</sup> C            |
| Voltage Applied to any pin                                     | (V <sub>SS</sub> - 0.3V) to (V <sub>DD</sub> + 0.3V) |
| Voltage applied to any pin (Input current limited to +/-20 mA) | (V <sub>SS</sub> - 1.0V) to (V <sub>DD</sub> + 1.0V) |
| Lead temperature (soldering – 10 seconds)                      | 300 <sup>0</sup> C                                   |
| V <sub>DD</sub> - V <sub>SS</sub>                              | -0.5V to +6V                                         |

**Note:** Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device. Functional operation is not implied at these conditions.

TABLE 9.2: OPERATING CONDITIONS (PACKAGED PARTS)

| Condition                                    | Value                                    |
|----------------------------------------------|------------------------------------------|
| Industrial operating temperature             | -40 <sup>0</sup> C to +85 <sup>0</sup> C |
| Supply voltage (V <sub>DD</sub> ) W682510 5V | +4.5V to +5.5V                           |
| Supply voltage (V <sub>DD</sub> ) W682310 3V | +2.7V to +3.8V                           |
| Ground voltage (V <sub>SS</sub> )            | 0V                                       |

## 10. ELECTRICAL CHARACTERISTICS

### 10.1. GENERAL PARAMETERS W682510 4.5V – 5.5V

| Symbol           | Parameters                                      | Conditions                                               | Min <sup>(2)</sup> | Typ <sup>(1)</sup> | Max <sup>(2)</sup> | Units |
|------------------|-------------------------------------------------|----------------------------------------------------------|--------------------|--------------------|--------------------|-------|
| V <sub>IL</sub>  | Input Low Voltage                               |                                                          | 0.0                |                    | 0.8                | V     |
| V <sub>IH</sub>  | Input High Voltage                              |                                                          | 2.2                |                    | V <sub>DD</sub>    | V     |
| V <sub>OL</sub>  | PCMT1, PCMT2 Output Low Voltage                 | R <sub>pullup</sub> > 500 Ω                              | 0.0                | 0.2                | 0.4                | V     |
| I <sub>DD</sub>  | V <sub>DD</sub> Current (Operating) - ADC + DAC | No Load, No Signal                                       |                    | 7                  | 14                 | mA    |
| I <sub>SB</sub>  | V <sub>DD</sub> Current (Standby)               | FST or BCLK = OFF; PUI = V <sub>DD</sub>                 |                    | 800                | 1300               | μA    |
| I <sub>PD</sub>  | V <sub>DD</sub> Current (Power Down)            | PUI = V <sub>SS</sub>                                    |                    | 1                  | 10                 | μA    |
| I <sub>IL</sub>  | Input Low Leakage Current                       | V <sub>SS</sub> < V <sub>IN</sub> < V <sub>DD</sub>      |                    |                    | 0.5                | μA    |
| I <sub>IH</sub>  | Input High Leakage Current                      | V <sub>SS</sub> < V <sub>IN</sub> < V <sub>DD</sub>      |                    |                    | 2                  | μA    |
| I <sub>OL</sub>  | PCMT1, PCMT2 Output Leakage Current             | V <sub>SS</sub> < PCMT < V <sub>DD</sub><br>High Z State |                    |                    | +/-10              | μA    |
| C <sub>IN</sub>  | Digital Input Capacitance                       |                                                          |                    | 5                  | 10                 | pF    |
| C <sub>OUT</sub> | PCMT1, PCMT2 Output Capacitance                 | PCMT1, PCMT2 = High Z                                    |                    |                    | 15                 | pF    |

1. Typical values: T<sub>A</sub> = 25°C, V<sub>DD</sub> = 5.0 V

2. All min/max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested.

### 10.2. GENERAL PARAMETERS W682310 2.7V – 3.8V

| Symbol          | Parameters                                      | Conditions                               | Min <sup>(2)</sup>   | Typ <sup>(1)</sup> | Max <sup>(2)</sup>   | Units |
|-----------------|-------------------------------------------------|------------------------------------------|----------------------|--------------------|----------------------|-------|
| V <sub>IL</sub> | Input Low Voltage                               |                                          | 0.0                  |                    | 0.16xV <sub>DD</sub> | V     |
| V <sub>IH</sub> | Input High Voltage                              |                                          | 0.45xV <sub>DD</sub> |                    | V <sub>DD</sub>      | V     |
| V <sub>OL</sub> | PCMT1, PCMT2 Output Low Voltage                 | R <sub>pullup</sub> > 500 Ω              | 0.0                  | 0.2                | 0.4                  | V     |
| I <sub>DD</sub> | V <sub>DD</sub> Current (Operating) - ADC + DAC | No Load, No Signal                       |                      | 7.4                | 14                   | mA    |
| I <sub>SB</sub> | V <sub>DD</sub> Current (Standby)               | FST or BCLK = OFF; PUI = V <sub>DD</sub> |                      | 700                | 2000                 | μA    |

| Symbol    | Parameters                          | Conditions                               | Min <sup>(2)</sup> | Typ <sup>(1)</sup> | Max <sup>(2)</sup> | Units   |
|-----------|-------------------------------------|------------------------------------------|--------------------|--------------------|--------------------|---------|
| $I_{PD}$  | $V_{DD}$ Current (Power Down)       | $PUI = V_{SS}$                           |                    | 1                  | 10                 | $\mu A$ |
| $I_{IL}$  | Input Low Leakage Current           | $V_{SS} < V_{IN} < V_{DD}$               |                    |                    | 0.5                | $\mu A$ |
| $I_{IH}$  | Input High Leakage Current          | $V_{SS} < V_{IN} < V_{DD}$               |                    |                    | 2                  | $\mu A$ |
| $I_{OL}$  | PCMT1, PCMT2 Output Leakage Current | $V_{SS} < PCMT < V_{DD}$<br>High Z State |                    |                    | +/-10              | $\mu A$ |
| $C_{IN}$  | Digital Input Capacitance           |                                          |                    | 5                  | 10                 | pF      |
| $C_{OUT}$ | PCMT1, PCMT2 Output Capacitance     | PCMT1, PCMT2 = High Z                    |                    |                    | 15                 | pF      |

1. Typical values:  $T_A = 25^\circ C$ ,  $V_{DD} = 3.0 V$
2. All min/max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested.

### 10.3. ANALOG SIGNAL LEVEL AND GAIN PARAMETERS

W682510:  $V_{DD}=5V \pm 10\%$ ;  $V_{SS}=0V$ ;  $T_A=-40^{\circ}C$  to  $+85^{\circ}C$ ; all analog signals referred to  $V_{REF}$ ;

W682310:  $V_{DD}=2.7V$  to  $3.8V$ ;  $V_{SS}=0V$ ;  $T_A=-40^{\circ}C$  to  $+85^{\circ}C$ ; all analog signals referred to  $V_{REF}$ ;

| PARAMETER                                                             | SYM.       | CONDITION                                                                          | TYP.           | TRANSMIT (A/D) |               | RECEIVE (D/A) |               | UNIT                 |
|-----------------------------------------------------------------------|------------|------------------------------------------------------------------------------------|----------------|----------------|---------------|---------------|---------------|----------------------|
|                                                                       |            |                                                                                    |                | MIN.           | MAX.          | MIN.          | MAX.          |                      |
| Reference Level Out<br>W682510 5V                                     | $L_{ABS}$  | 0 dBm0 = +0.8 dBm @<br>600 $\Omega$ load 1020 Hz                                   | 0.850          | ---            | ---           | ---           | ---           | $V_{RMS}$            |
| Reference Level In<br>W682510 5V                                      | $T_{OTLP}$ | 1020 Hz                                                                            | 0.850          | ---            | ---           | ---           | ---           | $V_{RMS}$            |
| Reference Level Out<br>W682310 3V                                     | $L_{ABS}$  | 0 dBm0 = -3.8 dBm @<br>1200 $\Omega$ load 1020<br>Hz                               | 0.500          | ---            | ---           | ---           | ---           | $V_{RMS}$            |
| Reference Level Out<br>W682310 3V                                     | $T_{OTLP}$ | 1020 Hz                                                                            | 0.350          | ---            | ---           | ---           | ---           | $V_{RMS}$            |
| Max. Transmit Level In<br>W682510 5V                                  | $T_{XMAX}$ | 3.17 dBm0 for $\mu$ -Law<br>3.14 dBm0 for A-Law                                    | 1.732<br>1.726 | ---            | ---           | ---           | ---           | $V_{PK}$<br>$V_{PK}$ |
| Max. Transmit Level In<br>W682310 3V                                  | $T_{XMAX}$ | 3.17 dBm0 for $\mu$ -Law<br>3.14 dBm0 for A-Law                                    | 0.712<br>0.708 | ---            | ---           | ---           | ---           | $V_{PK}$<br>$V_{PK}$ |
| Absolute Gain (0 dBm0<br>@ 1020 Hz; $T_A=+25^{\circ}C$ )              | $G_{ABS}$  | 0 dBm0 @ 1020 Hz;<br>$T_A=+25^{\circ}C$                                            | 0              | -0.2           | +0.2          | -0.2          | +0.2          | dB                   |
| Absolute Gain variation<br>with Temperature                           | $G_{ABST}$ | $T_A=0^{\circ}C$ to $T_A=+70^{\circ}C$<br>$T_A=-40^{\circ}C$ to $T_A=+85^{\circ}C$ | 0              | -0.08<br>-0.1  | +0.08<br>+0.1 | -0.08<br>-0.1 | +0.08<br>+0.1 | dB                   |
| Frequency Response,<br>Relative to 0dBm0 @<br>1020 Hz                 | $G_{RTV}$  | 15 Hz                                                                              | ---            | ---            | -40           | -0.5          | 0             | dB                   |
|                                                                       |            | 50 Hz                                                                              | ---            | ---            | -30           | -0.5          | 0             |                      |
|                                                                       |            | 60 Hz                                                                              | ---            | ---            | -20           | -0.5          | 0             |                      |
|                                                                       |            | 200 Hz                                                                             | ---            | -1.5           | -0.4          | -0.5          | 0             |                      |
|                                                                       |            | 300 to 3000 Hz                                                                     | ---            | -0.20          | +0.20         | -0.20         | +0.20         |                      |
|                                                                       |            | 3300 Hz                                                                            | ---            | -0.50          | +0.20         | -0.50         | +0.20         |                      |
|                                                                       |            | 3400 Hz                                                                            | ---            | -0.8           | 0             | -0.8          | 0             |                      |
|                                                                       |            | 3600 Hz                                                                            | ---            | ---            | 0             | ---           | 0             |                      |
|                                                                       |            | 4000 Hz                                                                            | ---            | ---            | -14           | ---           | -14           |                      |
|                                                                       |            | 4600 Hz to 100 kHz                                                                 | ---            | ---            | -32           | ---           | -30           |                      |
| Gain Variation vs. Level<br>Tone<br>(1020 Hz relative to -10<br>dBm0) | $G_{LT}$   | +3 to -40 dBm0                                                                     | ---            | -0.3           | +0.3          | -0.3          | +0.3          | DB                   |
|                                                                       |            | -40 to -50 dBm0                                                                    | ---            | -0.5           | +0.5          | -0.5          | +0.5          |                      |
|                                                                       |            | -50 to -55 dBm0                                                                    | ---            | -1.2           | +1.2          | -1.2          | +1.2          |                      |

#### 10.4. ANALOG DISTORTION AND NOISE PARAMETERS

W682510:  $V_{DD}=5V \pm 10\%$ ;  $V_{SS}=0V$ ;  $T_A=-40^{\circ}C$  to  $+85^{\circ}C$ ; all analog signals referred to  $V_{REF}$ ;

W682310:  $V_{DD}=2.7V$  to  $3.8V$ ;  $V_{SS}=0V$ ;  $T_A=-40^{\circ}C$  to  $+85^{\circ}C$ ; all analog signals referred to  $V_{REF}$ ;

| PARAMETER                                                                 | SYM.         | CONDITION             | TRANSMIT (A/D) |      |      | RECEIVE (D/A) |      |      | UNIT      |
|---------------------------------------------------------------------------|--------------|-----------------------|----------------|------|------|---------------|------|------|-----------|
|                                                                           |              |                       | MIN.           | TYP. | MAX. | MIN.          | TYP. | MAX. |           |
| Total Distortion vs. Level Tone (1020 Hz, $\mu$ -Law, C-Message Weighted) | $D_{LT\mu}$  | +3 dBm0               | 36             | ---  | ---  | 34            | ---  | ---  | dBC       |
|                                                                           |              | 0 dBm0 to -30 dBm0    | 36             | ---  | ---  | 36            | ---  | ---  |           |
|                                                                           |              | -40 dBm0              | 29             | ---  | ---  | 30            | ---  | ---  |           |
|                                                                           |              | -45 dBm0              | 25             | ---  | ---  | 25            | ---  | ---  |           |
| Total Distortion vs. Level Tone (1020 Hz, A-Law, Psophometric Weighted)   | $D_{LTA}$    | +3 dBm0               | 36             | ---  | ---  | 34            | ---  | ---  | dBp       |
|                                                                           |              | 0 dBm0 to -30 dBm0    | 36             | ---  | ---  | 36            | ---  | ---  |           |
|                                                                           |              | -40 dBm0              | 29             | ---  | ---  | 30            | ---  | ---  |           |
|                                                                           |              | -45 dBm0              | 25             | ---  | ---  | 25            | ---  | ---  |           |
| Spurious Out-Of-Band at RO- (300 Hz to 3400 Hz @ 0dBm0)                   | $D_{SPO}$    | 4600 Hz to 7600 Hz    | ---            | ---  | ---  | ---           | ---  | -30  | dB        |
|                                                                           |              | 7600 Hz to 8400 Hz    | ---            | ---  | ---  | ---           | ---  | -40  |           |
|                                                                           |              | 8400 Hz to 100000 Hz  | ---            | ---  | ---  | ---           | ---  | -30  |           |
| Spurious In-Band (700 Hz to 1100 Hz @ 0dBm0)                              | $D_{SPI}$    | 300 to 3000 Hz        | ---            | ---  | -47  | ---           | ---  | -47  | dB        |
| Intermodulation Distortion (300 Hz to 3400 Hz -4 to -21 dBm0)             | $D_{IM}$     | Two tones             | ---            | ---  | -41  | ---           | ---  | -41  | dB        |
| Crosstalk (1020 Hz @ 0dBm0)                                               | $D_{XT}$     |                       | ---            | ---  | -75  | ---           | ---  | -75  | dBm0      |
| Channel to Channel Crosstalk (1020 Hz @ 0dBm0)                            | $D_{XTCH}$   |                       | ---            | ---  | -75  | ---           | ---  | -75  | dBm0      |
| Absolute Group Delay                                                      | $\tau_{ABS}$ | 1600 Hz               | ---            | ---  | 360  | ---           | ---  | 240  | $\mu$ sec |
| Group Delay Distortion (relative to group delay @ 1200 Hz)                | $\tau_D$     | 500 Hz                | ---            | ---  | 750  | ---           | ---  | 750  | $\mu$ sec |
|                                                                           |              | 600 Hz                | ---            | ---  | 380  | ---           | ---  | 370  |           |
|                                                                           |              | 1000 Hz               | ---            | ---  | 130  | ---           | ---  | 120  |           |
|                                                                           |              | 2600 Hz               | ---            | ---  | 130  | ---           | ---  | 120  |           |
|                                                                           |              | 2800 Hz               | ---            | ---  | 750  | ---           | ---  | 750  |           |
| Idle Channel Noise                                                        | $N_{IDL}$    | $\mu$ -Law; C-message | ---            | ---  | 21   | ---           | ---  | 13   | dBnc      |
|                                                                           |              | A-Law; Psophometric   | ---            | ---  | -69  | ---           | ---  | -79  | dBm0p     |

### 10.5. ANALOG INPUT AND OUTPUT AMPLIFIER PARAMETERS

W682510:  $V_{DD}=5V \pm 10\%$ ;  $V_{SS}=0V$ ;  $T_A=-40^{\circ}C$  to  $+85^{\circ}C$ ; all analog signals referred to  $V_{REF}$ ;

W682310:  $V_{DD}=2.7V$  to  $3.8V$ ;  $V_{SS}=0V$ ;  $T_A=-40^{\circ}C$  to  $+85^{\circ}C$ ; all analog signals referred to  $V_{REF}$ ;

| PARAMETER                                                           | SYM.         | CONDITION                                                     | MIN.             | TYP.       | MAX.             | UNIT.           |
|---------------------------------------------------------------------|--------------|---------------------------------------------------------------|------------------|------------|------------------|-----------------|
| AI1, AI2 Input Offset Voltage                                       | $V_{OFF,AI}$ | Unity Gain                                                    | ---              | ---        | $\pm 20$         | mV              |
| AI1, AI2 Input Resistance                                           | $R_{IN,AI}$  | AI1, AI2 to $V_{REF}$                                         | 10               | ---        | ---              | M $\Omega$      |
| AO1-, AO2- Output Amplitude                                         | $V_{AD}$     | W682510<br>W682310                                            | 0                | ---        | 3.4<br>1.4       | V <sub>pp</sub> |
| AO1-, AO2- Load Resistance                                          | $R_{LOAD}$   |                                                               | 20               | ---        | ---              | k $\Omega$      |
| AO1-, AO2- Load Capacitance                                         | $C_{LOAD}$   | AO1-, AO2-                                                    | ---              | ---        | 30               | pF              |
| RO1, RO2 Load Resistance                                            | $R_{LOAD}$   | W682510<br>W682310                                            | 0.6<br>1.2       | ---        | ---              | k $\Omega$      |
| RO1, RO2 Load Capacitance                                           | $C_{LOAD}$   | RO1, RO2                                                      | ---              | ---        | 50               | pF              |
| RO1, RO2 Output Amplitude                                           | $V_{ORO}$    | W682510<br>W682310                                            | ---              | ---        | 3.4<br>2.0       | V <sub>pp</sub> |
| RO1, RO2 Output Offset Voltage                                      | $V_{OFF,RO}$ | RO to $V_{REF}$                                               | ---              | ---        | $\pm 100$        | mV              |
| Signal Ground Voltage to $V_{SSA}$                                  | $V_{REF}$    |                                                               | $V_{DD}/2 - 0.1$ | $V_{DD}/2$ | $V_{DD}/2 + 0.1$ | V               |
| Power Supply Rejection Ratio (0 to 100 kHz to $V_{DD}$ , C-message) | PSRR         | Transmit; 50 mV <sub>pp</sub><br>Receive; 50 mV <sub>pp</sub> | --<br>--         | 40<br>40   | ---              | dBC             |

## 10.6. DIGITAL I/O

TABLE 10.61:  $\mu$ -LAW ENCODE DECODE CHARACTERISTICS

| Normalized<br>Encode<br>Decision<br>Levels | Digital Code |       |       |       |      |      |      |      | Normalized<br>Decode<br>Levels |
|--------------------------------------------|--------------|-------|-------|-------|------|------|------|------|--------------------------------|
|                                            | D7           | D6    | D5    | D4    | D3   | D2   | D1   | D0   |                                |
|                                            | Sign         | Chord | Chord | Chord | Step | Step | Step | Step |                                |
| 8159                                       |              |       |       |       |      |      |      |      | 8031                           |
| 7903                                       | 1            | 0     | 0     | 0     | 0    | 0    | 0    | 0    |                                |
| :                                          |              |       |       |       |      |      |      |      | :                              |
| 4319                                       | 1            | 0     | 0     | 0     | 1    | 1    | 1    | 1    | 4191                           |
| 4063                                       |              |       |       |       |      |      |      |      | :                              |
| :                                          | 1            | 0     | 0     | 1     | 1    | 1    | 1    | 1    | 2079                           |
| 2143                                       |              |       |       |       |      |      |      |      | :                              |
| 2015                                       | 1            | 0     | 1     | 0     | 1    | 1    | 1    | 1    | 1023                           |
| :                                          |              |       |       |       |      |      |      |      | :                              |
| 1055                                       | 1            | 0     | 1     | 1     | 1    | 1    | 1    | 1    | 495                            |
| 991                                        |              |       |       |       |      |      |      |      | :                              |
| :                                          | 1            | 0     | 1     | 1     | 1    | 1    | 1    | 1    | 231                            |
| 511                                        |              |       |       |       |      |      |      |      | :                              |
| 479                                        | 1            | 1     | 0     | 0     | 1    | 1    | 1    | 1    | 99                             |
| :                                          |              |       |       |       |      |      |      |      | :                              |
| 239                                        | 1            | 1     | 0     | 1     | 1    | 1    | 1    | 1    | 33                             |
| 223                                        |              |       |       |       |      |      |      |      | :                              |
| :                                          | 1            | 1     | 0     | 1     | 1    | 1    | 1    | 1    | 2                              |
| 103                                        |              |       |       |       |      |      |      |      | :                              |
| 95                                         | 1            | 1     | 1     | 0     | 1    | 1    | 1    | 1    | 0                              |
| :                                          |              |       |       |       |      |      |      |      |                                |
| 35                                         | 1            | 1     | 1     | 1     | 1    | 1    | 1    | 0    |                                |
| 31                                         |              |       |       |       |      |      |      |      |                                |
| :                                          | 1            | 1     | 1     | 1     | 1    | 1    | 1    | 1    |                                |
| 3                                          |              |       |       |       |      |      |      |      |                                |
| 1                                          | 1            | 1     | 1     | 1     | 1    | 1    | 1    | 1    |                                |
| 0                                          |              |       |       |       |      |      |      |      |                                |

Notes:

Sign bit = 0 for negative values, sign bit = 1 for positive values

TABLE 10.62: A-LAW ENCODE DECODE CHARACTERISTICS

| Normalized<br>Encode<br>Decision<br>Levels | Digital Code |       |       |       |      |      |      |      | Normalized<br>Decode<br>Levels |
|--------------------------------------------|--------------|-------|-------|-------|------|------|------|------|--------------------------------|
|                                            | D7           | D6    | D5    | D4    | D3   | D2   | D1   | D0   |                                |
|                                            | Sign         | Chord | Chord | Chord | Step | Step | Step | Step |                                |
| 4096                                       | 1            | 0     | 1     | 0     | 1    | 0    | 1    | 0    | 4032                           |
| 3968                                       |              |       |       |       |      |      |      |      | :                              |
| :                                          |              |       |       |       |      |      |      |      |                                |
| 2048                                       | 1            | 0     | 1     | 0     | 0    | 1    | 0    | 1    | 2112                           |
| 2048                                       |              |       |       |       |      |      |      |      | :                              |
| :                                          |              |       |       |       |      |      |      |      |                                |
| 1088                                       | 1            | 0     | 1     | 1     | 0    | 1    | 0    | 1    | 1056                           |
| 1024                                       |              |       |       |       |      |      |      |      | :                              |
| :                                          |              |       |       |       |      |      |      |      |                                |
| 544                                        | 1            | 0     | 0     | 0     | 0    | 1    | 0    | 1    | 528                            |
| 512                                        |              |       |       |       |      |      |      |      | :                              |
| :                                          |              |       |       |       |      |      |      |      |                                |
| 272                                        | 1            | 0     | 0     | 1     | 0    | 1    | 0    | 1    | 264                            |
| 256                                        |              |       |       |       |      |      |      |      | :                              |
| :                                          |              |       |       |       |      |      |      |      |                                |
| 136                                        | 1            | 1     | 1     | 0     | 0    | 1    | 0    | 1    | 132                            |
| 128                                        |              |       |       |       |      |      |      |      | :                              |
| :                                          |              |       |       |       |      |      |      |      |                                |
| 68                                         | 1            | 1     | 1     | 0     | 0    | 1    | 0    | 1    | 66                             |
| 64                                         |              |       |       |       |      |      |      |      | :                              |
| :                                          |              |       |       |       |      |      |      |      |                                |
| 2                                          | 1            | 1     | 0     | 1     | 0    | 1    | 0    | 1    | 1                              |
| 0                                          |              |       |       |       |      |      |      |      |                                |

## Notes:

1. Sign bit = 0 for negative values, sign bit = 1 for positive values
2. Digital code includes inversion of all even number bits

TABLE 10.63: PCM CODES FOR ZERO AND FULL SCALE

| Level        | $\mu$ -Law       |                          |                            | A-Law            |                          |                            |
|--------------|------------------|--------------------------|----------------------------|------------------|--------------------------|----------------------------|
|              | Sign bit<br>(D7) | Chord bits<br>(D6,D5,D4) | Step bits<br>(D3,D2,D1,D0) | Sign bit<br>(D7) | Chord bits<br>(D6,D5,D4) | Step bits<br>(D3,D2,D1,D0) |
| + Full Scale | 1                | 000                      | 0000                       | 1                | 010                      | 1010                       |
| + Zero       | 1                | 111                      | 1111                       | 1                | 101                      | 0101                       |
| - Zero       | 0                | 111                      | 1111                       | 0                | 101                      | 0101                       |
| - Full Scale | 0                | 000                      | 0000                       | 0                | 010                      | 1010                       |

TABLE 10.64: PCM CODES FOR 0DBM0 OUTPUT

| Sample | $\mu$ -Law       |                          |                            | A-Law            |                          |                            |
|--------|------------------|--------------------------|----------------------------|------------------|--------------------------|----------------------------|
|        | Sign bit<br>(D7) | Chord bits<br>(D6,D5,D4) | Step bits<br>(D3,D2,D1,D0) | Sign bit<br>(D7) | Chord bits<br>(D6,D5,D4) | Step bits<br>(D3,D2,D1,D0) |
| 1      | 0                | 001                      | 1110                       | 0                | 011                      | 0100                       |
| 2      | 0                | 000                      | 1011                       | 0                | 010                      | 0001                       |
| 3      | 0                | 000                      | 1011                       | 0                | 010                      | 0001                       |
| 4      | 0                | 001                      | 1110                       | 0                | 011                      | 0100                       |
| 5      | 1                | 001                      | 1110                       | 1                | 011                      | 0100                       |
| 6      | 1                | 000                      | 1011                       | 1                | 010                      | 0001                       |
| 7      | 1                | 000                      | 1011                       | 1                | 010                      | 0001                       |
| 8      | 1                | 001                      | 1110                       | 1                | 011                      | 0100                       |

11. TYPICAL APPLICATION CIRCUIT

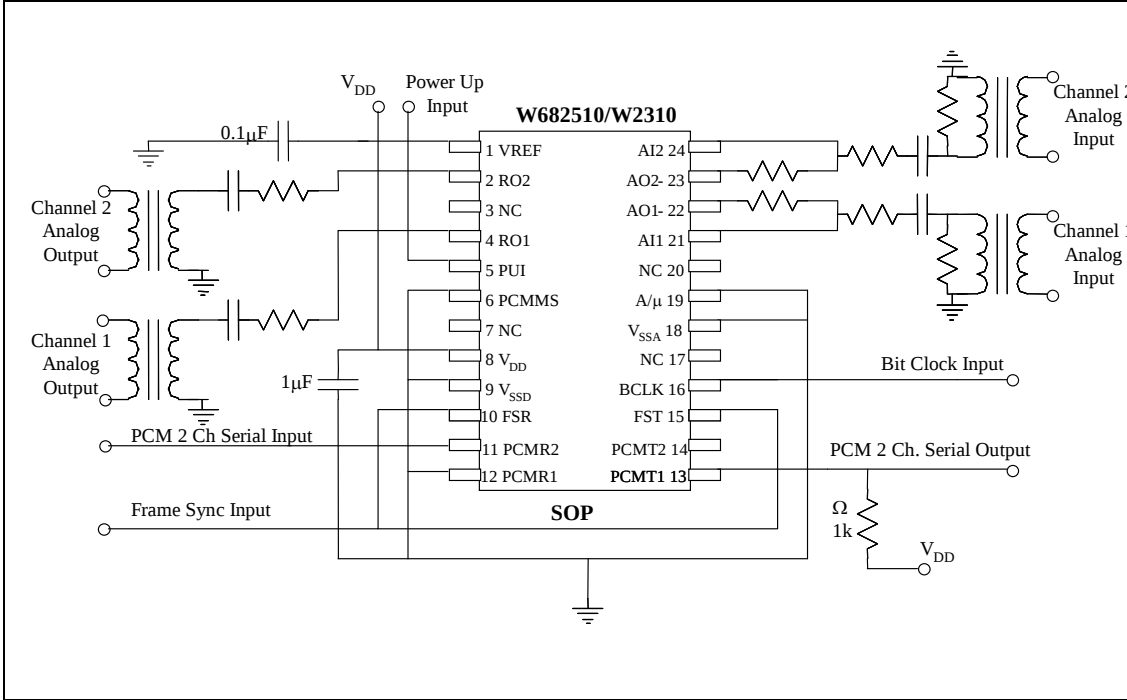


FIGURE 11.1: APPLICATION CIRCUIT FOR SERIAL MODE OPERATION

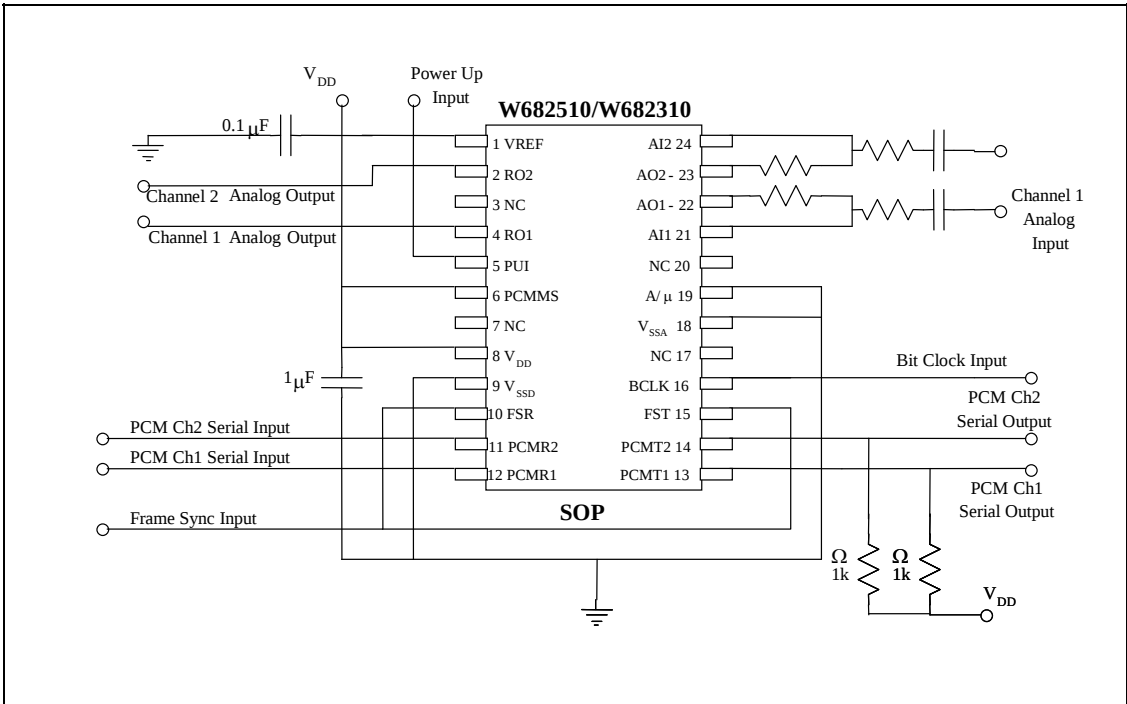
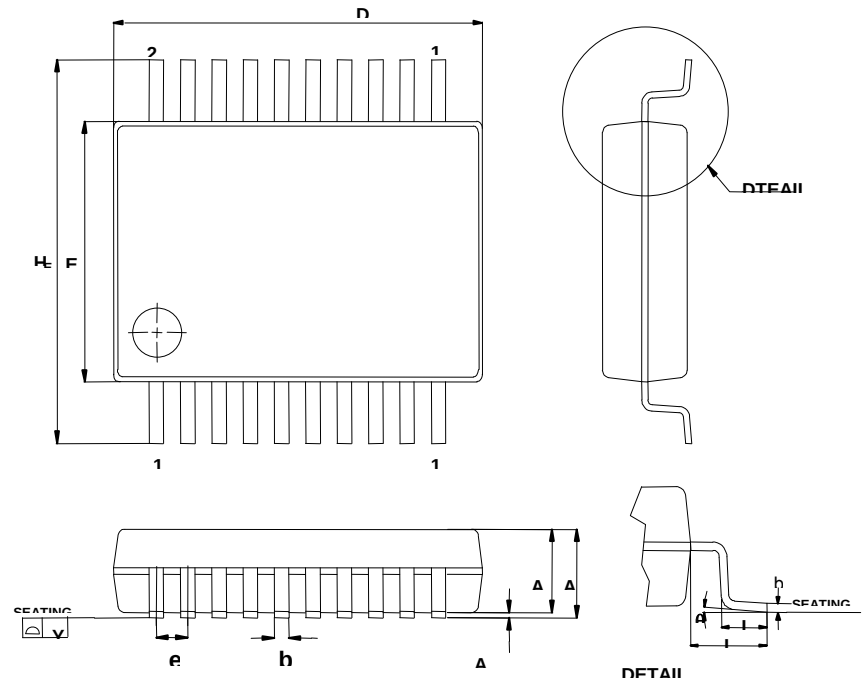


FIGURE 11.2: APPLICATION CIRCUIT FOR PARALLEL MODE OPERATION

12. PACKAGE DRAWING AND DIMENSIONS

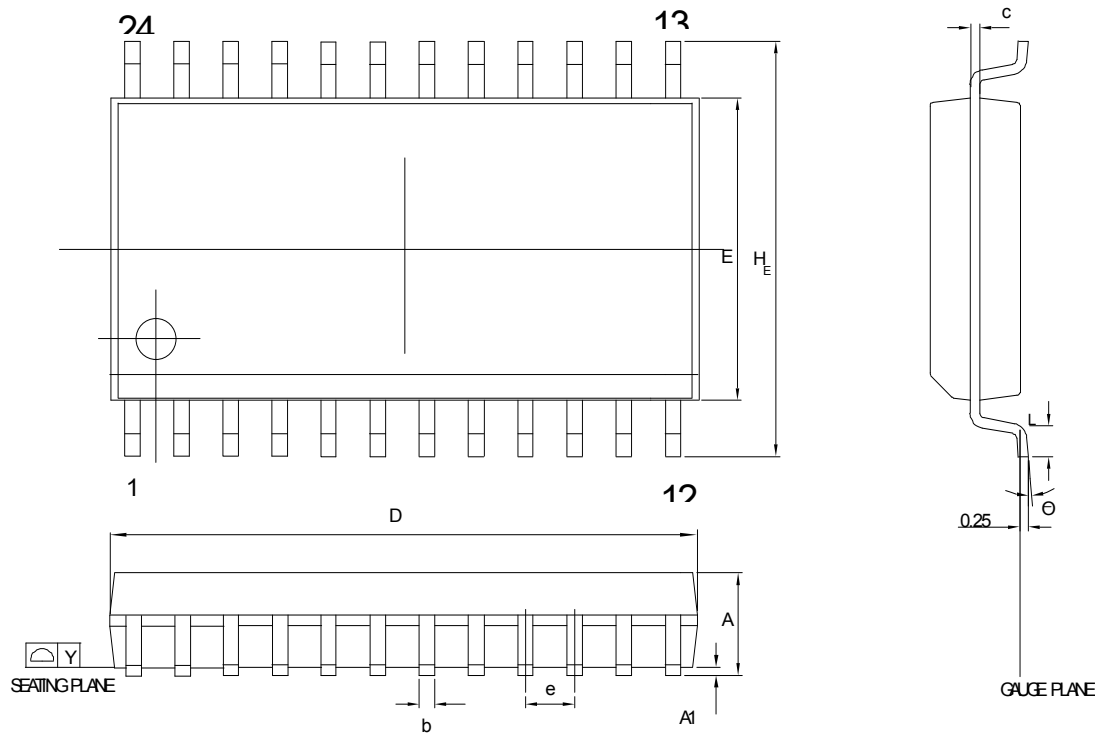
12.1. 20L SSOP – 209 MIL SHRINK SMALL OUTLINE PACKAGE DIMENSIONS



| SYMBOL         | DIMENSION (MM) |      |      | DIMENSION (INCH) |        |       |
|----------------|----------------|------|------|------------------|--------|-------|
|                | MIN.           | NOM. | MAX. | MIN.             | NOM.   | MAX.  |
| A              | -              | -    | 2.00 | -                | -      | 0.079 |
| A1             | 0.05           | -    | -    | 0.002            | -      | -     |
| A2             | 1.65           | 1.75 | 1.85 | 0.065            | 0.069  | -     |
| b              | 0.22           | -    | 0.38 | 0.009            | -      | 0.015 |
| c              | 0.09           | -    | 0.25 | 0.004            | -      | 0.010 |
| D              | 6.90           | 7.20 | 7.50 | 0.272            | 0.283  | 0.295 |
| E              | 5.00           | 5.30 | 5.60 | 0.197            | 0.209  | 0.220 |
| H <sub>E</sub> | 7.40           | 7.80 | 8.20 | 0.291            | 0.307  | 0.323 |
| e              | -              | 0.65 | -    | -                | 0.0256 | -     |
| L              | 0.55           | 0.75 | 0.95 | 0.021            | 0.030  | 0.037 |
| L1             | -              | 1.25 | -    | -                | 0.050  | -     |
| Y              | -              | -    | 0.10 | -                | -      | 0.004 |
| $\bar{0}$      | 0°             | -    | 8°   | 0                | -      | 8°    |



12.3. 24 SOP – 300 MIL

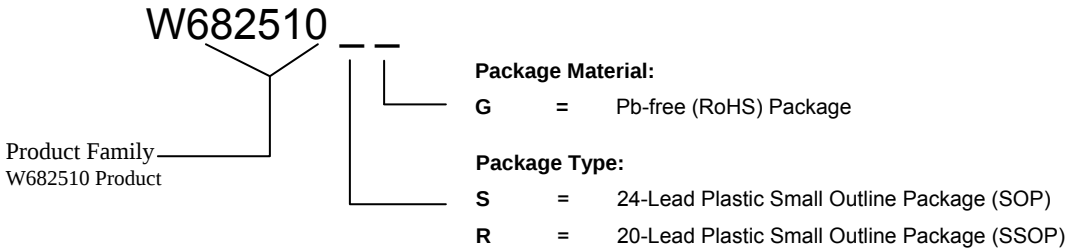


| SYMBOL         | DIMENSION (MM) |       | DIMENSION (INCH) |       |
|----------------|----------------|-------|------------------|-------|
|                | MIN.           | MAX.  | MIN.             | MAX.  |
| A              | 2.35           | 2.65  | 0.093            | 0.104 |
| A1             | 0.10           | 0.30  | 0.004            | 0.012 |
| b              | 0.33           | 0.51  | 0.013            | 0.020 |
| c              | 0.23           | 0.32  | 0.009            | 0.013 |
| E              | 7.40           | 7.60  | 0.291            | 0.299 |
| D              | 15.20          | 15.60 | 0.598            | 0.614 |
| e              | 1.27 BSC       |       | 0.050 BSC        |       |
| H <sub>E</sub> | 10.00          | 10.65 | 0.394            | 0.419 |
| Y              |                | 0.10  |                  | 0.004 |
| L              | 0.10           | 1.27  | 0.016            | 0.050 |
| θ              | 0°             | 8°    | 0                | 8°    |



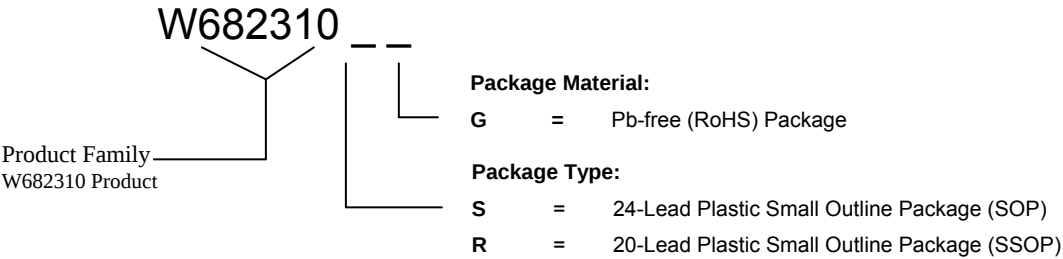
13. ORDERING INFORMATION

Product Number Descriptor Key



When ordering W682510 series devices, please refer to the following part numbers.

| Part Number |
|-------------|
| W682510SG   |
| W682510RG   |



When ordering W682310 series devices, please refer to the following part numbers.

| Part Number |
|-------------|
| W682310SG   |
| W682310RG   |

For the latest product information, access Nuvoton's worldwide website at <http://www.nuvoton-usa.com>



#### 14. VERSION HISTORY

| VERSION | DATE         | PAGE | DESCRIPTION                                         |
|---------|--------------|------|-----------------------------------------------------|
| 0.31    | Mar 2003     | All  | Preliminary Specifications                          |
| 0.34    | Apr. 2003    |      | Updates                                             |
| 0.35    | May 2003     |      | Frequency response updated                          |
| A10     | April 2005   | 35   | Add Important Notice                                |
| A11     | January 2009 | 24   | Idle channel Noise (u-Law; C-message) value updated |
|         |              | 32   | PDIP no longer support                              |
|         |              | 32   | Leaded packages are no longer supported             |

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