83C196EA CHMOS 16-Bit Microcontroller

Datasheet - Automotive

Advance Information

Product Features

- 40 MHz operation
- Optional clock doubler
- 2 Mbytes of linear address space
- 1 Kbyte of register RAM
- 3 Kbytes of code RAM
- 8 Kbytes of ROM
- Register-to-register architecture
- Stack overflow/underflow monitor with user-defined upper and lower stack pointer boundary limits
- 2 peripheral interrupt handlers (PIH) provide direct hardware handling of up to 16 peripheral interrupts
- Peripheral transaction server (PTS) with high-speed, microcoded interrupt service routines
- Up to 83 I/O port pins
- 2 full-duplex serial ports with dedicated baud-rate generators
- Enhanced synchronous serial unit
- 8 pulse-width modulator (PWM) outputs with 8-bit resolution
- 16-bit watchdog timer
- Sixteen 10-bit A/D channels with auto-scan mode and dedicated results registers
- Serial debug unit provides read and write access to code RAM with no CPU overhead
- Chip-select unit (CSU)
- 3 chip-select pins
- Dynamic demultiplexed/multiplexed address/data bus for each chip-select
- Programmable wait states (0, 1, 2, or 3) for each chip-select
- Programmable bus width (8- or 16-bit) for each chip-select
- Programmable address range for each chip-select
- Event processor array (EPA)
- 4 flexible 16-bit timer/counters
- 17 high-speed capture/compare channels
- 8 output-only channels capture value of any other timer upon compare, providing easy conversion between angle and time domains
- Programmable clock output signal
- 160-pin QFP package
- Complete system development support
- High-speed CHMOS technology

The 83C196EA is the first member of a new family of microcontrollers with features that are useful in automotive applications, such as powertrain control. Two Mbytes of linear address space provide more space for high-level language compilation. A demultiplexed address/data bus and three chip-select signals make it easier to design low-cost memory solutions. The external bus can dynamically switch between multiplexed and demultiplexed operation.

Notice: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Order Number: 272788-006
October 2000

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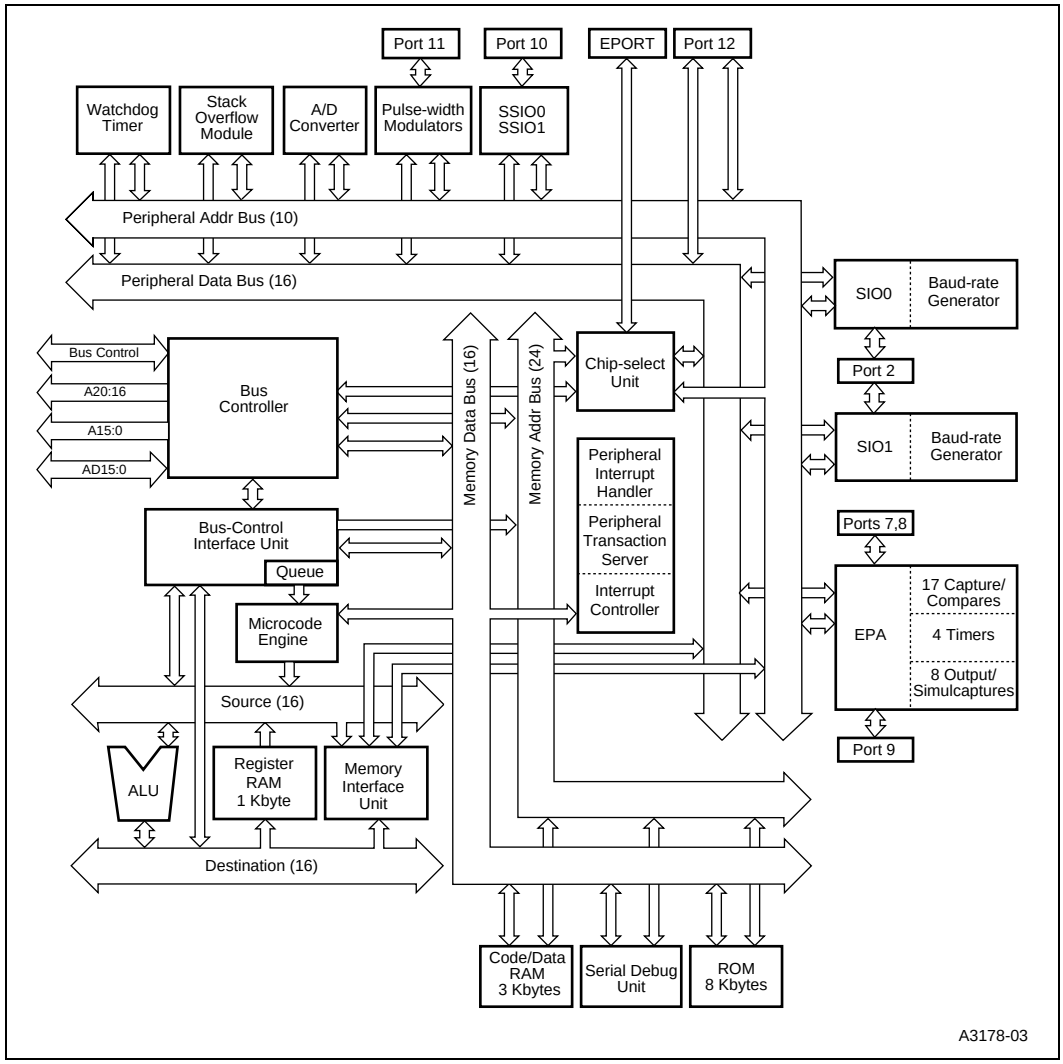
1.0 Product Overview

Figure 1. 83C196EA Block Diagram



The 83C196EA is highly integrated with an enhanced peripheral set. The serial debug unit (SDU) provides system debug and development capabilities. The SDU can set a single hardware breakpoint and provides read and write access to code RAM through a high-speed, dedicated serial link. A stack overflow/underflow monitor assists in code development by causing an unmaskable interrupt if the stack pointer crosses a user-defined boundary. The 16-channel A/D converter supports an auto-scan mode that operates with no CPU overhead. Each A/D channel has a dedicated result register. The EPA supports high-speed input captures and output compares with 17 programmable, high-speed capture/compare channels. Eight output-only channels provide support for time-base conversions by capturing the value of one of four timers when a compare occurs.

2.0 Nomenclature Overview

Figure 2. Product Nomenclature

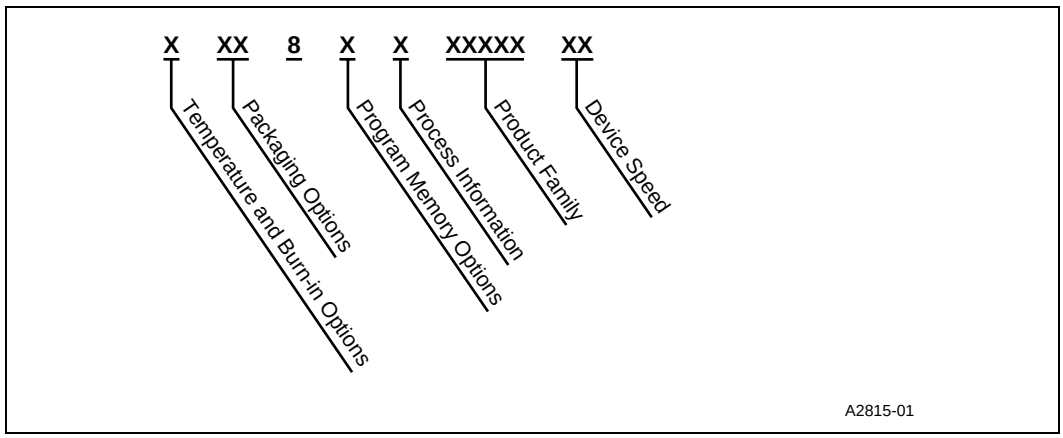
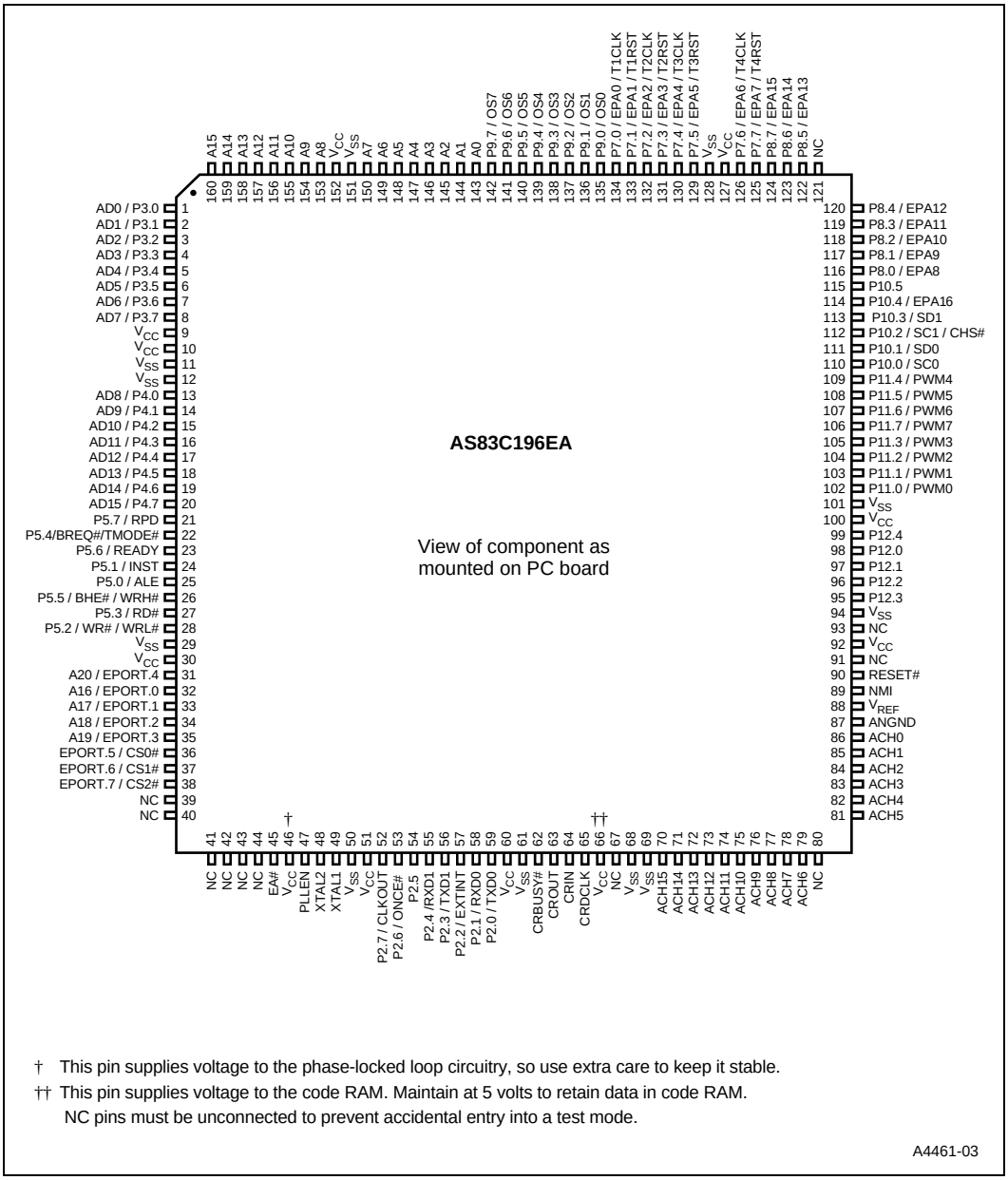


Table 1. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	A	Automotive operating temperature range (–40° C to 125° C case) with Intel standard burn-in.
Packaging Options	S	QFP
Program Memory Options	3	Internal ROM
Process Information	C	CHMOS
Product Family	196EA	
Device Speed	no mark	40 MHz

3.0 Pinout

Figure 3. 83C196EA 160-pin QFP Package



† This pin supplies voltage to the phase-locked loop circuitry, so use extra care to keep it stable.

†† This pin supplies voltage to the code RAM. Maintain at 5 volts to retain data in code RAM.

NC pins must be unconnected to prevent accidental entry into a test mode.

A4461-03

Table 2. 83C196EA 160-pin QFP Package Pin Assignments

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AD0 / P3.0	41	NC	81	ACH5	121	NC
2	AD1 / P3.1	42	NC	82	ACH4	122	P8.5 / EPA13
3	AD2 / P3.2	43	NC	83	ACH3	123	P8.6 / EPA14
4	AD3 / P3.3	44	NC	84	ACH2	124	P8.7 / EPA15
5	AD4 / P3.4	45	EA#	85	ACH1	125	P7.7 / EPA7 / T4RST
6	AD5 / P3.5	46	V_{CC}	86	ACH0	126	P7.6 / EPA6 / T4CLK
7	AD6 / P3.6	47	PLLEN	87	ANGND	127	V_{CC}
8	AD7 / P3.7	48	XTAL2	88	V_{REF}	128	V_{SS}
9	V_{CC}	49	XTAL1	89	NMI	129	P7.5 / EPA5 / T3RST
10	V_{CC}	50	V_{SS}	90	RESET#	130	P7.4 / EPA4 / T3CLK
11	V_{SS}	51	V_{CC}	91	NC	131	P7.3 / EPA3 / T2RST
12	V_{SS}	52	P2.7 / CLKOUT	92	V_{CC}	132	P7.2 / EPA2 / T2CLK
13	AD8 / P4.0	53	P2.6 / ONCE#	93	NC	133	P7.1 / EPA1 / T1RST
14	AD9 / P4.1	54	P2.5	94	V_{SS}	134	P7.0 / EPA0 / T1CLK
15	AD10 / P4.2	55	P2.4 / RXD1	95	P12.3	135	P9.0 / OS0
16	AD11 / P4.3	56	P2.3 / TXD1	96	P12.2	136	P9.1 / OS1
17	AD12 / P4.4	57	P2.2 / EXTINT	97	P12.1	137	P9.2 / OS2
18	AD13 / P4.5	58	P2.1 / RXD0	98	P12.0	138	P9.3 / OS3
19	AD14 / P4.6	59	P2.0 / TXD0	99	P12.4	139	P9.4 / OS4
20	AD15 / P4.7	60	V_{CC}	100	V_{CC}	140	P9.5 / OS5
21	P5.7 / RPD	61	V_{SS}	101	V_{SS}	141	P9.6 / OS6
22	P5.4/BREQ#/TMODE#	62	CRBUSY#	102	P11.0 / PWM0	142	P9.7 / OS7
23	P5.6 / READY	63	CROUT	103	P11.1 / PWM1	143	A0
24	P5.1 / INST	64	CRIN	104	P11.2 / PWM2	144	A1
25	P5.0 / ALE	65	CRDCLK	105	P11.3 / PWM3	145	A2
26	P5.5 / BHE# / WRH#	66	V_{CC}	106	P11.7 / PWM7	146	A3
27	P5.3 / RD#	67	NC	107	P11.6 / PWM6	147	A4
28	P5.2 / WR# / WRL#	68	V_{SS}	108	P11.5 / PWM5	148	A5
29	V_{SS}	69	V_{SS}	109	P11.4 / PWM4	149	A6
30	V_{CC}	70	ACH15	110	P10.0 / SC0	150	A7
31	A20 / EPORT.4	71	ACH14	111	P10.1 / SD0	151	V_{SS}
32	A16 / EPORT.0	72	ACH13	112	P10.2 / SC1	152	V_{CC}
33	A17 / EPORT.1	73	ACH12	113	P10.3 / SD1	153	A8
34	A18 / EPORT.2	74	ACH11	114	P10.4 / EPA16	154	A9
35	A19 / EPORT.3	75	ACH10	115	P10.5	155	A10
36	EPORT.5 / CS0#	76	ACH9	116	P8.0 / EPA8	156	A11
37	EPORT.6 / CS1#	77	ACH8	117	P8.1 / EPA9	157	A12
38	EPORT.7 / CS2#	78	ACH7	118	P8.2 / EPA10	158	A13
39	NC	79	ACH6	119	P8.3 / EPA11	159	A14
40	NC	80	NC	120	P8.4 /EPA12	160	A15

Table 3. Pin Assignment Arranged by Functional Categories (Sheet 1 of 2)

Addr & Data	
Name	Pin
A0	143
A1	144
A2	145
A3	146
A4	147
A5	148
A6	149
A7	150
A8	153
A9	154
A10	155
A11	156
A12	157
A13	158
A14	159
A15	160
A16	32
A17	33
A18	34
A19	35
A20	31
AD0	1
AD1	2
AD2	3
AD3	4
AD4	5
AD5	6
AD6	7
AD7	8
AD8	13
AD9	14
AD10	15
AD11	16
AD12	17
AD13	18
AD14	19
AD15	20

Input/Output			
Name	Pin	Name	Pin
P2.0 / TXD0	59	P7.0 / EPA0 / T1CLK	134
P2.1 / RXD0	58	P7.1 / EPA1 / T1RST	133
P2.2	57	P7.2 / EPA2 / T2CLK	132
P2.3 / TXD1	56	P7.3 / EPA3 / T2RST	131
P2.4 / RXD1	55	P7.4 / EPA4 / T3CLK	130
P2.5	54	P7.5 / EPA5 / T3RST	129
P2.6	53	P7.6 / EPA6 / T4CLK	126
P2.7	52	P7.7 / EPA7 / T4RST	125
P3.0	1	P8.0 / EPA8	116
P3.1	2	P8.1 / EPA9	117
R3.2	3	P8.2 / EPA10	118
P3.3	4	P8.3 / EPA11	119
P3.4	5	P8.4 / EPA12	120
P3.5	6	P8.5 / EPA13	122
P3.6	7	P8.6 / EPA14	123
P3.7	8	P8.7 / EPA15	124
P4.0	13	P9.0 / OS0	135
P4.1	14	P9.1 / OS1	136
P4.2	15	P9.2 / OS2	137
P4.3	16	P9.3 / OS3	138
P4.4	17	P9.4 / OS4	139
P4.5	18	P9.5 / OS5	140
P4.6	19	P9.6 / OS6	141
P4.7	20	P9.7 / OS7	142
P5.0	25	P10.0 / SC0	110
P5.1	24	P10.1 / SD0	111
P5.2	28	P10.2 / SC1	112
P5.3	27	P10.3 / SD1	113
P5.4	22	P10.4 / EPA16	114
P5.5	26	P10.5	115
P5.6	23	P11.0 / PWM0	102
P5.7	21	P11.1 / PWM1	103
EPORT.0	32	P11.2 / PWM2	104
EPORT.1	33	P11.3 / PWM3	105
EPORT.2	34	P11.4 / PWM4	109
EPORT.3	35	P11.5 / PWM5	108
EPORT.4	31	P11.6 / PWM6	107
EPORT.5	36	P11.7 / PWM7	106
EPORT.6	37	P12.0	98
EPORT.7	38	P12.1	97
		P12.2	96
		P12.3	95
		P12.4	99

Analog Inputs	
Name	Pin
ACH0	86
ACH1	85
ACH2	84
ACH3	83
ACH4	82
ACH5	81
ACH6	79
ACH7	78
ACH8	77
ACH9	76
ACH10	75
ACH11	74
ACH12	73
ACH13	72
ACH14	71
ACH15	70

Bus Control & Status	
Name	Pin
ALE	25
BHE#/WRH#	26
BREQ#	22
CS0#	36
CS1#	37
CS2#	38
INST	24
RD#	27
READY	23
WR#/WRL#	28

Processor Control	
Name	Pin
CLKOUT	52
EA#	45
EXTINT	57
NMI	89
ONCE#	53
PLLEN	47
RESET#	90
RPD	21
TMODE#	22
XTAL1	49
XTAL2	48

Table 3. Pin Assignment Arranged by Functional Categories (Sheet 2 of 2)

Power & Ground	
Name	**Pins**
ANGND	87
V_{CC}	9, 10, 30, 46†, 51, 60, 66††, 92, 100, 127, 152
V_{SS}	11, 12, 29, 50, 61, 68, 69, 94, 101, 128, 151
V_{REF}	88

Code Debug	
Name	**Pin**
CRBUSY#	62
CRDCLK	65
CRIN	64
CROUT	63

No Connection	
Name	**Pins**
NC†††	39–44, 67, 69, 80, 91, 93, 121

† This pin supplies voltage to the phase-locked loop circuitry, so use extra care to keep it stable.

†† This pin supplies voltage to code RAM. To retain data, maintain 5 volts.

†††Always leave NC (no connect) pins unconnected to prevent accidental entry into test modes.

4.0 Signals

Table 4. Signal Descriptions (Sheet 1 of 7)

Name	Type	Description
A15:0	O	System Address Bus These address lines provide address bits 0–15 during the entire external memory cycle during both multiplexed and demultiplexed bus modes.
A20:16	I/O	Address Lines 16–20 These address lines provide address bits 16–20 during the entire external memory cycle, supporting extended addressing of the 2 Mbyte address space. **NOTE:** Internally, there are 24 address bits; however, only 21 external address pins (A20:0) are implemented. The internal address space is 16 Mbytes (000000 FFFFFFH) and the external address space is 2 Mbytes (00000 1FFFFFH). The device resets to FF2080H in internal memory or 1F2080H in external memory. A20:16 are multiplexed with EPORT.4:0.
ACH15:0	I	Analog Channels These pins are analog inputs to the A/D converter. The ANGND and V_{REF} pins must be connected for the A/D converter to function.
AD15:0	I/O	Address/Data Lines The function of these pins depend on the bus size and mode. When a bus access is not occurring, these pins revert to their I/O port function. **16-bit Multiplexed Bus Mode**: AD15:0 drive address bits 0–15 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle. **8-bit Multiplexed Bus Mode**: AD15:8 drive address bits 8–15 during the entire bus cycle. AD7:0 drive address bits 0–7 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle. **16-bit Demultiplexed Mode**: AD15:0 drive or receive data during the entire bus cycle. **8-bit Demultiplexed Mode**: AD7:0 drive or receive data during the entire bus cycle. AD15:8 drive the data that is currently on the high byte of the internal bus. AD7:0 share package pins P3.7:0. AD15:8 share package pins P4.7:0.
ALE	O	Address Latch Enable This active-high output signal is asserted only during external memory cycles. ALE signals the start of an external bus cycle and indicates that valid address information is available on the system address/data bus (A20:16 and AD15:0 for a multiplexed bus; A20:0 for a demultiplexed bus). An external latch can use this signal to demultiplex address bits 0–15 from the address/data bus in multiplexed mode. ALE shares a package pin with P5.0.
ANGND	GND	Analog Ground ANGND must be connected for A/D converter operation. ANGND and V_{SS} should be nominally at the same potential.

Table 4. Signal Descriptions (Sheet 2 of 7)

Name	Type	Description
BHE#	O	Byte High Enable† During 16-bit bus cycles, this active-low output signal is asserted for word and high-byte reads and writes to external memory. BHE# indicates that valid data is being transferred over the upper half of the system data bus. Use BHE#, in conjunction with AD0, to determine which memory byte is being transferred over the system bus: **BHE#AD0Byte(s) Accessed** 00both bytes 01high byte only 10low byte only BHE# shares a package pin with P5.5 and WRH#. † The chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.
BREQ#	O	Bus Request This active-low output signal is asserted during a hold cycle when the bus controller has a pending external memory cycle. You must enable the bus-hold protocol before using this signal. BREQ# shares a package pin with P5.4.
CLKOUT	O	Clock Output Output of the internal clock generator. The CLKOUT frequency can be programmed to one of five frequencies: the internal operating frequency (f) divided by a factor of two, four, eight, or sixteen, or the same frequency as the oscillator input (F_{XTAL1}). CLKOUT has a 50% duty cycle. CLKOUT shares a package pin with P2.7
CRBUSY#	O	Code RAM Busy This signal indicates that the serial debug unit (SDU) is not ready to conduct a transaction.
CRDCLK	I	Code RAM Clock Provides the clock signal for the serial debug unit (SDU). The maximum clock frequency equals the operating frequency (f) divided by two.
CRIN	I	Code RAM Data Input Serial input for test instructions and data into the serial debug unit (SDU). Data is transferred in 8-bit bytes with the most-significant bit (MSB) first. Each bit is sampled on the rising edge of CRDCLK.
CROUT	O	Code RAM Data Output Serial output for data from the serial debug unit (SDU). Data is transferred in 8-bit bytes with the most-significant bit (MSB) first. Each bit is valid on the rising edge of CRDCLK.
CS2:0#	O	Chip-select Lines 0–2 The active-low output CS*x*# is asserted during an external memory cycle when the address to be accessed is in the range programmed for chip select *x*. If the external memory address is outside the range assigned to the three chip selects, no chip-select output is asserted and the bus configuration defaults to the CS2# values. Immediately following reset, CS0# is automatically assigned to the range FF2000 FF20FFH (1F2000 1F20FFH if external). CS2:0# share package pins with EPORT.7:5.

Table 4. Signal Descriptions (Sheet 3 of 7)

Name	Type	Description
EA#	I	External Access This input determines whether memory accesses to special-purpose and program memory partitions (FF2000 FF3FFFH) are directed to internal or external memory. These accesses are directed to internal memory if EA# is held high and to external memory if EA# is held low. For an access to any other memory location, the value of EA# is irrelevant. EA# is sampled and latched only on the rising edge of RESET#. Changing the level of EA# after reset has no effect. On devices with no internal nonvolatile memory, always connect EA# to V_{SS}.
EPA16:0	I/O	Event Processor Array (EPA) Capture/Compare Channels High-speed input/output signals for the EPA capture/compare channels. EPA16:0 share package pins with the following signals: EPA0/P7.0/T1CLK, EPA1/P7.1/T1RST, EPA2/P7.2/T2CLK, EPA3/P7.3/T2RST, EPA4/P7.4/T3CLK, EPA5/P7.5/T3RST, EPA6/P7.6/T4CLK, EPA7/P7.7/T4RST, EPA8/P8.0, EPA9/P8.1, EPA10/P8.2, EPA11/P8.3, EPA12/P8.4, EPA13/P8.5, EPA14/P8.6, EPA15/P8.7, and EPA16/P10.4.
EPORT.7:0	I/O	Extended Addressing Port This is a standard 8-bit, bidirectional port. EPORT.4:0 share package pins with A20:16. EPORT7:5 share package pins with CS2:0#.
EXTINT	I	External Interrupt In normal operating mode, a rising edge on EXTINT sets the EXTINT interrupt pending bit. EXTINT is sampled during phase 2 (CLKOUT high). The minimum high time is one state time. In powerdown mode, asserting the EXTINT signal for at least 50 ns causes the device to resume normal operation. The interrupt need not be enabled, but the pin must be configured as a special-function input. If the EXTINT interrupt is enabled, the CPU executes the interrupt service routine. Otherwise, the CPU executes the instruction that immediately follows the command that invoked the power-saving mode. In idle mode, asserting any enabled interrupt causes the device to resume normal operation. EXTINT shares a package pin with P2.2.
INST	O	Instruction Fetch This active-high output signal is valid only during external memory bus cycles. When high, INST indicates that an instruction is being fetched from external memory. The signal remains high during the entire bus cycle of an external instruction fetch. INST is low for data accesses, including interrupt vector fetches and chip configuration byte reads. INST is low during internal memory fetches. INST shares a package pin with P5.1.
NMI	I	Nonmaskable Interrupt In normal operating mode, a rising edge on NMI generates a nonmaskable interrupt. NMI has the highest priority of all prioritized interrupts. Assert NMI for greater than one state time to guarantee that it is recognized.
ONCE#	I	On-circuit Emulation Holding ONCE# low during the rising edge of RESET# places the device into on-circuit emulation (ONCE) mode. PLLEN must also be held low. This mode puts all pins into a high-impedance state, thereby isolating the device from other components in the system. The value of ONCE# is latched when the RESET# pin goes inactive. While the device is in ONCE mode, you can debug the system using a clip-on emulator. To exit ONCE mode, reset the device by pulling the RESET# signal low. To prevent inadvertent entry into ONCE mode, either configure this pin as an output or hold it high during reset and ensure that your system meets the V_{IH} specification. ONCE# shares a package pin with P2.6.

Table 4. Signal Descriptions (Sheet 4 of 7)

Name	Type	Description
OS7:0	O	Event Processor Array (EPA) Compare-only Channels with Simulcapture Outputs of the EPA's compare-only channels. These pins are multiplexed with port 9 and may be configured as standard I/O. OS7:0 share package pins with P9.7:0.
P2.7:0	I/O	Port 2 This is a standard, 8-bit, bidirectional port that is multiplexed with individually selectable special-function signals. P2.6 is multiplexed with ONCE#. To prevent inadvertent entry into ONCE mode, either configure this pin as an output or hold it high during reset and ensure that your system meets the V_{IH} specification. Port 2 shares package pins with the following signals: P2.0/TXD0, P2.1/RXD0, P2.2/EXTINT, P2.3/TXD1, P2.4/RXD1, P2.6/ONCE#, and P2.7/CLKOUT.
P3.7:0	I/O	Port 3 This is a memory-mapped, 8-bit, bidirectional port with programmable open-drain or complementary output modes. The pins are shared with the multiplexed address/data bus, which has complementary drivers. P3.7:0 share package pins with AD7:0.
P4.7:0	I/O	Port 4 This is a memory-mapped, 8-bit, bidirectional port with programmable open-drain or complementary output modes. The pins are shared with the multiplexed address/data bus, which has complementary drivers. P4.7:0 share package pins with AD15:8.
P5.7:0	I/O	Port 5 This is a memory-mapped, 8-bit, bidirectional port that is multiplexed with individually selectable control signals. P5.4 is multiplexed with TMODE#. If this pin is held low during reset, the device will enter a test mode. To prevent inadvertent entry into a reserved test mode, either configure this pin as an output or hold it high during reset and ensure that your system meets the V_{IH} specification. Port 5 shares package pins with the following signals: P5.0/ALE, P5.1/INST, P5.2/WR#/WRL#, P5.3/RD#, P5.4/BREQ#/TMODE#, P5.5/BHE#/WRH#, P5.6/READY, and P5.7/RPD.
P7.7:0	I/O	Port 7 This is a standard, 8-bit, bidirectional port that is multiplexed with individually selectable special-function signals. Port 7 shares package pins with the following signals: P7.0/EPA0/T1CLK, P7.1/EPA1/T1RST, P7.2/EPA2/T2CLK, P7.3/EPA3/T2RST, P7.4/EPA4/T3CLK, P7.5/EPA5/T3RST, P7.6/EPA6/T4CLK, and P7.7/EPA7/T4RST.
P8.7:0	I/O	Port 8 This is a standard, 8-bit, bidirectional port that is multiplexed with individually selectable special-function signals. P8.7:0 share package pins with EPA15:8.
P9.7:0	I/O	Port 9 This is a standard, 8-bit, bidirectional port that is multiplexed with individually selectable special-function signals. P9.7:0 share package pins with OS7:0.
P10.5:0	I/O	Port 10 This is a standard, 6-bit, bidirectional port that is multiplexed with individually selectable special-function signals. Port 10 shares package pins with the following signals: P10.0/SC0, P10.1/SD0, P10.2/SC1, P10.3/SD1, P10.4/EPA16, and P10.5.

Table 4. Signal Descriptions (Sheet 5 of 7)

Name	Type	Description
P11.7:0	I/O	Port 11 This is a standard, 8-bit, bidirectional port that is multiplexed with individually selectable special-function signals. P11.7:0 share package pins with PWM7:0.
P12.4:0	I/O	Port 12 This is a memory-mapped, 5-bit, bidirectional port. P12.2:0 select the test-ROM execution mode.
PLLEN	I	Phase-locked Loop Enable This active-high input pin enables the on-chip clock doubler. This pin must be held low when entering on-circuit emulation (ONCE) mode.
PWM7:0	O	Pulse Width Modulator Outputs These are PWM output pins with high-current drive capability. PWM7:0 share package pins with P11.7:0.
RD#	O	Read Read-signal output to external memory. RD# is asserted only during external memory reads. RD# shares a package pin with P5.3.
READY	I	Ready Input This active-high input signal is used to lengthen external memory cycles for slow memory by generating wait states in addition to the wait states that are generated internally. When READY is high, CPU operation continues in a normal manner with wait states inserted as programmed in the chip configuration registers or the chip-select *x* bus control register. READY is ignored for all internal memory accesses. READY shares a package pin with P5.6.
RESET#	I/O	Reset A level-sensitive reset input to and open-drain system reset output from the microcontroller. Either a falling edge on RESET# or an internal reset turns on a pull-down transistor connected to the RESET# pin for 16 state times. In the powerdown and idle modes, asserting RESET# causes the chip to reset and return to normal operating mode. After a device reset, the first instruction fetch is from FF2080H (or 1F2080H in external memory).
RPD	I	Return from Powerdown Timing pin for the return-from-powerdown circuit. If your application uses powerdown mode, connect a capacitor between RPD and V_{SS} if **either** of the following conditions are true. • the internal oscillator is the clock source • the phase-locked loop (PLL) circuitry is enabled (see PLLEN signal description) The capacitor causes a delay that enables the oscillator and PLL circuitry to stabilize before the internal CPU and peripheral clocks are enabled. The capacitor is not required if your application uses powerdown mode and if **both** of the following conditions are true. • an external clock input is the clock source • the phase-locked loop circuitry is disabled If your application does not use powerdown mode, leave this pin unconnected. RPD shares a package pin with P5.7.
RXD1:0	I/O	Receive Serial Data 0 and 1 In modes 1, 2, and 3, RXD0 and 1 receive serial port input data. In mode 0, they functions as either inputs or open-drain outputs for data. RXD0 shares a package pin with P2.1 and RXD1 shares a package pin with P2.4.

Table 4. Signal Descriptions (Sheet 6 of 7)

Name	Type	Description
SC1:0	I/O	Clock Pins for SSIO0 and 1 For handshaking mode, configure SC1:0 as open-drain outputs. This pin carries a signal only during receptions and transmissions. When the SSIO port is idle, the pin remains either high (with handshaking) or low (without handshaking). SC0 shares a package pin with P10.0, and SC1 shares a package pin with P10.2.
SD1:0	I/O	Data Pins for SSIO0 and 1 These pins are the data I/O pins for SSIO0 and 1. SD0 shares a package pin with P10.1, and SD1 shares a package pin with P10.1.
T1CLK	I	Timer 1 External Clock External clock for Timer 1.Timer 1 is programmable to increment or decement on the rising edge, the falling edge, or both rising and falling edges of T1CLK. T1CLK shares a package pin with P7.0 and EPA0.
T2CLK	I	Timer 2 External Clock External clock for timer 2. Timer 2 is programmable to increment or decement on the rising edge, the falling edge, or both rising and falling edges of T2CLK. External clock for the serial I/O baud-rate generator input (program selectable). T2CLK shares a package pin with P7.2 and EPA2.
T3CLK	I	Timer 3 External Clock External clock for timer 3. Timer 3 is programmable to increment or decement on the rising edge, the falling edge, or both rising and falling edges of T3CLK. T3CLK shares a package pin with P7.4 and EPA4.
T4CLK	I	Timer 4 External Clock External clock for timer 4. Timer 2 is programmable to increment or decement on the rising edge, the falling edge, or both rising and falling edges of T4CLK. T4CLK shares a package pin with P7.6 and EPA6.
T1RST	I	Timer 1 External Reset External reset for timer 1. Timer 1 is programmable to reset on the rising edge, the falling edge, or both rising and falling edges of T1RST. T1RST shares a package pin with P7.1 and EPA1.
T2RST	I	Timer 2 External Reset External reset for timer 2. Timer 2 is programmable to reset on the rising edge, the falling edge, or both rising and falling edges of T2RST. T2RST shares a package pin with P7.3 and EPA3.
T3RST	I	Timer 3 External Reset External reset for timer 3. Timer 3 is programmable to reset on the rising edge, the falling edge, or both rising and falling edges of T3RST. T3RST shares a package pin with P7.5 and EPA5.
T4RST	I	Timer 4 External Reset External reset for timer 4. Timer 4 is programmable to reset on the rising edge, the falling edge, or both rising and falling edges of T4RST. T4RST shares a package pin with P7.6 and EPA6.
TMODE#	I	Test-Mode Entry If this pin is held low during reset, the device will enter a test mode. The value of several other pins defines the actual test mode. All test modes, except test-ROM execution, are reserved for Intel factory use. If you choose to configure this signal as an input, always hold it high during reset and ensure that your system meets the V_{IH} specification to prevent inadvertent entry into test mode. TMODE# shares a package pin with P5.4 and BREQ#.

Table 4. Signal Descriptions (Sheet 7 of 7)

Name	Type	Description
TXD1:0	O	Transmit Serial Data 0 and 1 In serial I/O modes 1, 2, and 3, TXD0 and 1 transmit serial port output data. In mode 0, they are the serial clock output. TXD0 shares a package pin with P2.0 and TXD1 shares a package pin with P2.3.
V_{CC}	PWR	Digital Supply Voltage Connect each V_{CC} pin to the digital supply voltage.
V_{REF}	PWR	Reference Voltage for the A/D Converter This pin also supplies operating voltage to the analog portion of the A/D converter.
V_{SS}	GND	Digital Circuit Ground These pins supply ground for the digital circuitry. Connect each V_{SS} pin to ground through the lowest possible impedance path.
WR#	O	Write† This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes. WR# is multiplexed with P5.2 and WRL#. † The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
WRH#	O	Write High† During 16-bit bus cycles, this active-low output signal is asserted for high-byte writes and word writes to external memory. During 8-bit bus cycles, WRH# is asserted for all write operations. WRH# shares a package pin with P5.5 and BHE#. † The chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.
WRL#	O	Write Low† During 16-bit bus cycles, this active-low output signal is asserted for low-byte writes and word writes to external memory. During 8-bit bus cycles, WRL# is asserted for all write operations. WRL# shares a package pin with P5.2 and WR#. † The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
XTAL1	I	Input Crystal/Resonator or External Clock Input Input to the on-chip oscillator and the internal clock generators. The internal clock generators provide the peripheral clocks, CPU clock, and CLKOUT signal. When using an external clock source instead of the on-chip oscillator, connect the clock input to XTAL1. The external clock signal must meet the V_{IH} specification for XTAL1.
XTAL2	O	Inverted Output for the Crystal/Resonator Output of the on-chip oscillator inverter. Leave XTAL2 floating when the design uses an external clock source instead of the on-chip oscillator.

5.0 Address Map

Table 5. 83C196EA Address Map

Hex Address	Description (Note 1, Note 2)	Addressing Modes
FFFFFF FF4000	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
FF3FFF FF2400	Program memory (Note 3)	Indirect, indexed, extended
FF23FF FF2140	Program memory (Note 3)	Indirect, indexed, extended
FF213F FF20C0	Special-purpose memory (PIH vectors; Note 3)	Indirect, indexed, extended
FF20BF FF2080	Program memory (Note 3); (After reset, the first instruction is fetched from FF2080H.)	Indirect, indexed, extended
FF207F FF2000	Special-purpose memory (CCBs, interrupt vectors, PTS vectors; Note 3)	Indirect, indexed, extended
FF1FFF FF1000	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
FF0FFF FF0400	Internal code/data RAM (identically mapped from page 00H)	Indirect, indexed, extended
FF03FF FF0000	Reserved for in-circuit emulators	—
FEFFFF 1F0000	Overlaid memory (reserved for future devices); locations *x*F0000–*x*F03FFH are reserved for in-circuit emulators	Indirect, indexed, extended
1EFFFF 004000	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
003FFF 002400	A copy of internal ROM (FF2400–FF3FFFH) if CCB1.2=0 External memory if CCB1.2=1	Indirect, indexed, extended
0023FF 002000	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
001FFF 001FE0	Memory-mapped special-function registers (SFRs)	Indirect, indexed, extended
001FDF 001C00	Peripheral special-function registers (SFRs)	Indirect, indexed, extended, windowed direct
001BFF 001000	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
000FFF 000400	Internal code/data RAM (identically mapped into page FFH)	Indirect, indexed, extended
0003FF 000100	Upper register file (general-purpose register RAM)	Indirect, indexed, windowed direct
0000FF 00001A	Lower register file (general-purpose register RAM)	Direct, indirect, indexed
000019 000000	Lower register file (stack pointer and CPU SFRs)	Direct, indirect, indexed

NOTES:
1. Unless otherwise noted, write 0FFH to reserved memory locations and write 0 to reserved SFR bits.
2. The contents or functions of reserved locations may change in future device revisions, in which case a program that relies on one or more of these locations might not function properly.
3. External memory if EA# is low; internal ROM if EA# is high.

6.0 Electrical Characteristics

Absolute Maximum Ratings†

Storage Temperature . . . . . –60°C to +150°C
Supply Voltage with Respect to V_{SS} . . . . . –0.5 V to +7.0 V
Power Dissipation . . . . . 1.5 W

Operating Conditions†

T_C (Case Temperature Under Bias) . . . . . –40°C to +125°C
V_{CC} (Digital Supply Voltage) . . . . . 4.5 V to 5.5 V
V_{REF} (Analog Supply Voltage) . . . . . 4.5 V to 5.5 V
F_{XTAL1}
(Input frequency for V_{CC} = 4.5 V – 5.5 V)
(Note 1) . . . . . 20 MHz to 40 MHz

Notice: This document contains information on products in the design phase of development. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

†**Warning**: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTE:
1. This device is static and should operate below 1 Hz, but has been tested only down to 20 MHz.

6.1 DC Characteristics

Table 6. DC Characteristics at V_{CC} = 4.5 V – 5.5 V (Sheet 1 of 2)

Symbol	Parameter	Min	Typical (Note 1)	Max	Units	Test Conditions
I_{CC}	V_{CC} supply current		120	140	mA	XTAL1 = 40 MHz V_{CC} = 5.5 V Device in Reset
I_{IDLE}	Idle mode current		60	100	mA	XTAL1 = 40 MHz V_{CC} = 5.5 V
I_{PD}	Powerdown mode current		50		µA	V_{CC} = 5.5 V
I_{REF}	A/D reference supply current			5	mA	XTAL1 = 40 MHz V_{CC} = V_{REF}= 5.5 V Device in Reset
I_{CRVCC}	Code RAM V_{CC} Supply Current			110	µA	V_{CC}=5.5 V
I_{INJD}	Maximum injection current per port on bidirectional pins (Note 4)	–10		10	mA	
I_{LI}	Input leakage current (Standard inputs except analog inputs)	–10		10	µA	V_{SS} < V_{IN} < V_{CC}
I_{LI1}	Input leakage current (analog inputs)	–300		300	nA	V_{SS} + 100 mV < V_{IN} < V_{REF} – 100 mV

NOTES:
1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0 V.
2. For P2.7:0, P3.7:0, P4.7:0, P5.7:0, P6.7:0, P10.3:0, P11.7:0, P12.4:0, AD15:0, EA#, RESET#, PLLEN, NMI, TDI, TCLK, ONCE#, and XTAL1.
3. For P7.7:0, P8.7:0, P9.7:0, and P10.5:4.
4. The maximum injection current is not tested. The device is designed to meet this specification.
5. Pin capacitance is not tested. This value is based on design simulations.

Table 6. DC Characteristics at V_{CC} = 4.5 V – 5.5 V (Sheet 2 of 2)

Symbol	Parameter	Min	Typical (Note 1)	Max	Units	Test Conditions
I_{IH}	Input high current (NMI only)			175	µA	NMI = V_{CC} = 5.5 V
V_{IL1}	Input low voltage (Note 2)	–0.5		0.3 V_{CC}	V	
V_{IH1}	Input high voltage (Note 2)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{IL2}	Input low voltage (Note 3)	–0.5		0.4 V_{CC}	V	
V_{IH2}	Input high voltage (Note 3)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL1}	Output low voltage (output configured as complementary)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH1}	Output high voltage (output configured as complementary)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V V V	I_{OH} = –200 µA I_{OH} = –3.2 mA I_{OH} = –7.0 mA
V_{OL2}	Output low voltage in reset			0.5	V	I_{OL} = 15 µA
I_{OH2}	Output high current in reset	–30 –65 –75		–120 –240 –280	µA µA µA	V_{OH2} = V_{CC} – 1.0V V_{OH2} = V_{CC} – 2.5V V_{OH2} = V_{CC} – 4.0V
I_{OH3}	Output high current in reset on Port 11	-5 -8 -10		–50 –110 –130	µA µA µA	V_{OH3} = V_{CC} – 1.0V V_{OH3} = V_{CC} – 2.5V V_{OH3} = V_{CC} – 4.0V
V_{OH2}	Output high voltage in reset	V_{CC} – 1			V	I_{OH} = –15 µA
V_{HYS}	Hysteresis voltage on all inputs except XTAL1	700			mV	
C_S	Pin Capacitance (any pin to V_{SS}) (Note 5)			10	pF	
R_{RST}	Pull-up resistor on RESET# pin	9		95	kΩ	V_{CC} = 5.5 V, V_{IN} = 4.0 V

NOTES:
1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0 V.
2. For P2.7:0, P3.7:0, P4.7:0, P5.7:0, P6.7:0, P10.3:0, P11.7:0, P12.4:0, AD15:0, EA#, RESET#, PLLEN, NMI, TDI, TCLK, ONCE#, and XTAL1.
3. For P7.7:0, P8.7:0, P9.7:0, and P10.5:4.
4. The maximum injection current is not tested. The device is designed to meet this specification.
5. Pin capacitance is not tested. This value is based on design simulations.

6.2 AC Characteristics — Multiplexed Bus Mode

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 7. AC Characteristics, Multiplexed Bus Mode (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	Frequency on XTAL1, PLL in 1x mode	20	40	MHz (1, 8)
	Frequency on XTAL1, PLL in 2x mode	10	20	MHz (8)
f	Operating frequency, f = F_{XTAL1}; PLL in 1x mode	20	40	MHz (8)
	Operating frequency, f = $2F_{XTAL1}$; PLL in 2x mode			
t	Period, t = 1/f	25	50	ns
T_{AVDV}	Address Valid to Input Data Valid		3t – 40	ns (2)
T_{RLDV}	RD# Low to Input Data Valid		t – 23	ns (2)
T_{CHDV}	CLKOUT High to Input Data valid		2t – 35	ns (9)
T_{RHDZ}	RD# High to Input Data Float		t + 5	ns
T_{RXDX}	Data Hold after RD# Inactive	0		ns
T_{XHCH}	XTAL1 Rising Edge to CLKOUT High or Low	3	50	ns (9)
T_{CLCL}	CLKOUT Cycle Time	2t		ns (9)
T_{CHCL}	CLKOUT High Period	t – 10	t + 10	ns (9)
T_{CLLH}	CLKOUT Falling to ALE Rising	– 10	10	ns (9)
T_{LLCH}	ALE Falling to CLKOUT Rising	– 10	10	ns (9)
T_{LHLH}	ALE Cycle Time	4t		ns (2)
T_{LHLL}	ALE High Period	t – 10	t + 10	ns
T_{AVLL}	Address Setup to ALE Low	t – 15		ns
T_{LLAX}	Address Hold after ALE Low	t – 16		ns
T_{LLRL}	ALE Low to RD# Low	t – 15		ns
T_{RLCL}	RD# Low to CLKOUT Low	– 10	10	ns (9)
T_{RLRH}	RD# Low to RD# High	t – 12		ns (2)
T_{RHLH}	RD# High to ALE Rising	t – 5	t + 15	ns (3)
T_{RLAZ}	RD# Low to Address Float		7	ns
T_{LLWL}	ALE Low to WR# Low	t – 12		ns
T_{QVWH}	Data Stable to WR# Rising Edge	t – 15		ns (2)

NOTES:
1. 20 MHz is the maximum input frequency when using an external crystal oscillator; however, 40 MHz can be applied with an external clock source.
2. If wait states are used, add 2t × *n*, where *n* = number of wait states.
3. Assuming back-to-back bus cycles.
4. When forcing wait states using the BUSCON register, add 2t × *n*.
5. Exceeding the maximum specification causes additional wait states.
6. 8-bit bus only.
7. The first falling edge of READY is not synchronized to a CLKOUT edge; therefore, one programmed wait state is required.
8. Device is static by design but has been tested only down to 20 MHz.
9. Assumes CLKOUT is operating in divide-by-two mode (f/2).

Table 7. AC Characteristics, Multiplexed Bus Mode (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units
T_{CHWH}	CLKOUT High to WR# Rising Edge	– 10	10	ns (9)
T_{WLWH}	WR# Low to WR# High	t – 10		ns (2)
T_{WHQX}	Data Hold after WR# High	t – 16		ns
T_{WHLH}	WR# High to ALE High	t – 15	t + 10	ns
T_{WHBX}	BHE#, INST Hold after WR# High	t – 4		ns
T_{WHAX}	AD15:8, CS*x*# Hold after WR# High	t – 4		ns (6)
T_{RHBX}	BHE#, INST Hold after RD# High	t – 5		ns
T_{RHAX}	AD15:8, CS*x*# Hold after RD# High	t – 5		ns (6)
T_{WHSH}	A20:0, CS*x*# Hold after WR# High	0		ns
T_{RHSH}	A20:0, CS*x*# Hold after RD# High	0		ns
T_{AVYV}	AD15:0 Valid to READY Setup		2t – 40	ns (4)
T_{CLYX}	READY Hold after CLKOUT Low	0	2t – 40	ns (5, 7, 9)
T_{YLYH}	Non-READY Time	No Upper Limit		ns

NOTES:
1. 20 MHz is the maximum input frequency when using an external crystal oscillator; however, 40 MHz can be applied with an external clock source.
2. If wait states are used, add 2t × *n*, where *n* = number of wait states.
3. Assuming back-to-back bus cycles.
4. When forcing wait states using the BUSCON register, add 2t × *n*.
5. Exceeding the maximum specification causes additional wait states.
6. 8-bit bus only.
7. The first falling edge of READY is not synchronized to a CLKOUT edge; therefore, one programmed wait state is required.
8. Device is static by design but has been tested only down to 20 MHz.
9. Assumes CLKOUT is operating in divide-by-two mode (f/2).

Table 8. AC Timing Symbol Definitions

Signals						Conditions	
A†	Address	L	ALE	W	WR#, WRH#, WRL#	H	High
B	BHE#	Q	Output Data	X	XTAL1	L	Low
C	CLKOUT	R	RD#	Y	READY	V	Valid
D	Input Data	S	CS*x*#			X	No Longer Valid
						Z	Floating

† Address bus (demultiplexed mode) or address/data bus (multiplexed mode)

Figure 4. System Bus Timing Diagram (Multiplexed Bus Mode)

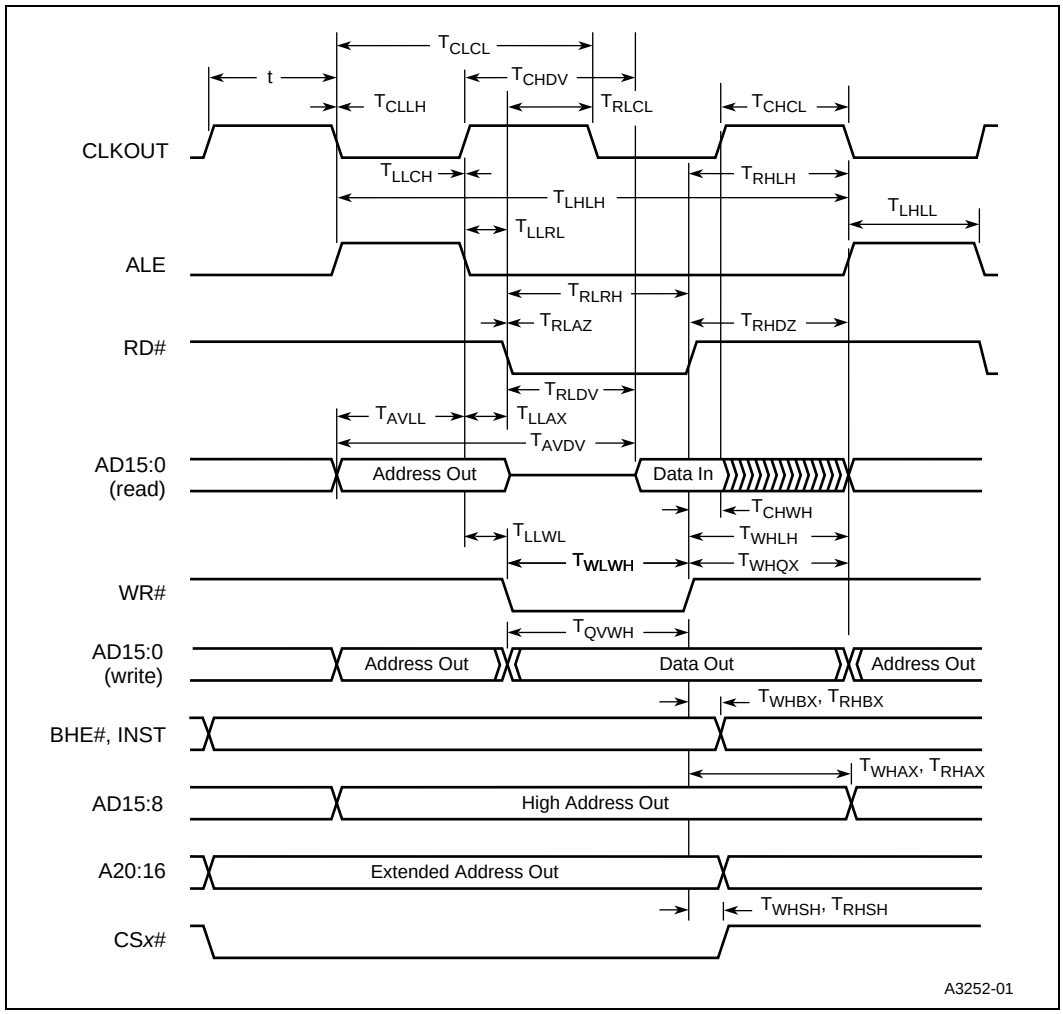
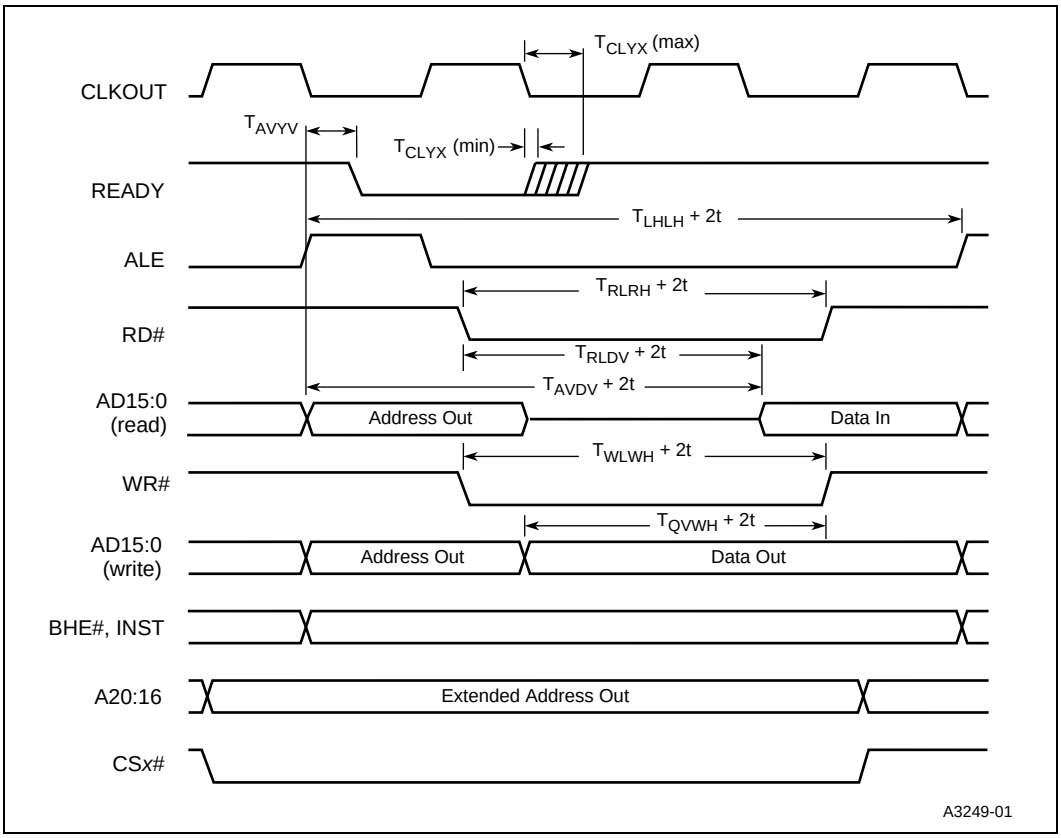


Figure 5. READY Timing Diagram (Multiplexed Bus Mode)



6.3 AC Characteristics — Demultiplexed Bus Mode

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 9. AC Characteristics, Demultiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	Frequency on XTAL1, PLL in 1x mode	20	40	MHz (1,8)
	Frequency on XTAL1, PLL in 2x mode	10	20	MHz (8)
f	Operating frequency, f = F_{XTAL1}; PLL in 1x mode	20	40	Mhz
	Operating frequency, f = $2F_{XTAL1}$; PLL in 2x mode			
t	Period, t = 1/f	25	50	ns
T_{AVDV}	Address Valid to Input Data Valid		4t – 23	ns (2)
T_{RLDV}	RD# Low to Input Data Valid		3t – 25	ns (2)
T_{AVWL}	Address Valid to WR# Low	t		ns
T_{AVRL}	Address Valid to RD# Low	t – 8		ns
T_{SLDV}	Chip Select Low to Data Valid		4t – 27	ns (2)
T_{CHDV}	CLKOUT Rising Edge to Input Data Valid		2t – 25	ns (9)
T_{RHDZ}	RD# High to Input Data Float		t - 5	ns
T_{RHRL}	Read High to Next Read Low	t – 5		ns
T_{RXDX}	Data Hold after RD# Inactive	0		ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	10	35	ns (9)
T_{CLCL}	CLKOUT Cycle Time	2t		ns (9)
T_{CHCL}	CLKOUT High Period	t – 10	t + 10	ns (9)
T_{CLLH}	CLKOUT Falling ALE Rising	– 10	10	ns (9)
T_{RLCL}	RD# Low to CLKOUT Low	– 5	5	ns (9)
T_{RLRH}	RD# Low to RD# High	3t – 12		ns (2)
T_{RHLH}	RD# Rising to ALE Rising	t – 4	t + 12	ns (3)
T_{WLCL}	WR# Low to CLKOUT Falling	– 13	5	ns (9)
T_{QVWH}	Data Stable to WR# Rising Edge	3t – 18		ns (3)
T_{CHWH}	CLKOUT High to WR# Rising Edge	– 5	10	ns (9)
T_{WLWH}	WR# Low to WR# High	3t – 15		ns (2)
T_{WHQX}	Data Hold after WR# Rising Edge	t	t + 15	ns
T_{WHBX}	BHE#, INST Hold after WR# High	t		ns
T_{WHAX}	A20:0, CS*x*# Hold after WR# High	0		ns
T_{RHBX}	BHE#, INST Hold after RD# High	t		ns
T_{RHAX}	A20:0, CS*x*# Hold after RD# High	0		ns
T_{AVYV}	A20:0 Valid to READY Setup		3t – 25	ns (4)
T_{CLYX}	READY Hold after CLKOUT Low	0	2t – 28	ns (5, 7,9)
T_{YLYH}	Non READY Time	No Upper Limit		ns

NOTES:
1. 20 MHz is the maximum input frequency when using an external crystal oscillator; however, 40 MHz can be applied with an external clock source.
2. If wait states are used, add 2t × *n*, where *n* = number of wait states.
3. Assuming back-to-back bus cycles.
4. When forcing wait states using the BUSCON register, add 2t × *n*.
5. Exceeding the maximum specification causes additional wait states.
6. 8-bit bus only.
7. The first falling edge of READY is not synchronized to a CLKOUT edge; therefore, one programmed wait state is required.
8. Device is static by design but has been tested only down to 20 MHz.
9. Assumes CLKOUT is operating in divide-by-two mode (f/2).

Figure 6. System Bus Timing Diagram (Demultiplexed Bus Mode)

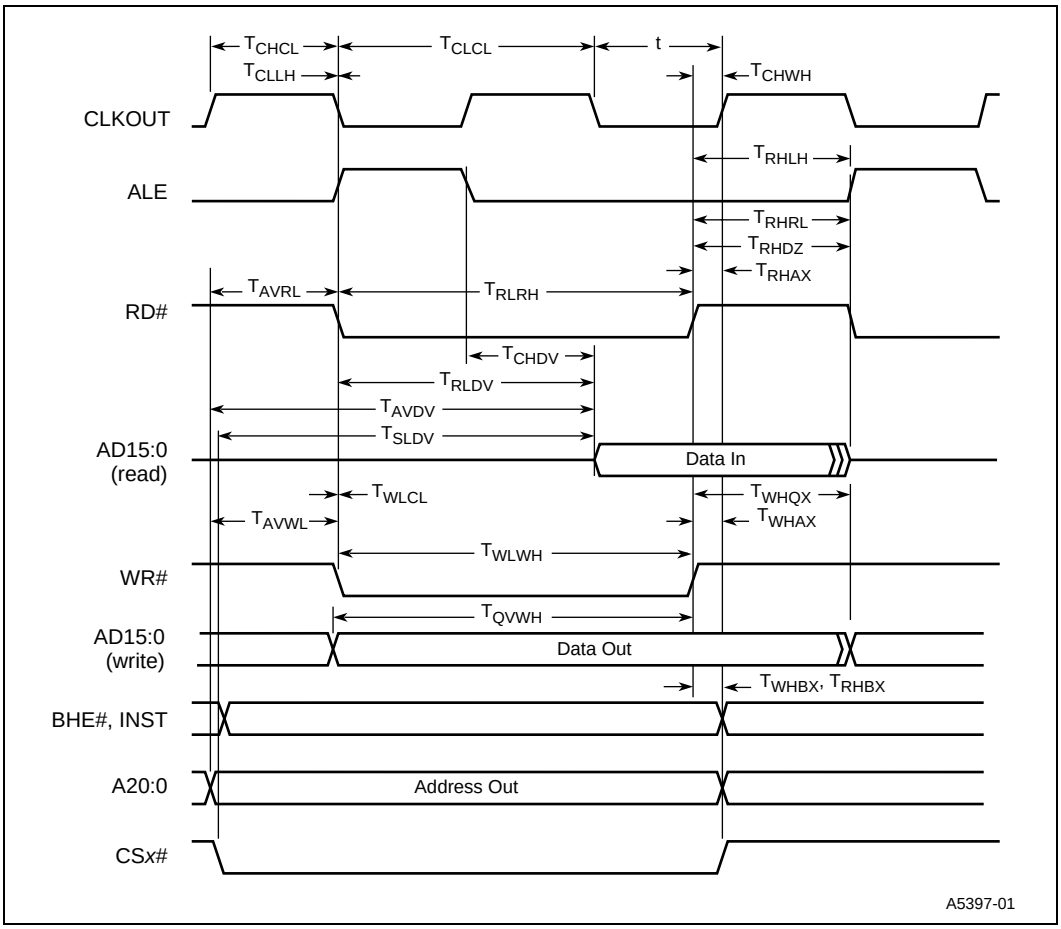
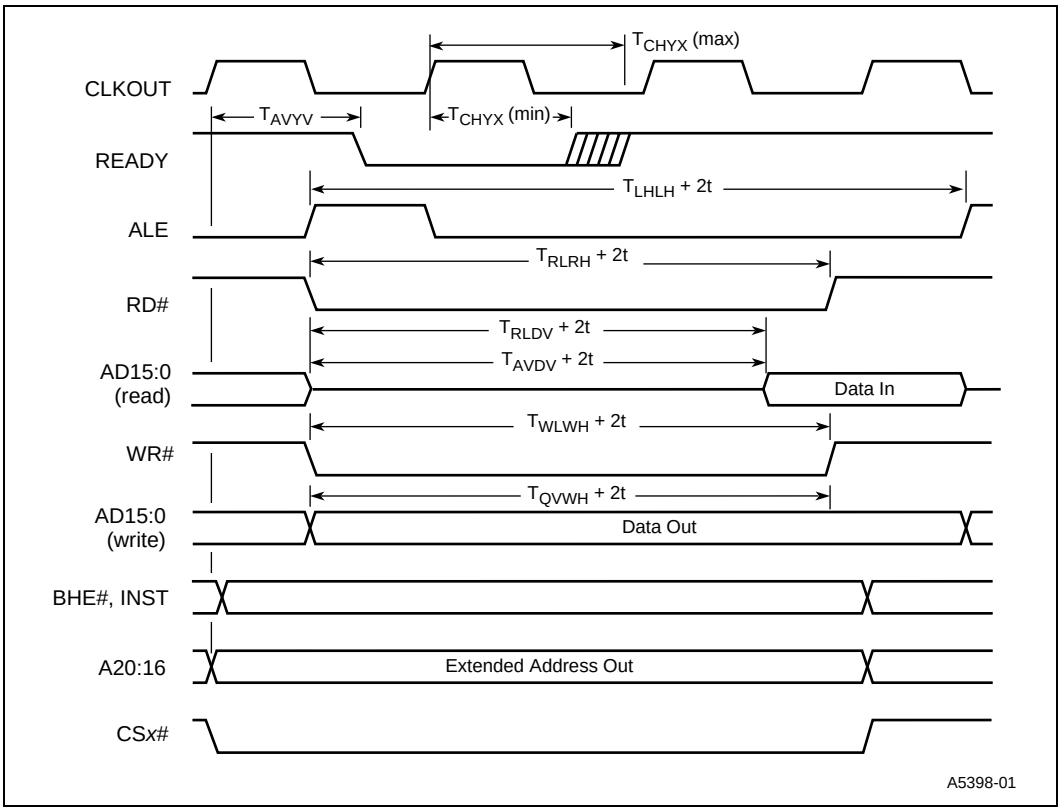


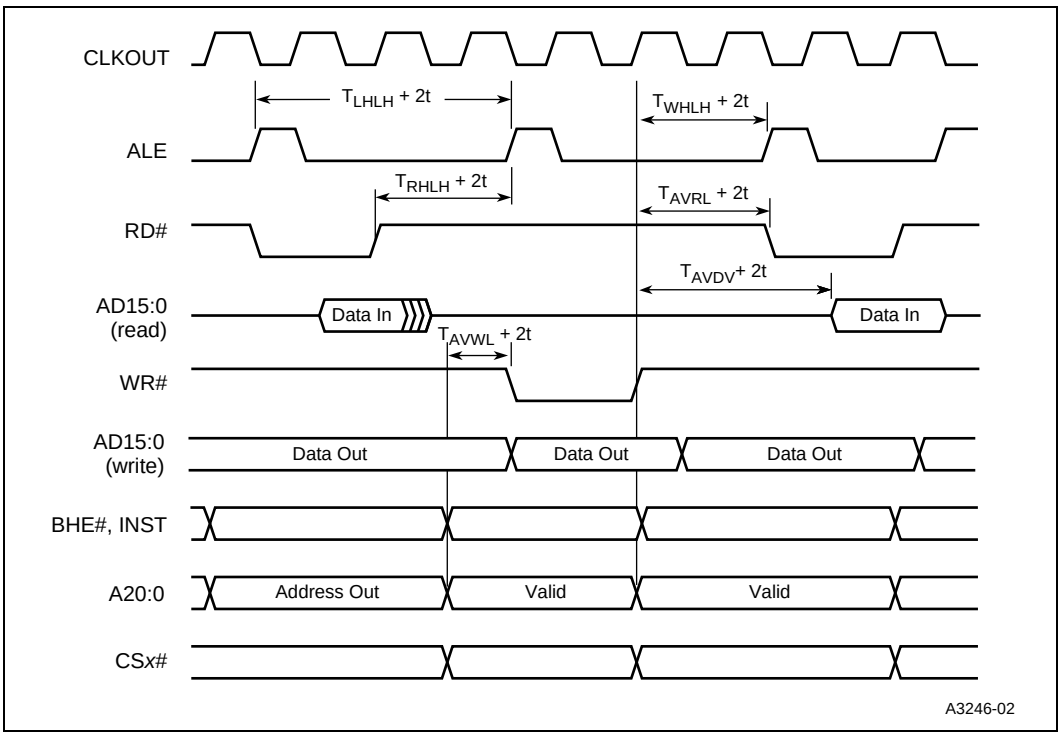
Figure 7. READY Timing Diagram (Demultiplexed Bus Mode)



6.4 Deferred Bus Timing Mode

Deferred Bus Cycle Mode: This bus mode (enabled by setting CCB1.5) reduces bus contention when using the 83C196EA in demultiplexed mode with slow memories. As shown in Figure 8, a delay of 2t occurs in the first bus cycle following a chip-select output change and the first write cycle following a read cycle.

Figure 8. Deferred Bus Mode Timing Diagram



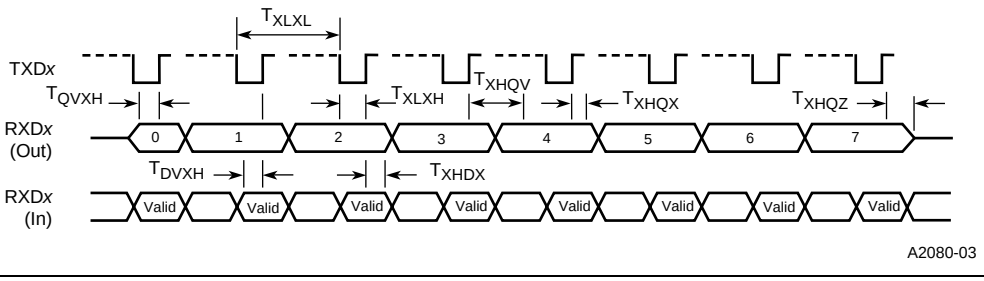
6.5 AC Characteristics — Serial Port, Shift Register Mode

Table 10. Serial Port Timing — Shift Register Mode

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock period • SP_BAUD ≥ *x*002H • SP_BAUD = *x*001H†	 6t 4t		 ns ns
T_{XLXH}	Serial Port Clock falling edge to rising edge • SP_BAUD ≥ *x*002H • SP_BAUD = *x*001H†	 4t – 27 2t – 27	 4t + 27 2t + 27	 ns ns
T_{QVXH}	Output data setup to clock high	4t – 30		ns
T_{XHQX}	Output data hold after clock high	2t – 30		ns
T_{XHQV}	Next output data valid after clock high		2t + 30	ns
T_{DVXH}	Input data setup to clock high	2t + 30		ns
T_{XHDX}	Input data hold after clock high	0		ns
T_{XHQZ}	Last clock high to output float		t + 30	ns

† The minimum baud-rate (SP_BAUD) register value for receive is *x*002H and the minimum baud-rate (SP_BAUD) register value for transmit is *x*001H.

Figure 9. Serial Port Waveform — Shift Register Mode

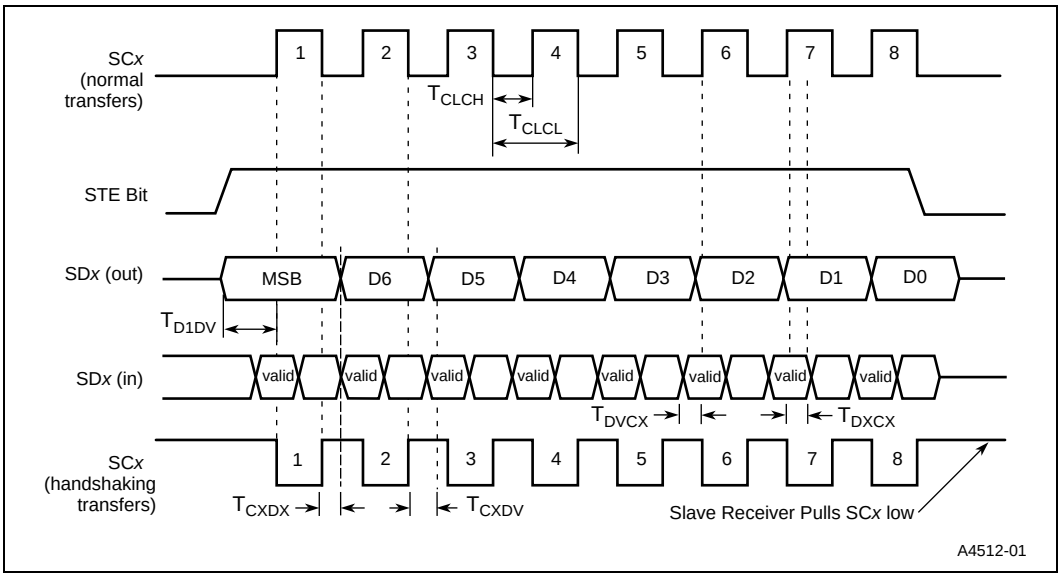


6.6 AC Characteristics — Synchronous Serial Port

Table 11. Synchronous Serial Port Timing

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Synchronous Serial Port Clock period	8t		ns
T_{CLCH}	Synchronous Serial Port Clock falling edge to rising edge	4t		ns
T_{D1DV}	Setup time for MSB output	2t		ns
T_{CXDV}	Setup time for D6:0 output		3t + 24	ns
T_{CXDX}	Output data hold after clock low	t	3t + 21	ns
T_{DVCX}	Setup time for input data	10		ns
T_{DXCX}	Input data hold after clock high	t + 5		ns

Figure 10. Synchronous Serial Port



6.7 A/D Sample and Conversion Times

Two parameters, sample time and conversion time, control the time required for an A/D conversion. The sample time is the length of time that the analog input voltage is actually connected to the sample capacitor. If this time is too short, the sample capacitor will not charge completely. If the sample time is too long, the input voltage may change and cause conversion errors. The conversion time is the length of time required to convert the analog input voltage stored on the sample capacitor to a digital value. The conversion time must be long enough for the comparator and circuitry to settle and resolve the voltage. Excessively long conversion times allow the sample capacitor to discharge, degrading accuracy.

The AD_TIME register programs the A/D sample and conversion times. Use the T_{SAM} and T_{CONV} specifications in Table 12 and Table 14 to determine appropriate values for SAM and CONV; otherwise, erroneous conversion results may occur.

When the SAM and CONV values are known, write them to the AD_TIME register. Do not write to this register while a conversion is in progress; the results are unpredictable.

Use the following formulas to determine the SAM and CONV values.

$$SAM = \frac{T_{SAM} \times f - 2}{8} \qquad CONV = \left[\frac{T_{CONV} \times f - 3}{2 \times B}\right] - 1$$

where:

SAM	equals a number, 1 to 7
CONV	equals a number, 2 to 31
T_{SAM}	is the sample time, in µsec (Table 12 and Table 14)
T_{CONV}	is the conversion time, in µsec (Table 12 and Table 14)
f	is the operating frequency, in MHz
B	is the number of bits to be converted (8 or 10)

At 40 Mhz, to meet T_{SAM} and T_{CONV} minimum specifications:

10-bit mode: $SAM = [5, 6, 7] \Rightarrow T_{SAM} \geq 1\mu s$

$ONV = [18, 19, 20, \ldots, 31] \Rightarrow T_{CONV} \geq 10\mu s$

8-bit mode: $SAM = [5, 6, 7] \Rightarrow T_{SAM} \geq 1\mu s$

$ONV = [23, 24, \ldots, 31] \Rightarrow T_{CONV} \geq 10\mu s$

6.7.1 AC Characteristics — A/D Converter, 10-bit Mode

Table 12. 10-bit A/D Operating Conditions (1)

Symbol	Description	Min	Max	Units	Notes
T_C	Case Temperature	– 40	+ 125	°C	
V_{CC}	Digital Supply Voltage	4.50	5.50	V	
V_{REF}	Analog Supply Voltage	4.50	5.50	V	2
T_{SAM}	Sample Time	1.0		µs	3
T_{CONV}	Conversion Time	10.0	15.0	µs	3

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than + 0.5 V because V_{REF} supplies both the resistor ladder and the analog portion of the converter and input port pins.
3. Program the AD_TIME register to meet the T_{SAM} and T_{CONV} specifications.

Table 13. 10-bit Mode A/D Characteristics Over Specified Operating Conditions (7)

Parameter	Typical (2)	Min	Max	Units (1)	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	± 3.0	LSBs	
Full-scale Error	0.25 ± 0.5			LSBs	
Zero Offset Error	0.25 ± 0.5			LSBs	
Nonlinearity	1.0 ± 2.0		± 3.0	LSBs	
Differential Nonlinearity		– 0.75	+ 0.75	LSBs	
Channel-to-channel Matching	± 0.1	0	± 1.0	LSBs	
Repeatability	± 0.25	0		LSBs	
Temperature Coefficients: • Offset • Full-scale • Differential Nonlinearity	 0.009 0.009 0.009			 LSB/C LSB/C LSB/C	
Off-isolation		– 60		dB	2, 3, 4
Feedthrough	– 60			dB	2, 3
V_{CC} Power Supply Rejection	– 60			dB	2, 3
Input Series Resistance		750	1.2K	W	5
Voltage on Analog Input Pin		ANGND	V_{REF}	V	6
Sampling Capacitor	3.0			pF	
DC Input Leakage	± 100	– 300	300	nA	8

NOTES:
1. An *LSB*, as used here, has a value of approximately 5 mV.
2. Most parts will meet these values at 25°C, but they are not tested or guaranteed.
3. DC to 100 KHz.
4. Multiplexer break-before-make guaranteed.
5. Resistance from device pin, through internal multiplexer, to sample capacitor.
6. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions were performed with processor in idle mode.
8. 100 mV < V_{IN} < V_{REF} – 100 mV.

6.7.2 AC Characteristics — A/D Converter, 8-bit Mode

Table 14. 8-bit A/D Operating Conditions (1)

Symbol	Description	Min	Max	Units	Notes
T_C	Case Temperature	– 40	+ 125	°C	
v_{CC}	Digital Supply Voltage	4.50	5.50	V	
v_{REF}	Analog Supply Voltage	4.50	5.50	V	2
T_{SAM}	Sample Time	1.0		µs	3
T_{CONV}	Conversion Time	8.0	12.8	µs	3

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than + 0.5 V because V_{REF} supplies both the resistor ladder and the analog portion of the converter and input port pins.
3. Program the AD_TIME register to meet the T_{SAM} and T_{CONV} specifications.

Table 15. 8-bit Mode A/D Characteristics Over Specified Operating Conditions (7)

Parameter	Typical (2)	Min	Max	Units (1)	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	± 1.0	LSBs	
Full-scale Error	± 0.5			LSBs	
Zero Offset Error	± 0.5			LSBs	
Nonlinearity		0	± 1.0	LSBs	
Differential Nonlinearity		– 0.5	+ 0.5	LSBs	
Channel-to-channel Matching		0	± 1.0	LSBs	
Repeatability	± 0.25	0		LSBs	
Temperature Coefficients: Offset Full-scale Differential Nonlinearity	 0.003 0.003 0.003			 LSB/°C LSB/°C LSB/°C	
Off Isolation		– 60		dB	2, 3, 4
Feedthrough	– 60			dB	2, 3
V_{CC} Power Supply Rejection	– 60			dB	2, 3
Input Series Resistance		750	1.2K	Ω	5
Voltage on Analog Input Pin		ANGND	V_{REF}	V	6
Sampling Capacitor	3.0			pF	
DC Input Leakage	±100	– 300	300	nA	8

NOTES:
1. An *LSB*, as used here, has a value of approximately 20 mV.
2. Most parts will need these values at 25°C, but they are not tested or guaranteed.
3. DC to 100 KHz.
4. Multiplexer break-before-make guaranteed.
5. Resistance from device pin, through internal multiplexer, to sample capacitor.
6. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions were performed with processor in idle mode.
8. 100 mV < V_{IN} < V_{REF} – 100 mV.

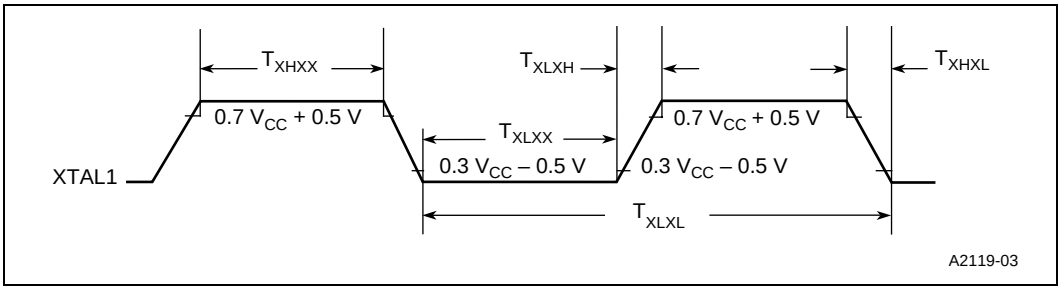
6.8 External Clock Drive

Table 16. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency (F_{XTAL1})	10	40 (1)	MHz (2)
T_{XLXL}	Oscillator Period (T_{XTAL1})	25	100	ns
T_{XHXX}	High Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXX}	Low Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

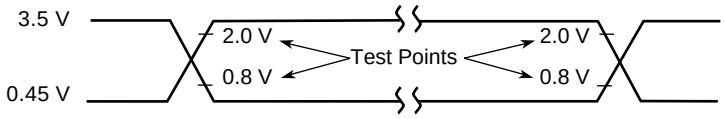
NOTES:
1. 20 MHz is the maximum input frequency when using an external crystal oscillator; however, 40 MHz can be applied with an external clock source.
2. These values represent PLL-bypass mode.

Figure 11. External Clock Drive Waveforms



6.9 Test Output Waveforms

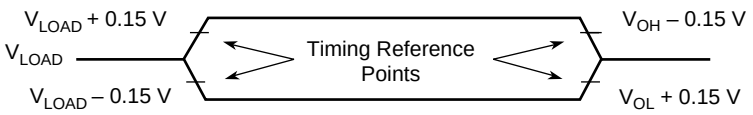
Figure 12. AC Testing Output Waveforms



Note:
AC testing inputs are driven at 3.5 V for a logic " 1" and 0.45 V for a logic " 0" . Timing measurements are made at 2.0 V for a logic " 1" and 0.8 V for a logic " 0".

A2120-04

Figure 13. Float Waveforms During 5.0 Volt Testing



Note:
For timing purposes, a port pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} \leq 15$ mA.

A2121-03

7.0 Thermal Characteristics

All thermal impedance data is approximate for static air conditions at 1 W of power dissipation. Values change depending on operating conditions and the application. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology. The *Components Quality and Reliability Handbook* (order number 210997) provides quality and reliability information.

Table 17. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
160-pin QFP	34°C/W	5°C/W

7.1 83C196EA Errata

The 83C196EA may contain design defects or errors known as errata. Characterized errata that may cause the 83C196EA's behavior to deviate from published specifications are documented in a specification update. Specification updates can be obtained from your local Intel sales office or from the World Wide Web (*www.intel.com*).

8.0 Datasheet Revision History

This datasheet is valid for devices with an “C” at the end of the topside field process order (FPO) number. Datasheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

This is the -004 version of the datasheet. The following changes were made in this version:

Table 18. Revision History (rev. 005 - 006)

Item	Description
Data Sheet	Formatted into new template.
Table 5 on page 18	Hex Address (cell #3): Changed FF2200 to FF2140. Hex Address (cell #4): Changed FF21FF to FF213F.
Table 11 on page 30	T_{CXDX} - Max: Changed 3t+20 to 3t+21.
Table 14 on page 33	T_{CONV} - Max: Changed 15.0 to 12.8.

Table 19. Revision History (rev. 004 - 005)

Item	Description
Table 1 on page 6	Program Memory Option: Removed option O — cpu only - no internal ROM

Table 20. Revision History (rev. 003 - 004)

Item	Description
Data Sheet	Removed all referances to 80C196EA.
Table 6 on page 19	I_{CC} - Max: Changed 135 to 140. I_{IDLE} - Max: Changed 95 to 100.
Table 7 on page 21	T_{RLDV} - Max: Changed t-18 to t-23. T_{LLAX} - Min: Changed t-15 to t-16. T_{RLAZ} - Max: Changed 5 to 7. T_{QVWH} - Min: Changed t-14 to t-15. T_{WHQX} - Min: Changed t-20 to t-16.
Table 9 on page 25	T_{WLCL} - Min: Changed -12 to -13.
Table 11 on page 30	T_{CXDV} - Max: Changed 3t+20 to 3t+24.
Table 21 on page 38	Corrected I_{HO2} and I_{HO3} to I_{OH2} and I_{OH3}.

Table 21. Revision History (rev. 002 - 003) (Sheet 1 of 2)

Item	Description
Data Sheet	Added 80C196EA device to heading. All device references changed to 83C196EA.
Figure 1 on page 5	Revised drawing to reflect “83C196EA”.
Table 4 on page 11	A15:0 - Type - Changed “I/O” to “O” only. AD15:0 - Description - 8-bit Demultiplexed Mode: Added last paragraph “AD7:0 share package pins P3.7:0. AD15:8 share package pins P4.7:0.” CRIN - Description: Changed “byte” to “bit”. CROUT - Description: Changed “byte” to “bit”. ONCE# - Description - 1st paragraph: Added second sentence “PLLEN must also be held low.” PLLEN - Description: Added last paragraph “This pin must be held low when entering on-circuit emulation (ONCE) mode.” T1CLK - Description: Removed sentence “External clock for the serial I/O baud-rate generator input (program selectable).” T2CLK - Description: Added sentence “External clock for the serial I/O baud-rate generator input (program selectable).” XTAL1 - Description: Corrected spelling “sourcel” to “source”.
Table 6 on page 19	I_{PD}: • Typical: Changed “20” to “50” • Max: Changed “50” to “blank” I_{REF} - Max: Changed TBD to “5”. I_{CRVCC} - Added row. $I_{OH2:}$ • Min: Changed $V_{OH2}=V_{CC}$-2.5 V to “-65”, $V_{OH2}=V_{CC}$-4.0 V to “-75” • Units: Changed all from “mA” to “µA” I_{OH3}: • Parameter: Changed “Port 12”to “Port 11” • Min: Changed $V_{OH3}=V_{CC}$-1.0 V to “-5”, $V_{OH3}=V_{CC}$-2.5 V to “-8”, $V_{OH3}=V_{CC}$-4.0 V to “-10” • Units: Changed all from “mA” to “µA”.
Table 7 on page 21	F_{XTAL1} - Min: • 1x mode changed from “15” to “20” • 2x mode changed from “8” to “10” f - Min: Changed from “15” to “20”. t - Max: Changed from “62.5” to “50”. T_{RLRH} - Min: Changed from “t-10” to “t-12”. T_{CHWH} - Max: Changed from “5” to “10”. T_{WHQX} - Min: Changed from “t-15” to “t-20”. Note 1: “16 MHz” changed to “20 MHz”.
Table 9 on page 25	F_{XTAL1} - Min: • 1x mode changed from “15” to “20” • 2x mode changed from “8” to “10” f - Min: Changed from “15” to “20”. t - Max: Changed from “62.5” to “50”. T_{CHCL} - Min: Changed from “t-5” to “t-10”; Max: Changed from “t+5” to “t+10”. T_{CLLH} - Min: Changed from “-5” to “-10”; Max: Changed from “5” to “10”. T_{RLRH} - Min: Changed from “3t-10” to “3t-12”. T_{WLWH} - Min: Changed from “3t-12” to “3t-15”. T_{AVYV} - Max: Changed from “3t-23” to “3t-25”. Note 1: “16 MHz” changed to “20 MHz”.

Table 21. Revision History (rev. 002 - 003) (Sheet 2 of 2)

Item	Description
Table 11 on page 30	T_{D1DV} - Symbol: Changed T_{D1VD}" to "T_{D1DV}". T_{D1DV} - Min: Changed TBD to "2t".
Figure 10 on page 30	Revised figure.
Table 13 on page 32	DC Input Leakage • Min - Changed "0" to "-300" • Max - Removed "±" from "300" Note 2: Changed "need" to "meet".
Table 15 on page 33	DC Input Leakage: • Typical: Added "±" to "100" • Min: Changed "0" to "-300"
Table 16 on page 34	$1/T_{XLXL}$ - Min: Changed "8" to "10". T_{XLXL}: • Min: Changed "50" to "25" • Max: Changed "125" to "100" Note 1: • Changed "16 MHz" to "20 MHz" • Changed "32 MHz" to "40 MHz"

Table 22. Revision History (rev. 001 - 002)

Item	Description
Data Sheet	Status changed from “Product Preview” to “Advance Information”.
Cover	The frequency designation was changed from 32 MHz to 40 MHz.
“DC Characteristics” on page 19	The following DC characteristics specifications were either changed or added: • I_{CC} (max) • I_{IDLE} (max) • I_{OH2} • I_{OH3}
“AC Characteristics — Multiplexed Bus Mode” on page 21	The following AC characteristics **multiplexed** bus mode specifications were changed: • T_{CHCL} (max) • T_{LLCH} (min/max) • T_{RLCL} (max) • T_{CHWH} (min) • T_{WHLH} (max) • T_{AVYV} (max) • T_{CLYX} (max) • T_{WHQX} (min) • T_{LLAX} (min) • T_{RLDV} (max)
“AC Characteristics — Demultiplexed Bus Mode” on page 25	The following AC characteristics **demultiplexed** bus mode specifications were changed: • T_{AVDV} (max) • T_{RLDV} (max) • T_{SLDV} (max) • T_{CHDV} (max) • T_{XHCH} min/(max) • T_{CHCL} (min/max) • T_{CLLH} (min/max) • T_{RLCL} (min) • T_{RLRH} (min) • T_{RHLH} (max) • T_{WLCL} (min) • T_{QVWH} (min) • T_{CHWH} (min) • T_{WLWH} (min) • T_{WHQX} (max) • T_{WHBX} (min) • T_{RHBX} (min) • T_{AVYV} (max) • T_{CLYX} (max)
“AC Characteristics — Demultiplexed Bus Mode” on page 25	The following AC characteristics **demultiplexed** bus mode specifications were removed: • T_{LLCH} • T_{LHLH} • T_{LHLL} • T_{WHLH}
Figure 6 on page 26	Address out line in the System Bus Timing Diagram (Demultiplexed Bus Mode) was corrected from A20:16 to A20:0.
Figure 5 on page 24	T_{CHYX} (max) timing was corrected in the Ready Timing Diagram to show the rising edge of READY after the falling edge of CLKOUT.
HOLD#/HLDA# Timings	Section was removed, and all references to either HOLD# or HLDA# were removed.
Table 11 on page 30	Synchronous Serial timing specifications changed in table.
“A/D Sample and Conversion Times” on page 31	A/D sample and conversion times example added.
Table 15 on page 33	Note 1 of the 8-bit mode A/D characteristics table changed to state 20 mV, instead of 5 mV.

Table 23. Revision History (rev. 001)

Item	Description
Table 17	Package thermal characteristics changed.