



CY7C107B CY7C1007B

1M x 1 Static RAM

Features

- **High speed**
— $t_{AA} = 12 \text{ ns}$
- **CMOS for optimum speed/power**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

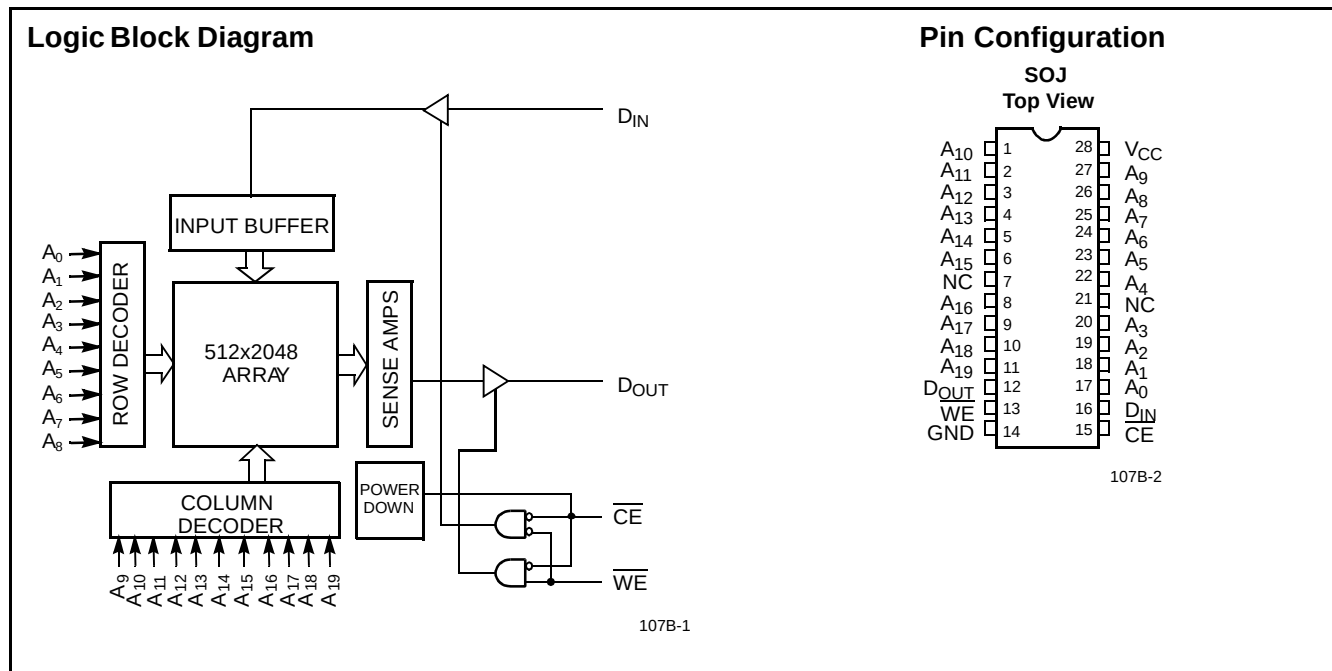
The CY7C107B and CY7C1007B are high-performance CMOS static RAMs organized as 1,048,576 words by 1 bit. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and three-state drivers. These devices have an automatic power-down feature that reduces power consumption by more than 65% when deselected.

Writing to the devices is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{19}).

Reading from the devices is accomplished by taking Chip Enable ($\overline{CE}$) LOW while Write Enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the data output (D_{OUT}) pin.

The output pin (D_{OUT}) is placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH) or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

The CY7C107B is available in a standard 400-mil-wide SOJ; the CY7C1007B is available in a standard 300-mil-wide SOJ.



Selection Guide

	7C107B-12 7C1007B-12	7C107B-15 7C1007B-15	7C107B-20 7C1007B-20	7C107B-25 7C1007B-25	7C107B-35 7C1007B-35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	90	80	75	70	60
Maximum CMOS Standby Current SB2 (mA)	2	2	2	2	2



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied..... -55°C to +125°C

Supply Voltage on V_{CC} Relative to GND^[1] -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to +70°C	5V $\pm$ 10%
Industrial	-40°C to +85°C	5V $\pm$ 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C107B-12 7C1007B-12		7C107B-15 7C1007B-15		7C107B-20 7C1007B-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-5	+5	-5	+5	-5	+5	μA
I_{OS}	Output Short Circuit Current ^[3]	$V_{CC} = \text{Max.}, V_{OUT} = GND$		-300		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.},$ $I_{OUT} = 0 \text{ mA},$ $f = f_{MAX} = 1/t_{RC}$		90		80		75	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$		20		20		20	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V, f = 0$		2		2		2	mA

Notes:

1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
2. T_A is the "Instant On" case temperature.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	7C107B-25 7C1007B-25		7C107B-35 7C1007B-35		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-5	+5	-5	+5	μA
I_{OS}	Output Short Circuit Current ^[3]	$V_{CC} = \text{Max.}, V_{OUT} = GND$		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.},$ $I_{OUT} = 0 \text{ mA},$ $f = f_{MAX} = 1/t_{RC}$		70		60	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$		20		20	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3\text{V}$, $V_{IN} \geq V_{CC} - 0.3\text{V}$ or $V_{IN} \leq 0.3\text{V}, f = 0$		2		2	mA

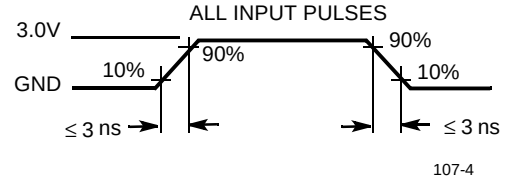
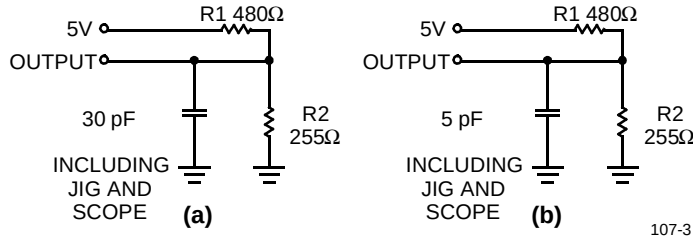
Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN} : Addresses	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz},$ $V_{CC} = 5.0\text{V}$	7	pF
C_{IN} : Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

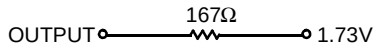
Note:

4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics^[5] Over the Operating Range

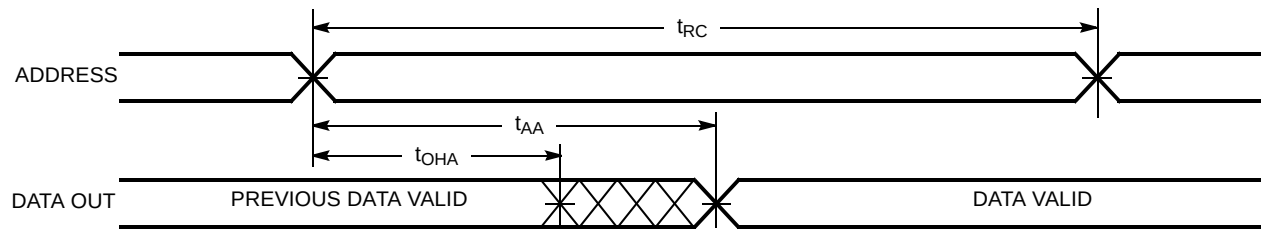
Parameter	Description	7C107B-12 7C1007B-12		7C107B-15 7C1007B-15		7C107B-20 7C1007B-20		7C107B-25 7C1007B-25		7C107B-35 7C1007B-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	12		15		20		25		35		ns
t _{AA}	Address to Data Valid		12		15		20		25		35	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[6]	3		3		3		3		3		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[6, 7]		6		7		8		10		10	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE ^[8]												
t _{WC}	Write Cycle Time	12		15		20		25		35		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		25		ns
t _{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		25		ns
t _{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[6]	3		3		3		3		3		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[6, 7]		6		7		8		10		10	ns

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

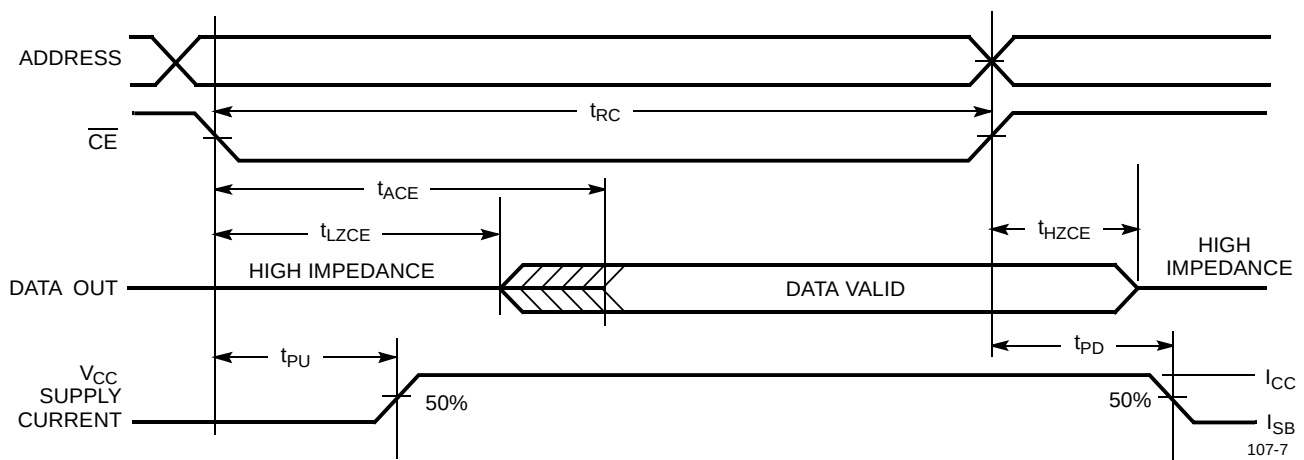
Switching Waveforms

Read Cycle No. 1^[10, 11]



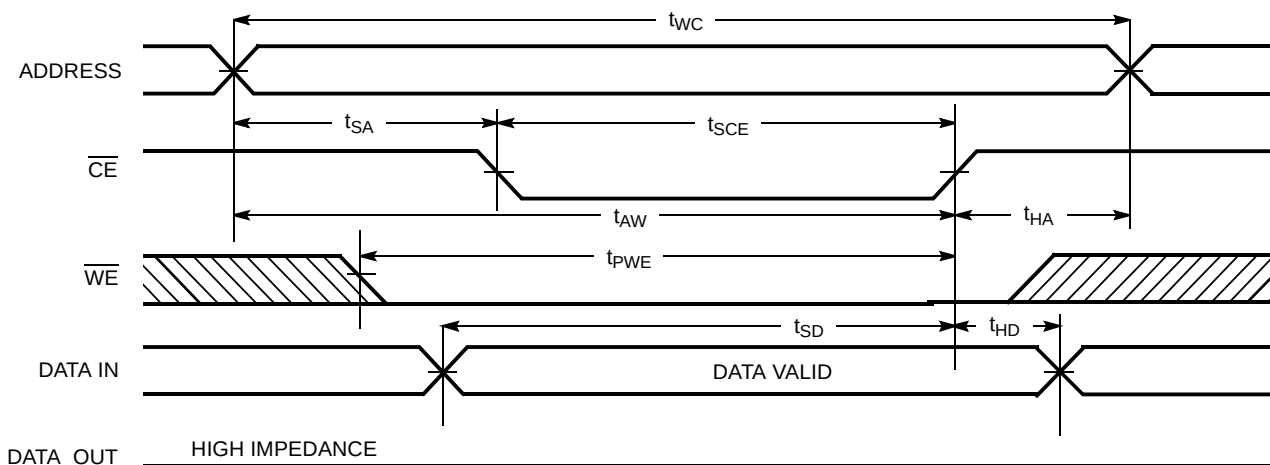
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Read Cycle No. 2^[11, 12]



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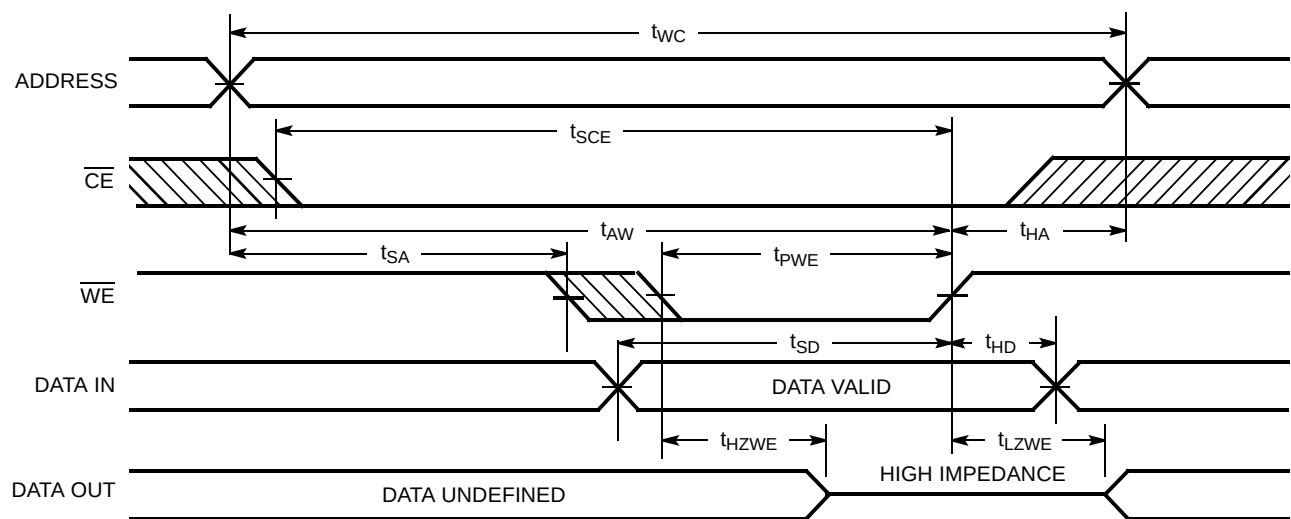
Write Cycle No. 1 (CE Controlled)^[13]



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Notes:

9. No input may exceed $V_{CC} + 0.5V$.
10. Device is continuously selected, $\overline{CE} = V_{IL}$.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)
Write Cycle No. 2 (WE Controlled)^[13]


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Note:

13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CE}$	$\overline{WE}$	D _{OUT}	Mode	Power
H	X	High Z	Power-Down	Standby (I _{SB})
L	H	Data Out	Read	Active (I _{CC})
L	L	High Z	Write	Active (I _{CC})

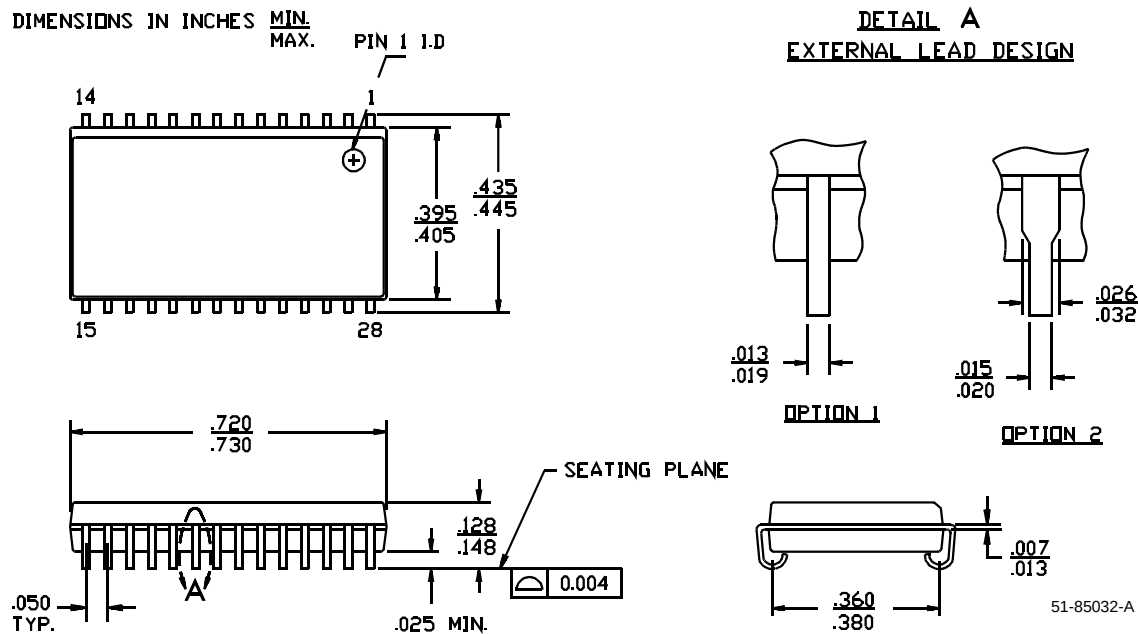
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C107B-12VC	V28	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1007B-12VC	V28	28-Lead (300-Mil) Molded SOJ	Commercial
15	CY7C107B-15VC	V28	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1007B-15VC	V28	28-Lead (300-Mil) Molded SOJ	Commercial
15	CY7C107B-15VI	V28	28-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1007B-15VI	V28	28-Lead (300-Mil) Molded SOJ	Industrial
20	CY7C107B-20VC	V28	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1007B-20VC	V28	28-Lead (300-Mil) Molded SOJ	Commercial
25	CY7C107B-25VC	V28	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1007B-25VC	V28	28-Lead (300-Mil) Molded SOJ	Commercial

Contact factory for "L" version availability.

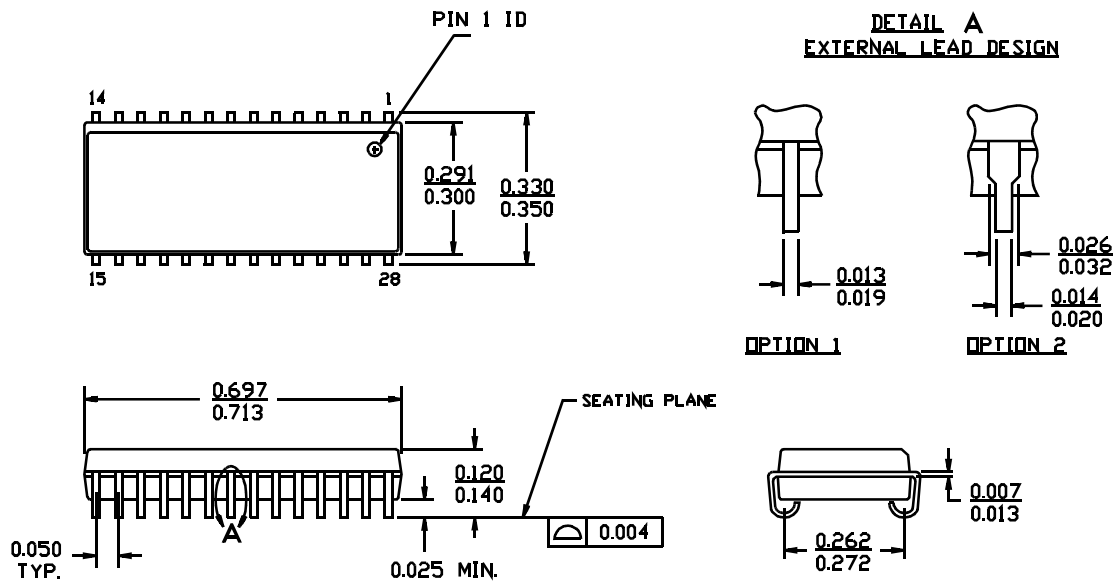
Package Diagrams

28-Lead (400-Mil) Molded SOJ V28



28-Lead (300-Mil) Molded SOJ V21

DIMENSIONS IN INCHES MIN.
MAX.





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**	109950	12/02/01	SZV	Change from Spec number: 38-01116 to 38-05030